CBCS SCHEME

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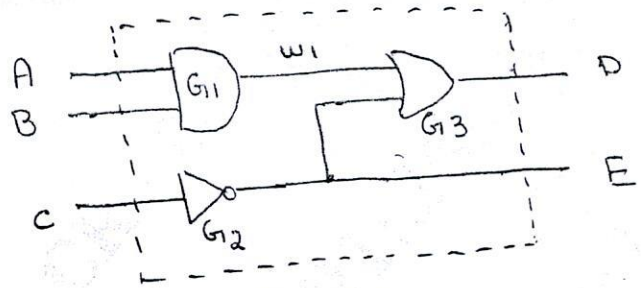
BCS302

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Determine the complement of the following function: (i) F = xy′+ x′y (ii) F = x′yz′ + x′y′z	06	L3	CO1
	b.	Describe map method for three variables.	04	L2	CO1
	c.	Apply K map technique to simplify the following function: (i) F(x, y, z) = Σ(0, 2, 4, 5, 6) (ii) F(x, y, z) = x′y + yz′ + y′z′	10	L3	CO1
		OR			
Q.2	a.	Apply K map technique to simplify the function : F(w, x, y, z) = Σ(1, 3, 7, 11, 15) and d(w, x, y, z) = Σ(0, 2, 5)	06	L3	CO1
	b.	Determine all the prime implicants for the Boolean function F and also determine which are essential F(w, x, y, z) = Σ(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)	10	L3	CO1
	c.	Develop a verilog gate-level description of the circuit shown in Fig.Q2(c).  Fig.Q2(c)	04	L3	CO1
		Module – 2			
Q.3	a.	Explain the combinational circuit design procedure with code conversion example.	10	L2	CO2
	b.	Design a full adder circuit. Also develop data flow verilog model for full adder.	10	L3	CO2
		OR			
Q.4	a.	Describe 4 × 1 MUX with block diagram and truth table. Also develop a behavioral model verilog code for 4 × 1 MUX.	10	L2	CO2
	b.	What are storage elements? Explain the working of SR and D latch along with logic diagram and function table.	10	L2	CO2
		Module – 3			
Q.5	a.	Explain the basic operational concepts between the processor and memory.	10	L2	CO3
	b.	Describe the following: (i) Processor clock (ii) Basic performance equation (iii) Clock rate (iv) SPEC rating	10	L2	CO3
		OR			
Q.6	a.	Define addressing mode. Explain any four types of addressing mode with example.	10	L2	CO3

	b.	Mention four types of operations to be performed by instructions in a computer. Explain the basic types of instruction formats to carry out. C ← [A] + [B]	10	L2	CO3
		Module – 4			
Q.7	a.	With a neat diagram, explain the concept of accessing I/O devices.	10	L2	CO4
	b.	What is bus arbitration? Explain centralized and distributed arbitration method with a neat diagram.	10	L2	CO4
		OR			
Q.8	a.	With neat sketches, explain various methods for handling multiple interrupts requests raised by multiple devices.	10	L2	CO4
	b.	What is cache memory? Explain any two mapping function of cache memory.	10	L2	CO4
		Module – 5			
Q.9	a.	Draw the single bus architecture and write the control sequence for execution of instruction ADD (R_3), R_1.	10	L3	CO5
	b.	With suitable diagram, explain the concept of register transfer and fetching of word from memory.	10	L2	CO5
		OR			
Q.10	a.	With a neat diagram, explain the flow of 4-stage pipeline operation.	10	L2	CO5
	b.	Explain the role of cache memory and pipeline performance.	10	L2	CO5

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