CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, Dec.2024/Jan.2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the construction, working and V-I characteristics of photo diode. **(06 Marks)**

b. List the different types of BJT biasing. Derive the expression for fixed bias circuit. **(06 Marks)**

c. With the help of neat circuit diagram and waveform explain the working principle of relaxation oscillator. **(08 Marks)**

OR

2 a. With a neat waveform and circuit diagram, explain the working of monostable multivibrator. **(06 Marks)**

b. Explain the working of R-2R ladder D to A converter. **(06 Marks)**

c. Explain performance parameters of a power supply. **(08 Marks)**

Module-2

3 a. A logic circuit realizing the function f has four inputs A, B, C and D. The three inputs A, B and C are the binary representation of the digits 0 through 7 with A being the most significant bit. The input D is an odd parity bit, i.e., the value of D is such that A, B, C and D always contain an odd number of 1's. (For example, the digit 1 is represented by ABC = 001 and D = 0, and the digit 3 is represented by ABCD = 0111). The function f has value 1 if the input digit is an odd number and value 0 if the input digit is an even number.

i) List the minterms and don't-care minterms of f in algebraic form.

ii) List the maxterms and don't-care maxterms of f in algebraic form. **(10 Marks)**

b. Solve for the Boolean expression using K-map to get minimum SOP and minimum POS expression:

i) $f(A, B, C, D) = \Sigma m (0, 1, 4, 8, 9, 10) + d(2, 11)$

ii) $f(A, B, C, D) = \pi M (0, 1, 3, 4, 7)$ **(10 Marks)**

OR

4 a. Determine the essential prime implicants using Q method for the function $f(A, B, C, D) = \Sigma m (0, 1, 2, 3, 10, 12, 11, 13, 14, 15)$. **(10 Marks)**

b. Explain with explain Petrik's method. **(06 Marks)**

c. Find the minimum SOP for the function $f(A, B, C) = \Sigma m(2, 6, 7)$ using Quine McCluskey method. **(04 Marks)**

Module-3

5 a. How do you detect static hazards in combinational logic circuits? Explain with examples. **(06 Marks)**

b. With a neat diagram, explain 3 to 8 line decoder. **(06 Marks)**

c. Design 7 segment decoder and realize using PLA. **(08 Marks)**

OR

6 a. Implement $Y(A, B, C, D) = \Sigma m (0, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 15)$ using 16 – to -1 multiplexer (IC 74150) and 8 – to -1 multiplexer. **(08 Marks)**

b. Implement full adder using PAL. **(08 Marks)**

c. Explain simulation and testing of digital circuits. **(04 Marks)**

Module-4

7 a. Explain the structure of VHDL program. Write VHDL code for 4-bit parallel adder using full adder as component. **(08 Marks)**

b. Construct SR latch using NAND gates and derive the characteristics equation for the same. **(08 Marks)**

c. Differentiate between latch and flip flop. Show how SR flip flop can be converted to D flip flop. **(04 Marks)**

OR

8 a. Derive the characteristics equations for D, T, SR and JK flipflops. **(08 Marks)**

b. Explain the working of a JK flip flop. Write its Truth table, state diagram and excitation table. **(08 Marks)**

c. Give the implementation of T flip flop from D flip flop. **(04 Marks)**

Module-5

9 a. What is register? Explain how 4 bit register with data, load, clear and clock input is constructed using D flip-flops. **(06 Marks)**

b. With a neat diagram, explain 4 bit SISO register. **(06 Marks)**

c. Design a random counter using T flip flops whose transition graph is shown in Fig.Q.9(c).

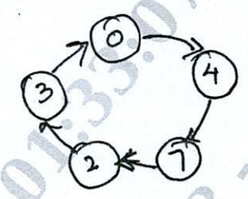

Fig.Q.9(c) **(08 Marks)**

OR

10 a. With the help of state graph, state and transistor tables and timing diagrams explain sequential parity checker. **(08 Marks)**

b. Differentiate between Moore and Melay machines. Analyze following Moore sequential circuit for an input sequence of X = 01101 and draw the timing diagram. **(08 Marks)**

c. Write a note on Ring counter. **(04 Marks)**

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