1] Descaibe the following processing methods with neat sketches.

i] Wafer processing using the Czochralski method.

ii] selective diffusion process.

:-r The basic rare material used in modern semi-Conductor plants is wafer are disc of silicon which varies from 75mm to 150mm in diameter and len than 1mmthick.

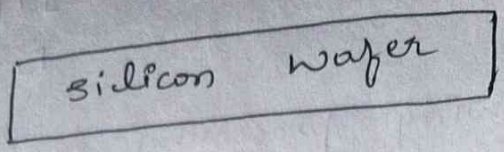
Wafer are cut from ingots of single crystal silicon that is pulled from a crucible melt of pure molten polycrystal alline silicon.

This is known as (Zochralski method and is currently most comonon method for producing Single crystall material.

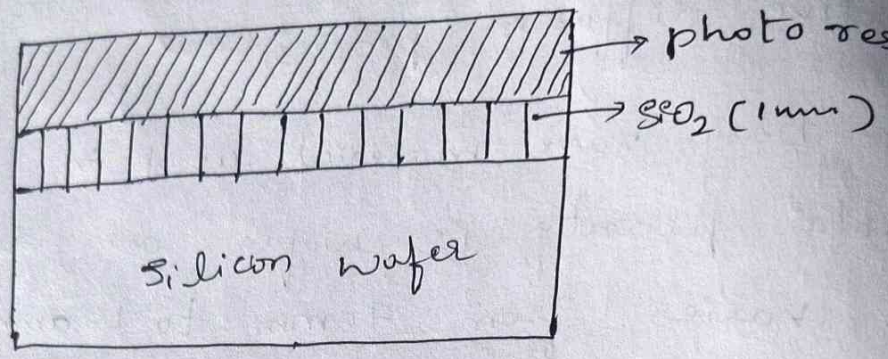
Controlled amounts of impurities are added to the melt to provide the crystall with requir electrical properties.

The crystal orienflation is deferminied by seed crystal confained in a quarth crucible that sourrounded by a graphical radiator.

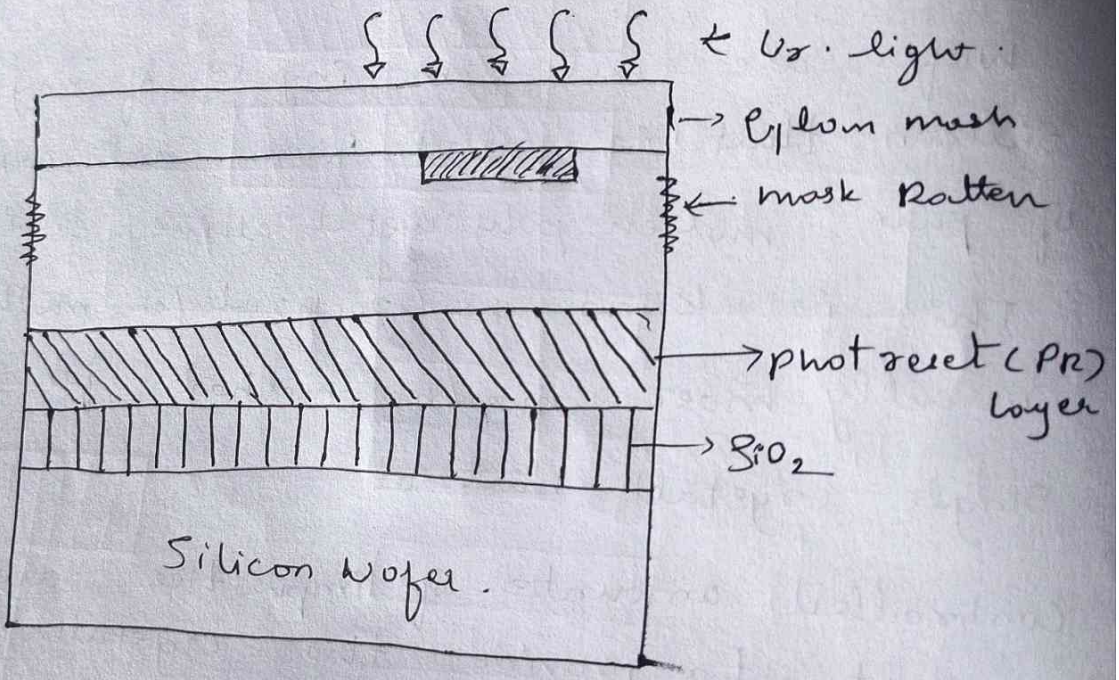
Step (1)



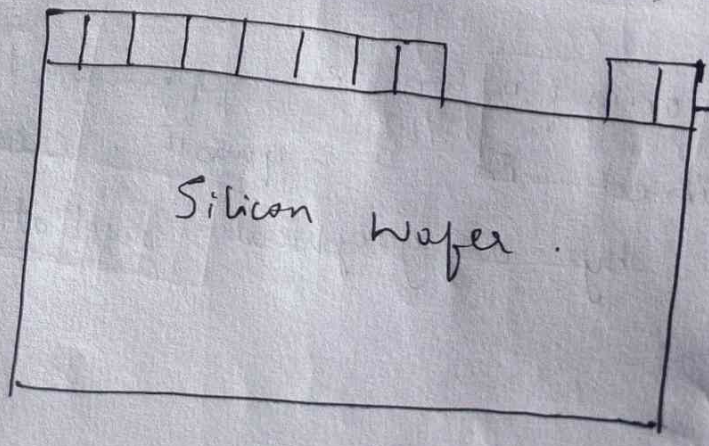
Step (2)



Step (3)

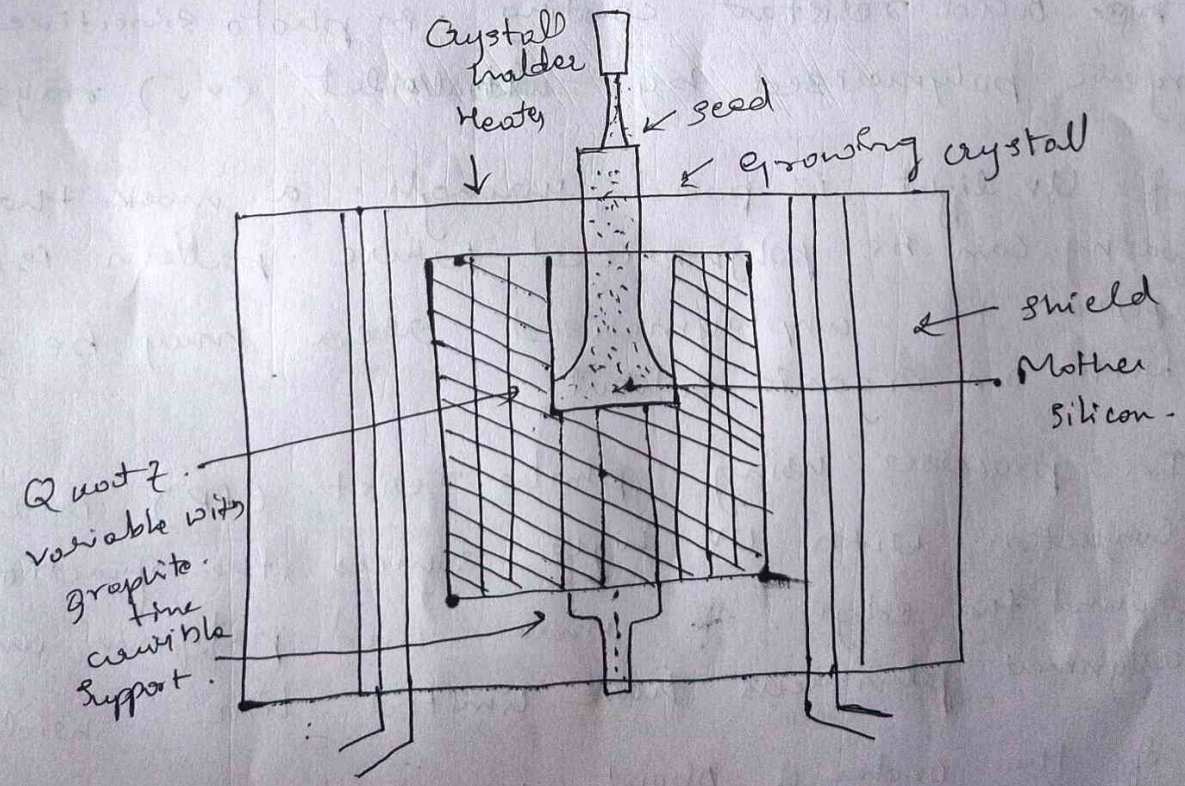


Step (4)



The atmosphere above melt is helium or argon. After seed is dipped into the melt, the seed is gradually withdrawn vertically from the melt while simultaneously being rotated.

- The molten polycrystalline silicon melts the tip of seed and as it is withdrawn, refreezing occurs.
- Slicing the wafer is usually carried out using internal cutoff edge diamond blade. Wafers are usually b/w 0.25mm to 1.0mm thick depending on their diagram.



ii] Selective diffusion process :-

* The ability of SiO_2 to act as a barrier against doping impurities in creating different types of silicon containing different portion of donor and acceptor impurities is called as selective diffusion.
* The SiO_2 layer maybe used as a pattern mask
* Area where SiO_2 overlays the silicon act as barrier to the dopant atom.
* The process used for selectively removing the oxide with an acid resistant coating.
* The SiO_2 is removed using an etching technique
* The acid resistant coating is photo sensitive organic polymerised by ultraviolet (UV) rays/light
* If UV light is posed through a mask the coating can be polymericed where pattern is/o. opaque the unpolymerised area may be moved with an organic solvent.
* In processes using photo resist (PR) in conjuction with UV light sources, the fraction around the edge of mask and pattern and alignment tolerances have limited line width of the order of about 1.5um to 2um.
* The process can be seen as follows

) Explain switching characteristic of a CMOS gate with determination of following switching times:

i) Rise time ii) Fall time iii) Delay time.

-> The switching speed of CMOS gate is limited by the time taken to charge & discharge the load capacitance C_L.

-> An output transition results in output transition that either charges C_L to V_{DD} or discharge to V_{SS}.

-> Rise time (t_r): is time for waveform to rise from 10% to 90% of it's steady state value.

-> Fall time (t_f): is time for waveform to rise from 90% to 10% of it's steady state value.

-> Delay time (t_d): is time difference between input transition (50%) and output level (50%)

Rise time (t_r) :- Fall time is faster than rise time due to different carrier mobilities associated with p and n-devices If we want approx value of rise & fall time. We need to make $\frac{\beta_n}{\beta_p} = 1$ and $W_p = W_n$ $t_r = \frac{4 C_L}{\beta_p r_{on}}$

If $\beta_n = 2\beta_p$ then $t_f = \frac{t_r}{2}$

ii] Delay time (td): The delay of single gate is dominated by the output nsers fall time the delay can be given by.

$$t_{dr} = \frac{t_r}{2} \qquad t_{df} = \frac{t_f}{2}$$

Averorge delay for rising & falling transition.

can be $t_{avg} = \frac{t_{df} + t_{dr}}{2} = \frac{t_r + t_f}{2}$

iii) Fall time (t_f):- when device is charged. to V_{DD}, the operating point changes and it moves to origin when charged it moves to origin when charged it moves to x_2 and finally down to x_3 = ~~used~~ therfore fall time consists of.

a) I_{f_1} = period during which capacitor voltage drops from V_{DD} to $V_{DD} - V_{in}$

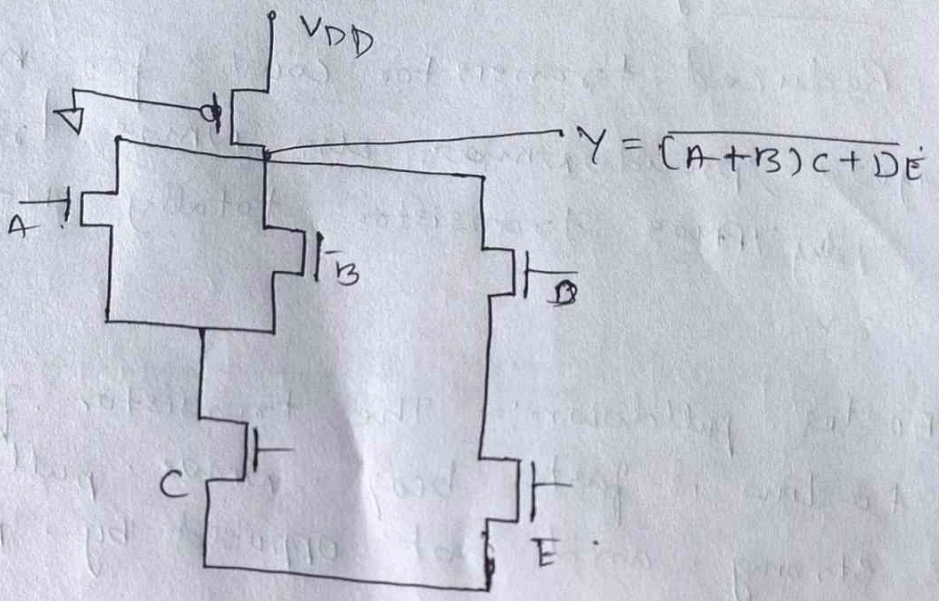
b) t_{f_2} = period during which capacitor voltage drops from $V_{DD} - V_{in}$ to $V_{DD(min)}$.

while saturation: $C_L \frac{dv_o}{dt} + \frac{B_D}{2} (V_{DD} - V_{in})$

$V_o \geq V_{DD} - V_{in}$

$t_f = 4 \cdot \frac{C_L}{B_n V_{DD}}$

3) Draw the schematic. Boolean function representation of the following $Y = \overline{(A+B)C+DE}$ using pseudo. nMOS logic and explain its operation also discuss the advantages & dis advantages of this logic.



It is kind of digital logic circuit that use combination of NMOS & PMOS it simplifies single PMOS as a pull up and multiple NMOS transistor for pull down.

Operation :-

output HIGH (logic 1) :- where Nmos pull down network is OFF.

In this state nmos don't conduct. the weak pmos load (m-p) continously pull the output Y towards Vdd

∴ Y goes to a High State.

output low (logic 0) :- NMOS is ON it pulls the output voltage down to 0V resulting in low output.

Advantage:

Reduced transistor count :- for n-of input gates, pseudo NMOS else NMOS transistor.

play 1 PMOS transistor totally N+1 full CMOS = 2V.

- Faster pulldown :- The transistor from HIGH to Low is faster bcoz. NMOS. pull down network is strong. and not opposed by - PMOS transistor turning OFF.
- simpler design.

disadvantages:

① Reduced Noise Margin :- due to low voltage doesn't reach 0V. exactly due to constant Pull by PMOS transistors.

Describe the behaviour of a two-interface basic bi-stable element?

→ Bi-stable element Circuit :-

→ It has two stable state (0/1) or operation mode each of which can be opposed under certain input and output condition.

→ The Bistable circuits are widely used all basic latch flip-flops circuit registers. memory element are used under this category.

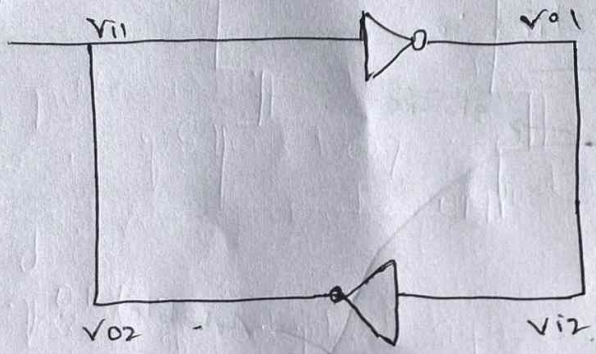
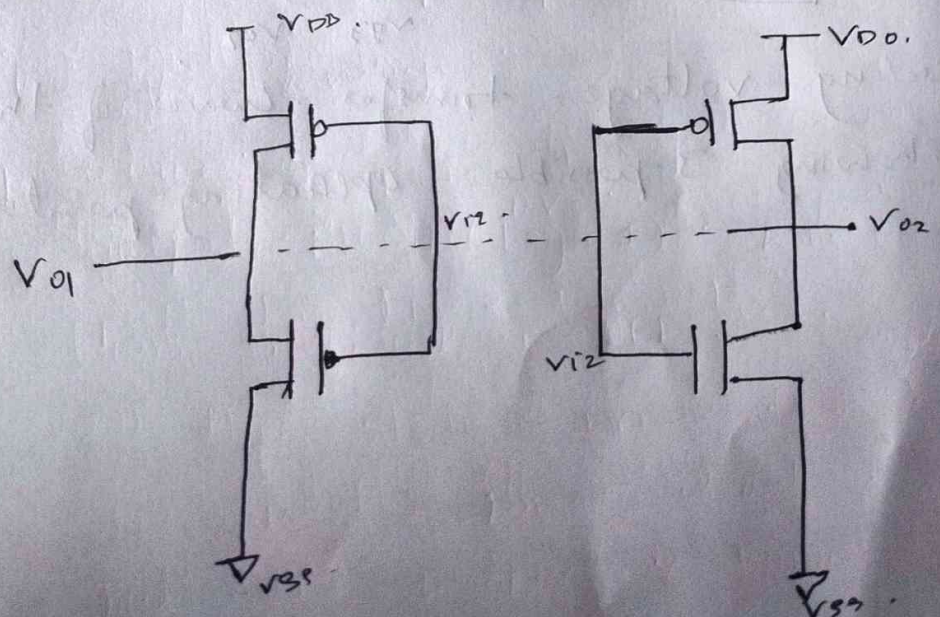


Fig 1 = static behaviour of 2 Inverter bistable elements.

Schematic Circuit :-



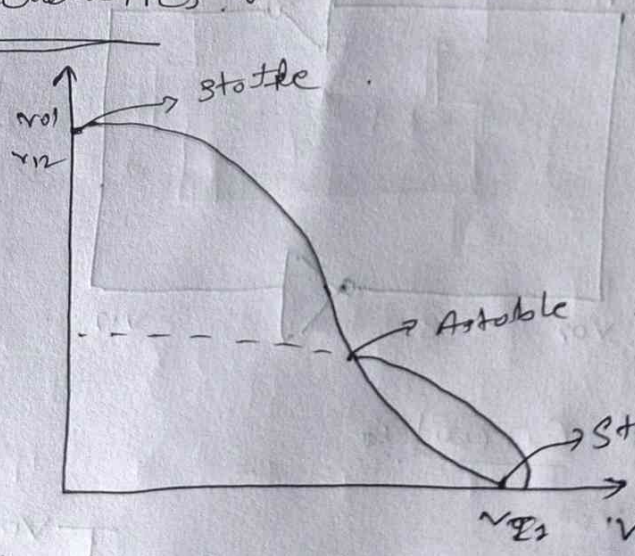
In this circuit the output voltage of Inv-1 Equal to input vdtg of Inv-2. and the output voltage of Inv-2 is Equal to input vdtg of Inv-1.

$$V_{O1} = V_{I2} \quad \rightarrow (1)$$

$$V_{O2} = V_{I1} \quad \rightarrow (2).$$

When they are connected in cross completed state two voltage transfer characteristics. can be seen of point to 3 interaction. blowes.

DC characteristics :-



Interfecting voltage transfer curves of the 2 Inverter showing 3-possible operating points.

5] Explain any four technique used for reducing the complexity of IC design. In structured design structured design strategies.

-> HIERARCHY.

-> Divide and Conquer " Strategy.

-> Divide system into modules and then into submodules till the deepest submodule in it easily implementable.

-> or prebuilt component is available. (stand Cell from library or IP).

-> the Equivalency tools to ensure consistency of each domain.

REGULARITY:-

-> Divide a system through hierarchy alone. Cannot solve the complexity.

-> We may divide a system into a large number of different submodules.

- Circuit level: uniformly sized transistor can be used.
- Gate level: Logic gates.
- Logic level: RAM's and ROM's
- Architectural level: Identical cores.

MODULARITY :-

→ In Ic modularity corresponding to a clearly defined behavioural, spectural. and physical interface

-> Inteface indicates the function name signal type electrical and timing constraints on. ports of the design

LOCACITY :

* Modularity and. locality together are a form of information hiding. which reduces complexity

* Locality means temporal locality or. adherence to. a check or a timing protocol.

Examples :-

→ Analog blocks (ADCs. and DACs) are placed adjacent to IO pads.

-> Floorplanning.

-> Local routing

06) what is purpose of layout design rule? what are the prog. constraints of layout design rule?

→ A set of layout rules also called as design rules that act as interface or communication link between the circuit designer and the process engineer during manufacturing phase.

→ The objective associated with layout rules is to obtain a circuit with optimum yield - in as small an area possible without compromising reliability of the circuit

→ Design rules can be conservative or aggressive based on whether yield or performance is desired so the need of design rules varies due to problem like photoresis, shrinkage, variation in material deposition impurities and variation in material deposition ~~in~~ across wafer

why design rule?

→ Interface between designers & process engineer

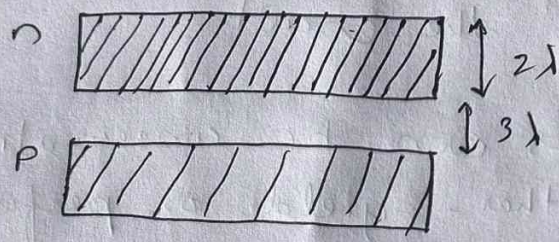
→ The process technology refered to length of silicon channel b/w source & drain terminals in field effects transistors.

iii]. Minimum spacing / separation rules.

- Diffusion - Diffusion = 3λ
- Polysilicon - polysilicon = 2λ
- polysilicon - Diffusion. = 1λ
- metal 1 - metal 1 = 3λ
- metal 2 - metal 2 = 4λ.
- Contact cuts:-

i) metal - diffusion, metal - polysilicon.
ii) polysilicon - diffusion.
iii) Buffing contact.

Example :-



n - diffusion -

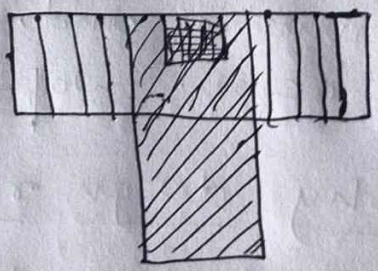
p - diffusion -

metal 1 =

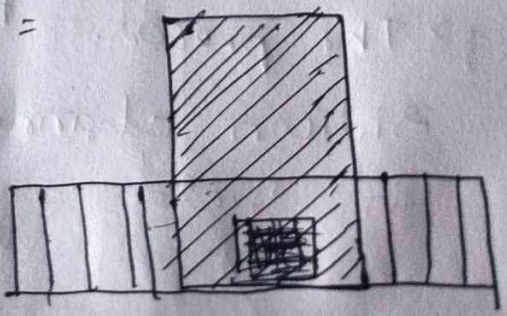
metal 2 =

Contact =

V_{DD} =



V_{SS} =



i] Minimum width layers :-

n- diffusion = 2λ

P- diffusion = 2λ

Polysilicon = 3λ.

metal 1 = 3λ

metal 2 = 4λ.

ii] Operating of layers :-

nmos transistor.