CBCS SCHEME

USN | | | | | | | | | | BEC602

Sixth Semester B.E/B.Tech. Degree Examination, June/July 2025
VLSI Design and Testing

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Compare CMOS and NMOS logic.	5	L3	CO1
	b.	With neat diagram, explain the physical representation of transmission gate.	5	L2	CO1
	c.	Design CMOS compound gate for the functions : i) $Y = \overline{A(B+C)+DE}$ ii) $Y = \overline{A}B + A\overline{B}$.	10	L3	CO1
		OR			
2	a.	Design D-flip-flop using transmission gates and explain its operation with necessary conditions on LD input.	7	L3	CO1
	b.	Illustrate different alternate circuit representations used in digital circuit designs with an example for each.	6	L2	CO1
	c.	With a neat diagram, explain the physical representation of CMOS inverter.	7	L2	CO1
		Module – 2			
3	a.	With neat diagram, explain the working of nMOS enhancement mode transistor under various voltage conditions.	6	L2	CO2
	b.	How does body effect influences threshold voltage? What are the design strategies to minimize body effect?	6	L2	CO2
	c.	For an nMOSFET, derive the equation for drain current in linear and saturation region.	8	L3	CO2
		OR			
4	a.	Explain the working of pseudo nMOS inverter. Find the output voltage equation for pseudo nMOS inverter.	6	L3	CO2
	b.	Find the expression for V_{out} in region C of CMOS inverter transfer characteristics.	8	L3	CO2
	c.	Illustrate with suitable sketch, latup phenomenon in CMOS circuits and also explain its prevention.	6	L2	CO2
		Module – 3			
5	a.	Illustrate with neat diagram wafer processing and selective diffusion.	6	L2	CO3
	b.	Derive the equation for rise time, fall time and delay time.	8	L3	CO3
	c.	Explain with neat diagram, the process flow of fabricating inverter (CMOS) using Twin-tub process.	6	L2	CO3

		OR			
6	a.	What is sheet resistance? Estimate the sheet resistance for a given layer having length 'L' and width 'W'.	7	L4	CO3
	b.	Explain the various capacitances in MOS transistor.	6	L2	CO3
	c.	Estimate the total capacitance for the structure as shown in below Fig.Q6(c).	7	L4	CO3

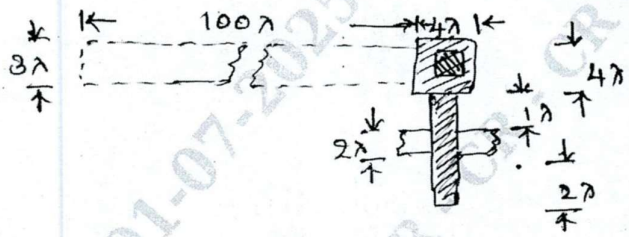

Fig.Q6(c)

		Module – 4			
7	a.	Differentiate static and dynamic CMOS circuit with relevant diagrams.	7	L3	CO4
	b.	Explain the percharge and evaluate phase in dynamic logic.	6	L2	CO4
	c.	Design a CVSL (Cascade Voltage Switch Logic) based XOR gate.	7	L3	CO4
		OR			
8	a.	Design a 2 : 1 multiplexer using pass transistor logic.	7	L3	CO4
	b.	Draw and explain the layout diagram of a 2 input NAND gate.	6	L2	CO4
	c.	Design a schematic and layout for $Z = \overline{(A + B + CD)}$ using Euler's graph.	7	L3	CO4
		Module – 5			
9	a.	With appropriate neat diagram of two inverter bistable element, explain in detail the voltage transfer characteristics (VTC) and potential energy analogy.	7	L2	CO5
	b.	Explain the operation of SR latch using CMOS NAND2 gates and switch level diagram.	6	L2	CO5
	c.	With neat appropriate diagrams, explain the clocked JK – Latch using NOR2 gates.	7	L2	CO5
		OR			
10	a.	What is structured design strategy? Explain the factors modularity, regularity and locality.	7	L2	CO5
	b.	Distinguish self-test and built-in test with examples.	6	L3	CO5
	c.	Explain with neat diagram, Gate Array Design flow.	7	L2	CO5

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1 a.

Compare CMOS and NMOS logic.

Feature	CMOS	nMOS
Logic Levels	Fully restored logic; output settles at V_{DD} or V_{SS} (GND).	Output does not settle at GND, leading to degraded noise margin.
Transition Times	Rise and fall times are of the same order.	Rise times are inherently slower than fall times.
Transmission Gates	Passes both logic levels well; output can drive other transmission gates.	Pass transistor transfers logic '0' well, but logic '1' is degraded. Cannot drive a second pass transistor.
Power Dissipation	Almost zero static power dissipation; power dissipated only during logic transition.	Power dissipated in the circuit even when output is stable, in addition to switching losses.
Precharging Characteristics	Both n-type and p-type devices can precharge a bus to V_{DD} or V_{SS}.	With enhancement-mode transistors, the best achievable precharge is $(V_{DD} - V_t)$. Bootstrapping or hot clocking is often required.
Power Supply	Voltage required to switch a gate is a fixed percentage of V_{DD}; variable range from 1.5V to 15V.	Somewhat dependent on supply voltage; fixed.
Packing Density	Requires $2N$ devices for N-input complementary static gates; fewer for dynamic gates.	Requires $(N + 1)$ devices for N-input gates.
Pull-up to Pull-down Ratio	Load-to-driver ratio typically 2:1.	Load-to-enhancement-driver ratio optimized for logic '0' level and minimal current consumption.
Layout	Encourages regular layout styles.	Depletion load and different driver transistor sizes inhibit layout regularity.

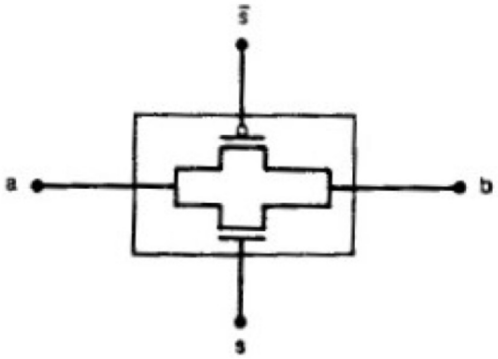
1 b.

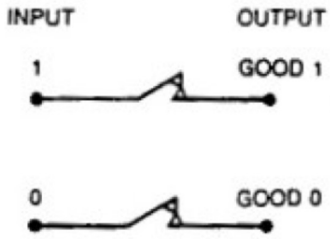
With neat diagram, explain the physical representation of transmission gate.

A transmission gate consists of an nMOS and a pMOS transistor connected in parallel. It is controlled by:

. Control signal (C) applied to nMOS.

. Complementary control signal (C) applied to pMOS.





Advantages of Transmission Gates

. Overcomes the limitations of individual nMOS and pMOS switches.

. Provides low resistance for both '0' and '1' signals.

. Used in multiplexers, flip-flops, and pass-transistor logic circuits.

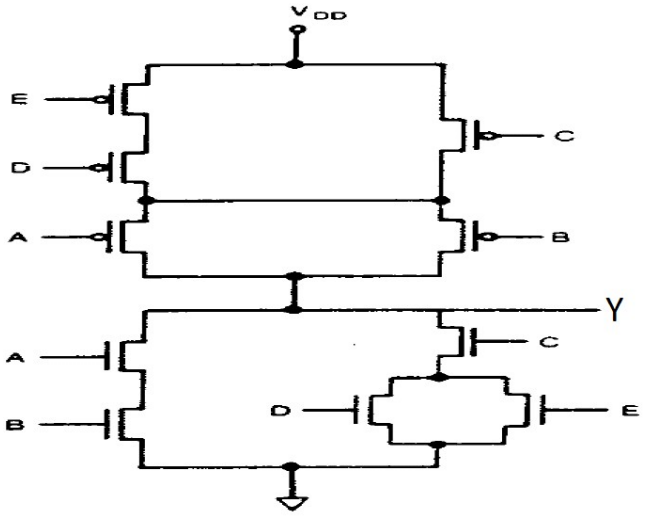
Table 1: Summary of Switch Behavior

Switch Type	Gate Signal	State	Passes '0' Well	Passes '1' Well
nMOS	1 (V_{DD})	ON	Yes	No (degraded '1')
	0 (V_{SS})	OFF	No	No
pMOS	0 (V_{SS})	ON	No (degraded '0')	Yes
	1 (V_{DD})	OFF	No	No
Transmission Gate	$C = 1, \overline{C} = 0$	ON	Yes	Yes

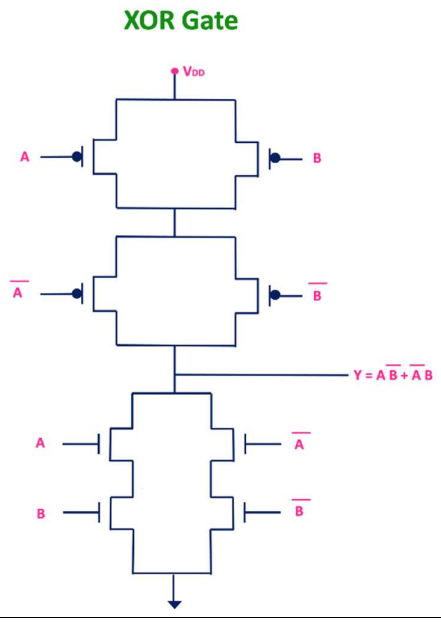
1 c. Design CMOS compound gate for the functions :

i) $Y = \overline{A(B+C)+DE}$ ii) $Y = \overline{A}B + A\overline{B}$.

i) $Y = \overline{(A.B) + C(D.E)}$



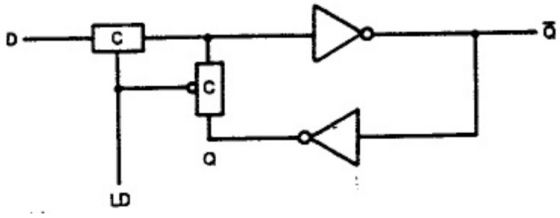
ii) $Y = \overline{A}.B + A.\overline{B}$



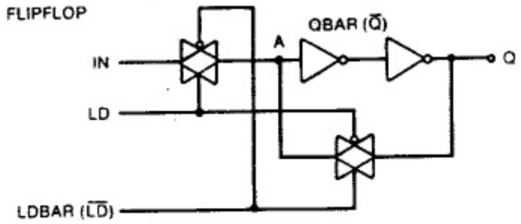
2 a.	Design D-flip-flop using transmission gates and explain its operation with necessary conditions on LD input.

Flip-Flop Using a Multiplexer and Inverters

- A simple flip-flop can be designed using a 2-input multiplexer and two inverters, as shown in figure below.



Flip - flop

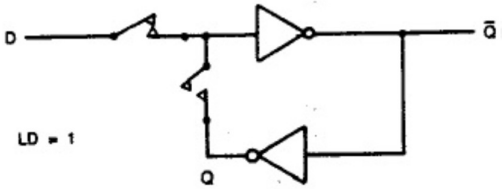


Schematic representation of CMOS flip-flop

This circuit operates based on a load signal (LD) to control data storage.

Write Mode (LD = 1)

- When the load signal is high (LD = 1):
  -The output Q is directly set to the input D.
  -This allows new data to be stored in the flip-flop.
  -This operation is illustrated in figure below.

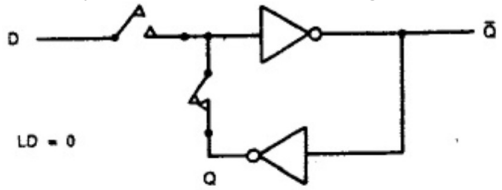


Hold Mode (LD = 0)

. When the load signal is low (LD = 0):

- The multiplexer switches to a feedback loop, connecting the output back to itself through the inverters.
- This feedback maintains the stored value, effectively holding the previous state of Q, while the input D is ignored.

. This operation is illustrated in figure below.



. This simple circuit demonstrates how memory elements can be built using fundamental CMOS components.

. Flip-flops like this serve as the foundation for registers, latches, and memory units in digital systems.

2 b.	Illustrate different alternate circuit representations used in digital circuit designs with an example for each.

Behavioral representation

- A behavioral representation defines how a system or circuit responds to a given set of inputs.
- This representation focuses on the functionality of a system rather than its implementation details, making it independent of the underlying technology.

Behavioral Specification at the Logic Level

- At the logic level, the behavior of a digital circuit can be described using Boolean functions.
- For example, the behavior of a logic gate can be expressed as: F = ((A + B + C) · D)

Structural representation

. A structural specification defines how components are interconnected to perform a function or achieve a specific behavior.

. Unlike behavioral descriptions, which focus on logical operations, structural descriptions specify the physical arrangement of circuit elements.

. One example of a structural description language is MODEL, developed by Lattice Logic Ltd. This language provides a formal way to define circuit components and their interconnections. Structural Representation in MODEL

. In MODEL, circuit elements such as transistors are explicitly defined along with their connections.

. Example 1: Inverter Description in MODEL

```
Part inv (in) -> out
Nfet out in vss
Pfet out in vdd
End
```

- The first line defines a part named inv with input in and output out.
- The Nfet transistor has its drain = out, gate = in, and source = vss.
- The Pfet transistor has its drain = out, gate = in, and source = vdd.

Physical representation

. The physical specification for a circuit is used to define how a particular part must be constructed to yield a specific structure and, consequently, a defined behavior.

. In an Integrated Circuit (IC) process, the lowest level of physical specification is the photo-mask information, which is crucial for the various processing steps during fabrication.

. At this stage, we focus on a simplified model for the physical nature of a CMOS circuit.

Transistor Physical Representation

. A typical physical representation for a transistor involves two rectangles, representing the lithography required for the transistor’ s fabrication.

. These rectangles have precise dimensions defined by the design rules, which are based on the specific process being used.

. These rules often change for different processes, and the corresponding dimensions may not change linearly.

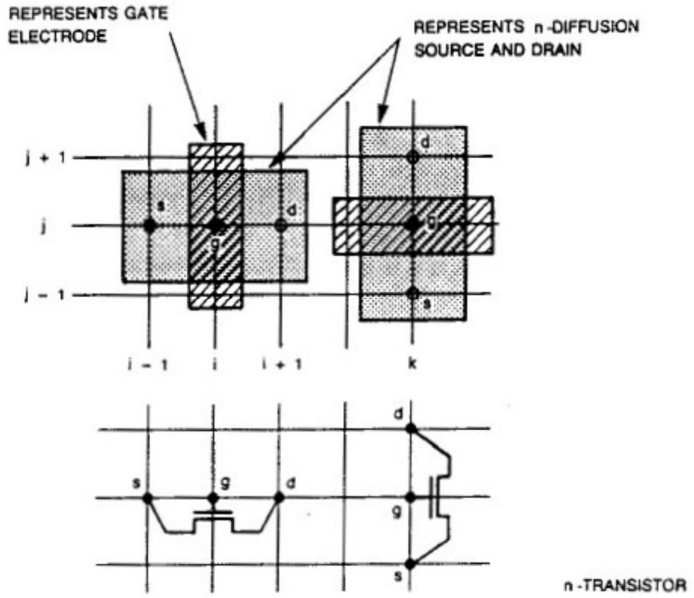
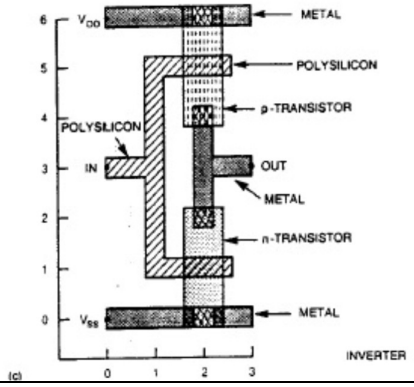
. Rather than focusing on these complex rules, we use a single symbol to represent a transistor in a non-metric format, maintaining the essential physical nature of the transistor.

n-Transistor representation

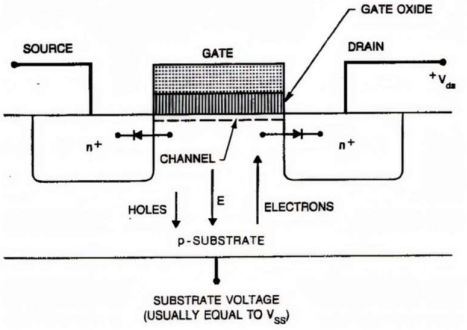
. The physical symbol for an n-transistor is shown in figure below.

. In n-transistor, two process levels are overlaid: one for the gate connection and another for the source and drain.

. These symbols are placed on a grid where:

	- The center grid point is for the gate. - The grid point to the right (or above) is the drain. - The grid point to the left (or below) is the source. . These grid points can be visualized as part of a schematic layout. 
2 c.	With a neat diagram, explain the physical representation of CMOS inverter.
	Physical Symbolic Layout for an Inverter . A symbolic layout for an inverter can be constructed using the transistor symbols. 

3 a.	With neat diagram, explain the working of nMOS enhancement mode transistor under various voltage conditions.



2.2 Principle of Operation

The operation of the nMOS transistor depends on the applied gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}).

2.2.1 With Zero Gate Bias ($V_{GS} = 0$)

- The p-type substrate prevents current flow between the source and drain because the two p-n junctions (between the n+ regions and the p-substrate) are reverse biased.
- The source and drain act as two isolated n-regions, with only leakage current flowing.

2.2.2 Applying a Positive Gate Voltage ($V_{GS} > 0$)

- The positive voltage on the gate creates an electric field (E) that repels holes and attracts electrons toward the oxide-silicon interface.
- When V_{GS} exceeds a threshold voltage (V_t), sufficient electrons accumulate to form an **inversion layer**, effectively turning the p-type region beneath the gate into an n-type channel.
- This allows current to flow between source and drain if a voltage V_{DS} is applied.

2.2.3 Field-Induced vs. Metallurgical Junction

- Unlike BJTs, where n-type conductivity is introduced via doping, the MOSFET channel is induced by an electric field.
- This field-induced junction enables voltage-controlled operation.

2.3 Operating Regions of nMOS Transistor

The nMOS transistor operates in three regions based on the applied voltages:

1. **Cutoff Region ($\mathbf{V_{GS} < V_t}$):**
   - The gate voltage is below the threshold voltage.
   - No conduction occurs except for a small leakage current.
   - The transistor acts as an open switch.
2. **Linear (Triode) Region ($\mathbf{V_{GS} > V_t}$ and $\mathbf{V_{DS} < V_{GS} - V_t}$):**
   - The inversion layer forms a conductive channel between the source and drain.
   - The transistor behaves like a voltage-controlled resistor.
   - Drain current I_{DS} is approximately proportional to V_{DS}.
   - The drain current in this region is given by:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1}$$

   where:

μ_n is the electron mobility.
C_{ox} is the gate oxide capacitance per unit area.
W is the channel width.
L is the channel length.

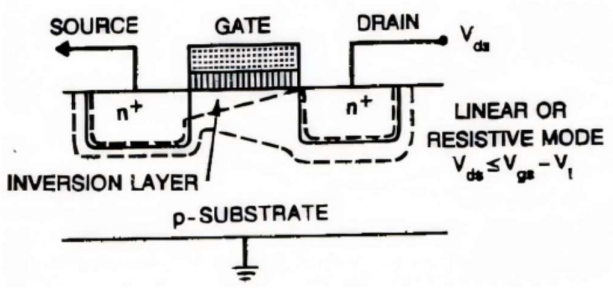


Figure 3: nMOS in Linear region

3. **Saturation Region ($\mathbf{V_{GS} > V_t}$ and $\mathbf{V_{DS} > V_{GS} - V_t}$):**

- The channel becomes **pinched off** at the drain end.
- The drain current is primarily controlled by V_{GS} and is almost independent of V_{DS}.
- The drain current in this region is given by:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2 \tag{2}$$

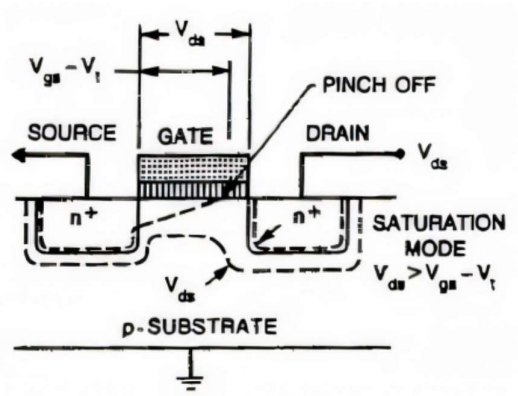


Figure 4: nMOS in Saturation region

- **Pinch-Off and Channel Behavior**
  - At the source end, the full gate voltage is effective.
  - At the drain end, only $(V_{GS} - V_{DS})$ is effective.
  - When $V_{DS} > V_{GS} - V_t$, the channel is **pinched off**.
  - Electrons drift toward the drain due to the electric field.

3 b.	How does body effect influences threshold voltage? What are the design strategies to minimize body effect?

Body Effect

- In MOSFETs, the **body effect** (also known as the **substrate bias effect**) occurs when the voltage difference between the **source** and **substrate** (V_{sb}) affects the **threshold voltage** (V_t).
- This effect becomes significant in circuits where multiple transistors are connected in series, such as in CMOS logic gates, because the substrate voltage is usually common for all transistors.
  - In most MOS circuits, all transistors share a **common substrate**.
  - Under normal conditions, the substrate voltage remains the same for all transistors.
  - However, in certain configurations — especially when multiple MOSFETs are connected in series — this assumption no longer holds.
  - Consider a chain of MOSFETs connected in series, as shown in figure above.
  - The first transistor in the series may have its source directly connected to ground, leading to a source-to-substrate voltage of **zero** ($V_{sb1} = 0$).
  - However, for the second transistor in the series, its source is connected to the drain of the first transistor, which is at a **higher potential**.
  - This results in a nonzero source-to-substrate voltage ($V_{sb2} \neq 0$).
  - As we move along the series chain, V_{sb} continues to increase.

6.2 How the Body Effect Alters the Threshold Voltage

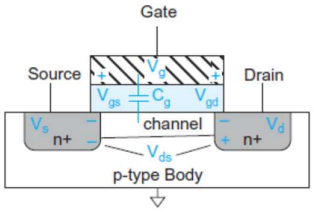
- The **threshold voltage** of a MOSFET is the minimum gate-to-source voltage (V_{gs}) required to form a conductive channel between the source and drain.
- Under normal conditions, when $V_{gs} > V_t$, a **channel** is formed, and charge carriers (electrons in nMOS or holes in pMOS) flow from the source to the drain.
- When V_{sb} increases, it affects the **depletion region** at the substrate-channel junction:
  - The **depletion layer width** increases.
  - More **charge carriers** get trapped in the depletion layer.
  - To maintain **charge neutrality**, the available **channel charge decreases**.
- Since the channel charge is reduced, the gate must apply **more voltage** to invert the channel.
- This means that the **threshold voltage** (V_t) increases, making it harder to turn the transistor **ON**.
- This phenomenon is called the **body effect**.

3 c.	For an nMOSFET, derive the equation for drain current in linear and saturation region.

The long-channel model assumes that the current through an OFF transistor is 0. When a transistor turns ON ($V_{gs} > V_t$), the gate attracts carriers (electrons) to form a channel. The electrons drift from source to drain at a rate proportional to the electric field between these regions. Thus, we can compute currents if we know the amount of charge in the channel and the rate at which it moves. We know that the charge on each plate of a capacitor is $Q = CV$. Thus, the charge in the channel $Q_{channel}$ is

$$Q_{channel} = C_g\left(V_{gc} - V_t\right) \tag{2.1}$$

where C_g is the capacitance of the gate to the channel and $V_{gc} - V_t$ is the amount of voltage attracting charge to the channel beyond the minimum required to invert from p to n. The gate voltage is referenced to the channel, which is not grounded. If the source is at V_s and the drain is at V_d, the average is $V_c = (V_s + V_d)/2 = V_s + V_{ds}/2$. Therefore, the mean difference between the gate and channel potentials V_{gc} is $V_g - V_c = V_{gs} - V_{ds}/2$, as shown in Figure 2.5.



Average gate to channel potential:

$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$

FIGURE 2.5 Average gate to channel voltage

We can model the gate as a parallel plate capacitor with capacitance proportional to area over thickness. If the gate has length L and width W and the oxide thickness is t_{ox}, as shown in Figure 2.6, the capacitance is

$$C_g = k_{ox}\varepsilon_0 \frac{WL}{t_{ox}} = \varepsilon_{ox}\frac{WL}{t_{ox}} = C_{ox}WL \tag{2.2}$$

where ε_0 is the permittivity of free space, 8.85×10^{-14} F/cm, and the permittivity of SiO_2 is $k_{ox} = 3.9$ times as great. Often, the ε_{ox}/t_{ox} term is called C_{ox}, the capacitance per unit area of the gate oxide.

Some nanometer processes use a different gate dielectric with a higher dielectric constant. In these processes, we call t_{ox} the *equivalent oxide thickness* (EOT), the thickness of a layer of SiO_2 that has the same C_{ox}. In this case, t_{ox} is thinner than the actual dielectric.

Each carrier in the channel is accelerated to an average velocity, v, proportional to the lateral electric field, i.e., the field between source and drain. The constant of proportionality μ is called the *mobility*.

$$v = \mu E \tag{2.3}$$

A typical value of μ for electrons in an nMOS transistor with low electric fields is 500–700 $cm^2/V \cdot s$. However, most transistors today operate at far higher fields where the mobility is severely curtailed (see Section 2.4.1).

The electric field E is the voltage difference between drain and source V_{ds} divided by the channel length

$$E = \frac{V_{ds}}{L} \tag{2.4}$$

The time required for carriers to cross the channel is the channel length divided by the carrier velocity: L/v. Therefore, the current between source and drain is the total amount of charge in the channel divided by the time required to cross

$$\begin{aligned} I_{ds} &= \frac{Q_{channel}}{L/v} \\ &= \mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \\ &= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} \end{aligned} \tag{2.5}$$

where

$$\beta = \mu C_{ox}\frac{W}{L};\ V_{GT} = V_{gs} - V_t \tag{2.6}$$

The term $V_{gs} - V_t$ arises so often that it is convenient to abbreviate it as V_{GT}. EQ (2.5) describes the linear region of operation, for $V_{gs} > V_t$, but V_{ds} relatively small. It is called *linear* or *resistive* because when $V_{ds} << V_{GT}$, I_{ds} increases almost linearly with V_{ds}, just like an ideal resistor. The geometry and technology-dependent parameters are sometimes merged into a single factor β. Do not confuse this use of β with the same symbol used for the ratio of collector-to-base current in a bipolar transistor. Some texts [Gray01] lump the technology-dependent parameters alone into a constant called "k prime."[3]

$$k' = \mu C_{ox} \tag{2.7}$$

If $V_{ds} > V_{dsat} \equiv V_{GT}$, the channel is no longer inverted in the vicinity of the drain; we say it is pinched off. Beyond this point, called the *drain saturation voltage*, increasing the drain voltage has no further effect on current. Substituting $V_{ds} = V_{dsat}$ at this point of maximum current into EQ (2.5), we find an expression for the saturation current that is independent of V_{ds}.

$$I_{ds} = \frac{\beta}{2} V_{GT}^2 \tag{2.8}$$

This expression is valid for $V_{gs} > V_t$ and $V_{ds} > V_{dsat}$. Thus, long-channel MOS transistors are said to exhibit *square-law behavior* in saturation.

Two key figures of merit for a transistor are I_{on} and I_{off}. I_{on} (also called I_{dsat}) is the ON current, I_{ds}, when $V_{gs} = V_{ds} = V_{DD}$. I_{off} is the OFF current when $V_{gs} = 0$ and $V_{ds} = V_{DD}$. According to the long-channel model, $I_{off} = 0$ and

$$I_{on} = \frac{\beta}{2}\left(V_{DD} - V_t\right) \tag{2.9}$$

EQ (2.10) summarizes the current in the three regions:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} & \text{Linear} \\ \dfrac{\beta}{2} V_{GT}^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases} \tag{2.10}$$

4 a.	Explain the working of pseudo nMOS inverter. Find the output voltage equation for pseudo nMOS inverter.

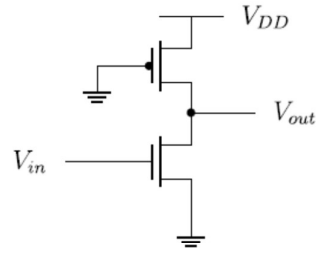


Figure 15: Pseudo-nMOS Inverter

- A **pseudo-nMOS inverter** is a variation of the standard CMOS inverter, where the **pMOS pull-up transistor has its gate permanently grounded**.
- This design is similar to using a **depletion-mode transistor** as a load in nMOS logic.

4 b.	Find the expression for V_{out} in region C of CMOS inverter transfer characteristics.

Region C. In this region both the n- and p-devices are in saturation. The saturation currents for the two devices are given by

$$I_{ds_p} = \frac{1}{2}\beta_p(V_{in} - V_{DD} - V_{t_p})^2$$

$$I_{ds_n} = \frac{1}{2}\beta_n(V_{in} - V_{t_n})^2$$

with

$$I_{ds_p} = -I_{ds_n}.$$

This yields

$$V_{in} = \frac{V_{DD} + V_{t_p} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}. \qquad (2.20)$$

By setting

$$\beta_n = \beta_p \text{ and } V_{t_n} = -V_{t_p},$$

we obtain

$$V_{in} = \frac{V_{DD}}{2}, \qquad (2.21)$$

which implies that region C exists for only one value of V_{in}. The possible values of V_O in this region can be deduced as follows:

$$\text{n-channel:} \quad V_{in} - V_O < V_{tn}$$
$$V_O > V_{in} - V_{tn}$$
$$\text{p-channel:} \quad V_{in} - V_O > V_{tp}$$
$$V_O < V_{in} - V_{tp}.$$

Combining the two inequalities results in

$$V_{in} - V_{tn} < V_O < V_{in} - V_{tp}. \qquad \textbf{(2.22)}$$

4 c. Illustrate with suitable sketch, latup phenomenon in CMOS circuits and also explain its prevention.

14 Latch-up in CMOS

- Latch-up is a parasitic circuit effect that causes a low-resistance path between power supply rails (VDD and VSS) in CMOS circuits.
- This results in excessive current flow, leading to circuit failure or permanent damage.
- Early CMOS processes were highly susceptible to latch-up, but modern fabrication techniques and circuit design strategies have significantly mitigated this issue.

14.1 Mechanism of Latch-up

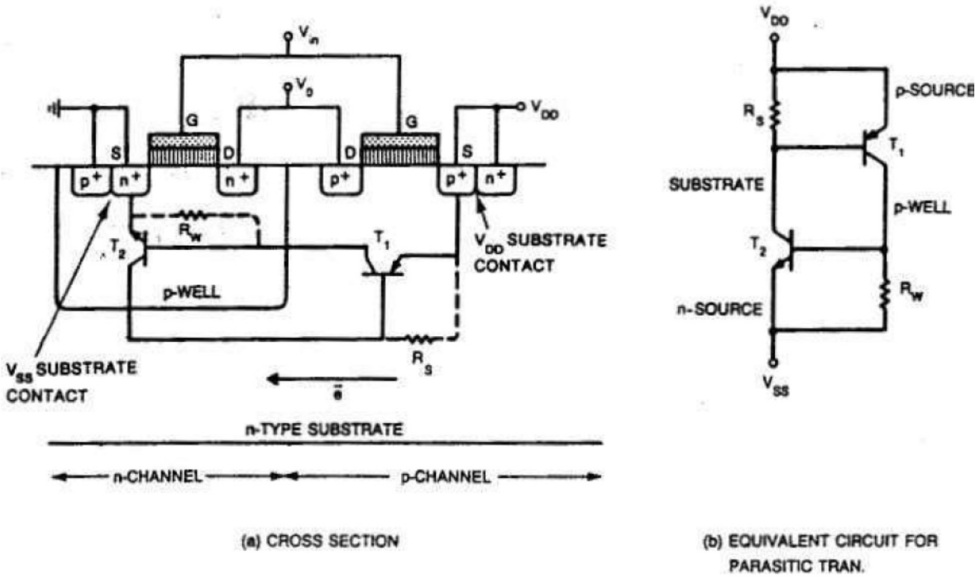
- Latch-up occurs due to the presence of **parasitic bipolar junction transistors (BJTs)** within the CMOS structure.
- These unintended transistors can form a positive feedback loop, causing a short circuit between VDD and VSS.

14.1.1 Parasitic Bipolar Transistor Formation

A CMOS structure consists of nMOS transistors in a *p-well* and pMOS transistors in an *n-substrate*. Two parasitic bipolar transistors—**npn** and **pnp**—are inadvertently formed:

- The **npn transistor** consists of:
  - **Emitter**: n+ source/drain of nMOS
  - **Base**: p-well
  - **Collector**: n-substrate

- The **pnp transistor** consists of:
  - **Emitter**: p+ source/drain of pMOS
  - **Base**: n-substrate
  - **Collector**: p-well



(a) CROSS SECTION

(b) EQUIVALENT CIRCUIT FOR PARASITIC TRAN.

Latch-up occurs when:

1. **Excess carrier injection**: Voltage spikes or transient currents inject minority carriers into the substrate or well.
2. **Voltage drop across Rs and Rw**: If sufficient voltage develops, it can forward bias the base-emitter junctions of the parasitic transistors.
3. **Positive feedback activation**: The feedback loop between the npn and pnp transistors sustains the low-resistance state.

To prevent latch-up, the following design strategies are implemented:

14.2.1 Substrate and Well Contacting

- Every well should have a **substrate contact**.
- Substrate contacts should be directly connected to supply pads using metal.
- Contacts should be placed **close to transistor source connections** to reduce resistance.

14.2.2 Transistor Placement Guidelines

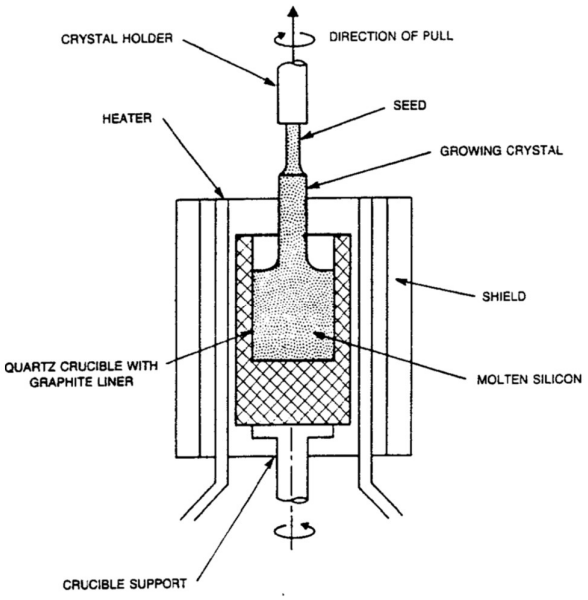
- Maintain **separation** between nMOS and pMOS devices.
- Group nMOS transistors closer to **VSS** and pMOS transistors closer to **VDD**.
- Avoid **checkerboard-style layouts**.

14.2.3 I/O Structure Design

- Use **guard rings** (p+ around nMOS, n+ around pMOS).
- Employ **minimum-area p-wells** to reduce photocurrent injection.
- Hard-wire the **p-well to ground (via p+ contact)**.
- Reduce **spacing between p-well and nMOS source contact**.

5 a.	Illustrate with neat diagram wafer processing and selective diffusion.

Wafer Processing



The basic raw material used in modern semiconductor plants is a *wafer* or disk of silicon, which varies from 75 mm to 150 mm in diameter and is less than 1 mm thick. Wafers are cut from ingots of single crystal silicon that have been pulled from a crucible melt of pure molten polycrystalline silicon. This is known as the "Czochralski" method (Fig. 3.1) and is currently the most common method for producing single crystal material. Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties. The crystal *orientation* is determined by a *seed* crystal that is dipped into the melt to initiate single crystal growth. The melt is contained in a quartz crucible, which is surrounded by a graphite radiator. The graphite is heated by radio frequency induction and the temperature is maintained a few degrees above the melting point of silicon (≈1425° C). The atmosphere above the melt is typically helium or argon.

After the seed is dipped into the melt, the seed is gradually withdrawn vertically from the melt while simultaneously being rotated. The molten polycrystalline silicon melts the tip of the seed and as it is withdrawn, refreezing occurs. As the melt freezes, it assumes the single crystal form of the seed. This process is continued until the melt is consumed. The diameter of the ingot is determined by the seed withdrawal rate and the seed rotation rate. Growth rates range from 30 to 180 mm/hour.

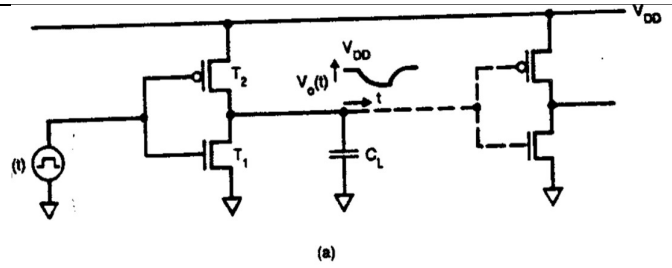
Slicing into wafers is usually carried out using internal cutting edge diamond blades. Wafers are usually between 0.25 mm and 1.0 mm thick, depending on their diameter. Following this operation, at least one face is polished to a flat, scratch-free mirror finish.

Selective Diffusion

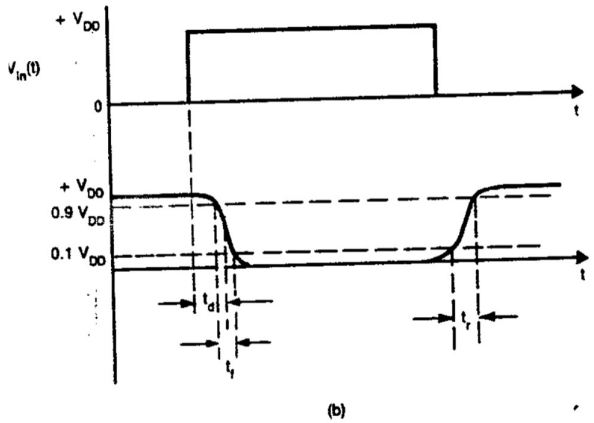
To create different types of silicon, containing different proportions of donor or acceptor impurities, further processing is required. As these areas are required to be precisely placed and sized, a means of ensuring this is required. The ability of SiO_2 to act as a barrier against doping impurities is a vital factor in this process called *selective diffusion*. The SiO_2 layer may be used as a *pattern mask*. Areas on the silicon wafer surface where there is an absence of SiO_2 allow dopant atoms to pass into the wafer, thus changing the characteristics of the silicon. Areas where SiO_2 overlays the silicon act as barriers to the dopant atoms. Thus selective diffusion entails:

- Opening windows in a layer of SiO_2 grown on the surface of the wafer.
- Removing SiO_2, but not Si, with a suitable etchant.
- Subjecting exposed Si to a dopant source.

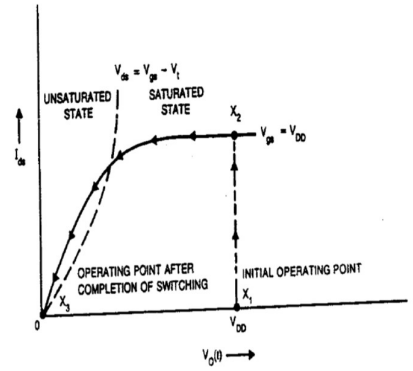
5 b. Derive the equation for rise time, fall time and delay time.



(a)



(b)



1 t_{f1} = period during which the capacitor voltage, V_o, drops from 0.9 V_{DD} to ($V_{DD} - V_{tn}$).

2 t_{f2} = period during which the capacitor voltage, V_o, drops from ($V_{DD} - V_{tn}$) to 0.1 V_{DD}.

The equivalent circuits that illustrate the above behavior are shown in Fig. 4.17. From Fig. 4.17a, while in saturation

$$C_L \frac{dV_o}{dt} + \frac{\beta_n}{2}(V_{DD} - V_{tn})^2 = 0; \qquad V_o \geq V_{DD} - V_{tn}. \tag{4.21}$$

Integrating from $t = t_1$, corresponding to $V_o = 0.9\ V_{DD}$, to $t = t_2$ corresponding to $V_o = (V_{DD} - V_{tn})$ results in

$$t_{f1} = 2\frac{C_L}{\beta_n(V_{DD} - V_{tn})^2}\int_{V_{DD}-V_{tn}}^{0.9V_{DD}} dV_o = \frac{2C_L(V_{tn} - 0.1\ V_{DD})}{\beta_n(V_{DD} - V_{tn})^2}. \tag{4.22}$$

When the n-device begins to operate in the linear region, the discharge current is no longer constant. The time, t_{f2}, taken to discharge the capacitor voltage from ($V_{DD} - V_{tn}$) to 0.1 V_{DD} can be obtained as before, giving

$$t_{f2} = \frac{C_L}{\beta_n(V_{DD} - V_{tn})}\int_{0.1V_{DD}}^{V_{DD}-V_{tn}} \frac{dV_o}{\frac{V_o^2}{2(V_{DD} - V_{tn})} - V_o} = \frac{C_L}{\beta_n(V_{DD} - V_{tn})}\ln\left(\frac{19\ V_{DD} - 20\ V_{tn}}{V_{DD}}\right). \tag{4.23}$$

Thus the complete term for the fall time, t_f is

$$t_f = 2\frac{C_L}{\beta_n(V_{DD} - V_{tn})} \times \left[\frac{V_{tn} - 0.1\ V_{DD}}{V_{DD} - V_{tn}} + \frac{1}{2}\ln\left(\frac{19\ V_{DD} - 20\ V_{tn}}{V_{DD}}\right)\right]. \tag{4.24}$$

If we make the assumption that $V_{tn} \simeq 0.2\ V_{DD}$ (in a 5 volt process $V_{tn} = 1$ v $V_{tp} \simeq -1$ v), then t_f can be approximated as

$$t_f \simeq 4\frac{C_L}{\beta_n V_{DD}}. \tag{4.25}$$

4.4.2 Rise time

Due to the symmetry of the CMOS circuit, a similar approach may be used to obtain the rise time, t_r (Fig. 4.17b). Thus

$$t_r = 2\frac{C_L}{\beta_p(V_{DD} - |V_{tp}|)} \times \left[\frac{|V_{tp}| - 0.1\ V_{DD}}{V_{DD} - |V_{tp}|} + \frac{1}{2}\ln\left(\frac{19\ V_{DD} - 20|V_{tp}|}{V_{DD}}\right)\right]. \tag{4.26}$$

As before, with $|V_{tp}| \simeq 0.2\ V_{DD}$, Eq. (4.26) reduces to

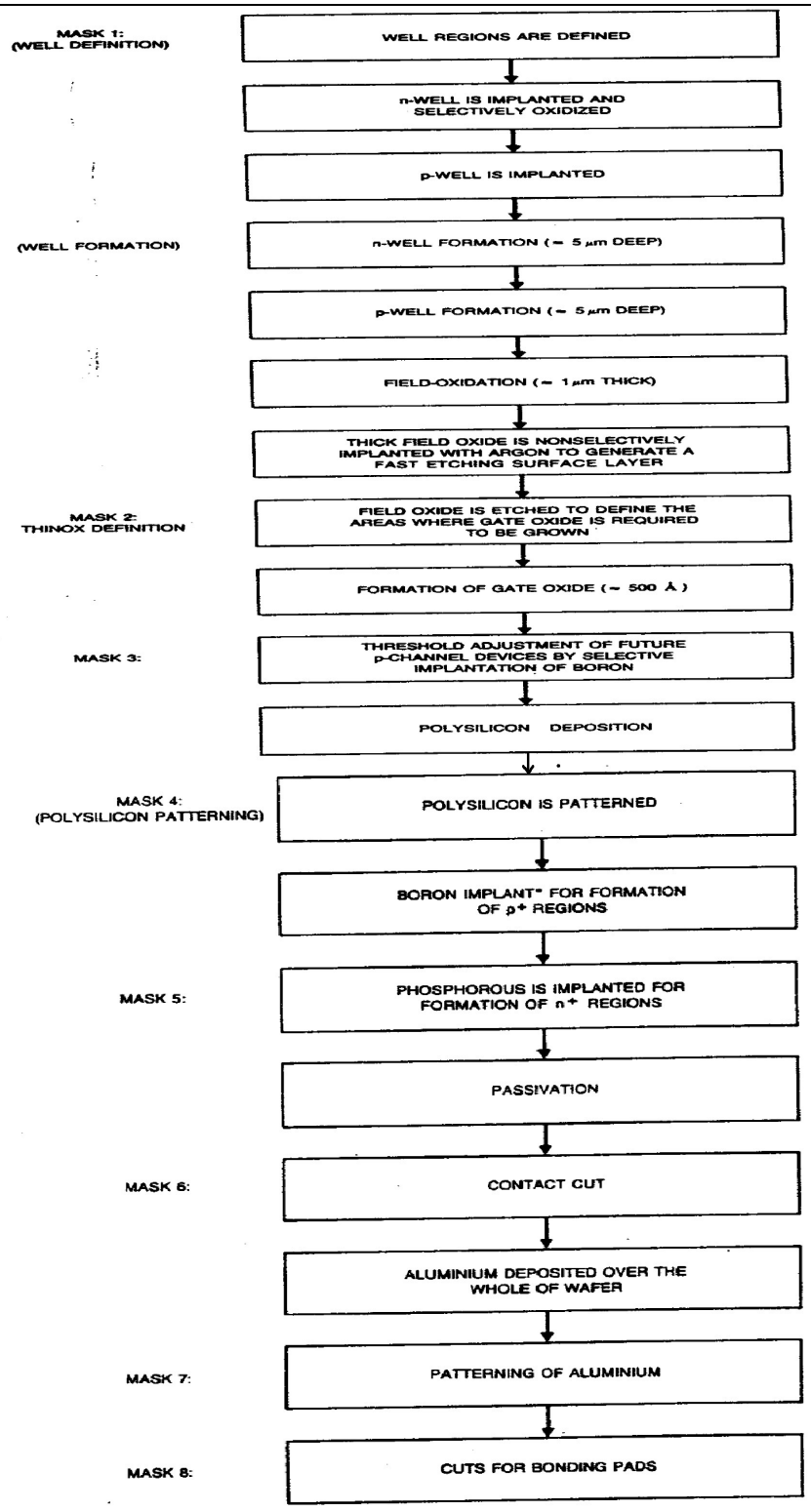
$$t_r \simeq 4\frac{C_L}{\beta_p V_{DD}}. \tag{4.27}$$

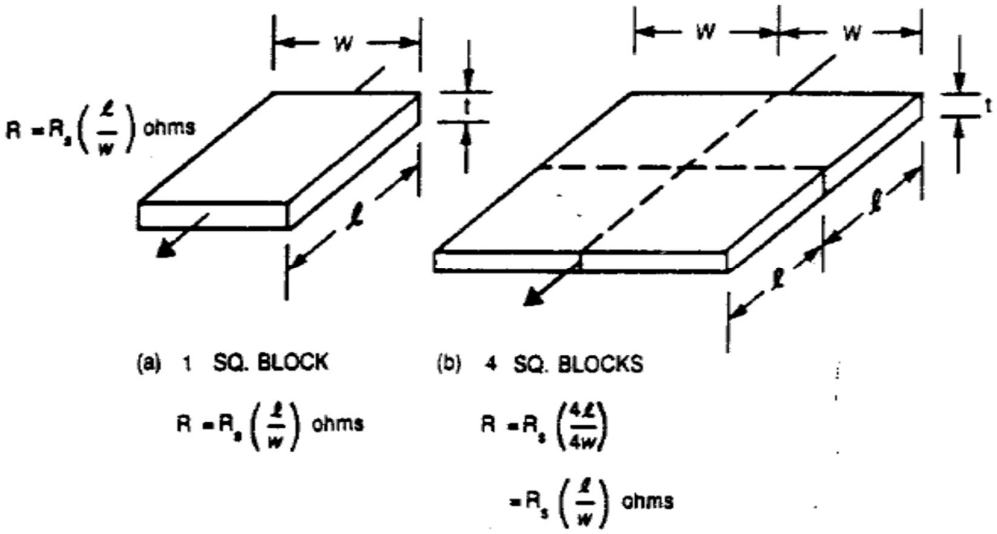
For equally sized n- and p-transistors, where $\beta_n = 2\beta_p$

$$t_f = \frac{t_r}{2}. \tag{4.28}$$

Thus the fall time is faster than the rise time, primarily due to different carrier mobilities associated with the p- and n-devices (i.e.,

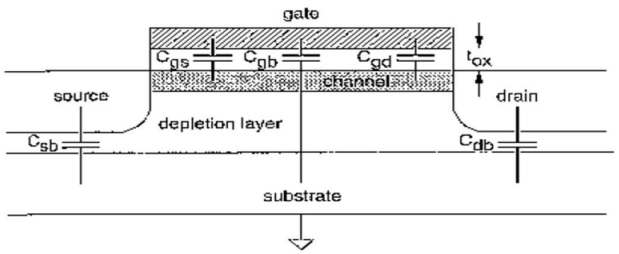
5 c.	Explain with neat diagram, the process flow of fabricating inverter (CMOS) using Twin-tub process.
	Twin-tub CMOS technology provides the basis for separate optimization of the p-type and n-type transistors, thus making it possible for threshold voltage, body effect, and the gain associated with n- and p-devices to be independently optimized [Parr80]. Generally the starting material is either an n^+ or p^- substrate with a lightly doped *epitaxial* or *epi* layer, which is used for protection against latch-up. The aim of *epitaxy* (which means "arranged upon") is to grow high purity silicon layers of controlled thickness with accurately determined dopant concentrations distributed homogeneously throughout the layer. The electrical properties for this layer are determined by the dopant and its concentration in the silicon. **The process sequence, which is similar to the p-well process apart from the tub formation where both p-well and n-well are utilized, entails the following steps:** • **tub formation** • **thin oxide etching** • **source and drain implantations** • **contact cut definition** • **metallization.**


MASK 1:
(WELL DEFINITION)
WELL REGIONS ARE DEFINED
n-WELL IS IMPLANTED AND SELECTIVELY OXIDIZED
p-WELL IS IMPLANTED
(WELL FORMATION)
n-WELL FORMATION (~ 5 μm DEEP)
p-WELL FORMATION (~ 5 μm DEEP)
FIELD-OXIDATION (~ 1 μm THICK)
THICK FIELD OXIDE IS NONSELECTIVELY IMPLANTED WITH ARGON TO GENERATE A FAST ETCHING SURFACE LAYER
MASK 2:
THINOX DEFINITION
FIELD OXIDE IS ETCHED TO DEFINE THE AREAS WHERE GATE OXIDE IS REQUIRED TO BE GROWN
FORMATION OF GATE OXIDE (~ 500 Å)
MASK 3:
THRESHOLD ADJUSTMENT OF FUTURE p-CHANNEL DEVICES BY SELECTIVE IMPLANTATION OF BORON
POLYSILICON DEPOSITION
MASK 4:
(POLYSILICON PATTERNING)
POLYSILICON IS PATTERNED
BORON IMPLANT* FOR FORMATION OF p+ REGIONS
MASK 5:
PHOSPHOROUS IS IMPLANTED FOR FORMATION OF n+ REGIONS
PASSIVATION
MASK 6:
CONTACT CUT
ALUMINIUM DEPOSITED OVER THE WHOLE OF WAFER
MASK 7:
PATTERNING OF ALUMINIUM
MASK 8:
CUTS FOR BONDING PADS

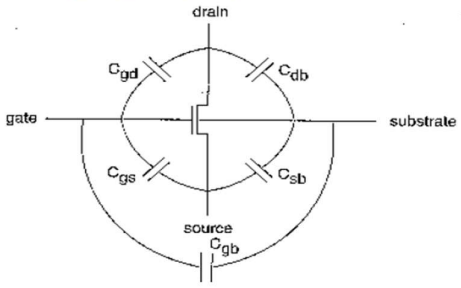
6 a.	What is sheet resistance? Estimate the sheet resistance for a given layer having length 'L' and width 'W'.
	Resistance Estimation The resistance of a uniform conducting slab is $R=\left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right)=R_s\left(\frac{l}{w}\right)$ where ρ = resistivity. t = thickness. l = conductor length. w = conductor width. R_s = Sheet resistance having units of $\Omega/square$ According to the above formula, the two metal slabs shown in Figure have the same resistance.  (a) 1 SQ. BLOCK $R = R_s\left(\frac{\ell}{w}\right)$ ohms (b) 4 SQ. BLOCKS $R = R_s\left(\frac{4\ell}{4w}\right)$ $= R_s\left(\frac{\ell}{w}\right)$ ohms
6 b.	Explain the various capacitances in MOS transistor.
	Capacitance Estimation – The total load capacitance on the output of a CMOS gate is the sum of • gate capacitance (of other inputs connected to the output of the logic gate) • diffusion capactance (of the drain regions connected to the output) • routing capacitance (of connections between the output and other inputs)

MOS Device capacitances.

- Figure diagramatic representation of the parasistic capacitance fo an MOS transistor. It is assumed that the overlap of the gate over source/drain is equal to zero.
- The following capacitance components exist:
  - C_{gs}, C_{gd} = gate to channel capacitances, lumped at the source and the drain regions of the channel, respectively.
  - C_{sb}, C_{db} = source and drain-diffusion capacitance to bulk (or substrate).
  - C_{gb} = gate to bulk capacitance.



- Figure shows a circuit model comprising parasitic copacitances and the transistor. The total gate capacitance is given by $C_g = C_{gb} + C_{gs} + C_{gd}$.



6 c. Estimate the total capacitance for the structure as shown in below Fig.Q6(c).

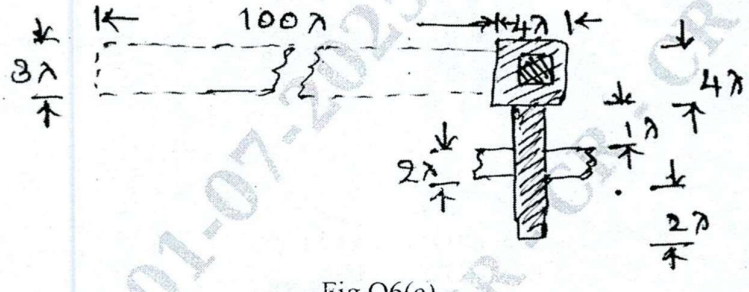


Fig.Q6(c)

metal; $C_{mf} = [3\lambda * 100\lambda]0.3 * 10^{-4} = 0.036pF$

poly; $C_p = [(4\lambda * 4\lambda) + (\lambda + 2\lambda) * 2\lambda]0.6 * 10^{-4} = 0.0053pF$

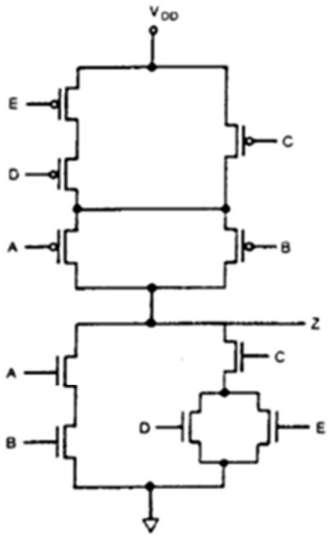
gate; $C_g = [2\lambda * 2\lambda]5.0 * 10^{-4} = 0.008pF.$

Therefore the total capacitance is

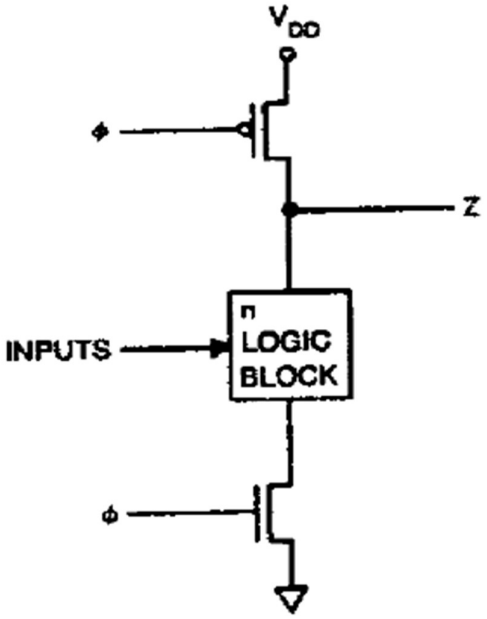
$$C_T = C_{mf} + C_p + C_g$$
$$\approx 0.049pF.$$

7 a.	Differentiate static and dynamic CMOS circuit with relevant diagrams.

Static CMOS logic offers simplicity, low static power consumption, and high noise immunity, but is slower and uses more transistors. Dynamic CMOS logic, while requiring precharging and clock synchronization, provides higher speed, lower dynamic power consumption, smaller transistor count, and reduced area, but suffers from increased susceptibility to noise and charge leakage. Dynamic logic is often necessary for very high-frequency designs, while static logic is preferred for applications where power efficiency and reliability are paramount.



Structure of Static CMOS



Structure of Dynamic CMOS

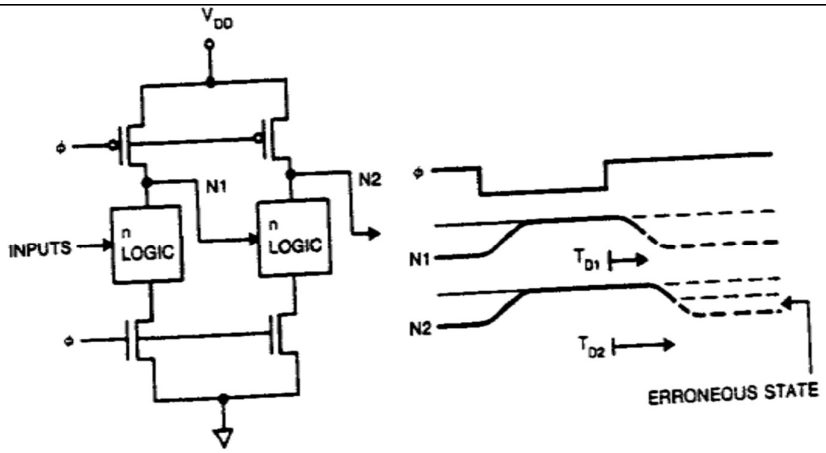
7 b.	Explain the percharge and evaluate phase in dynamic logic.

Operation Phases

The dynamic CMOS gate operates in two main phases, controlled by the clock signal ϕ:

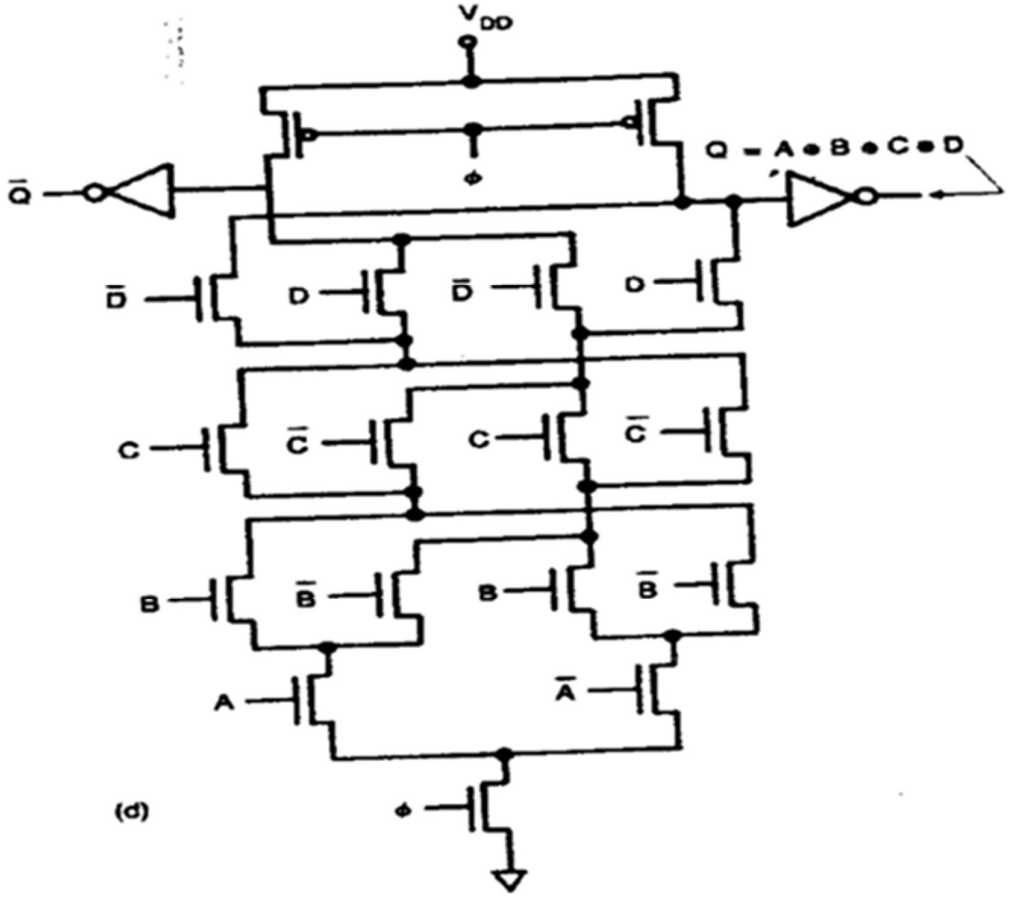
1. **Precharge Phase** ($\phi = 0$)
   - The pMOS precharge transistor turns ON, charging the output node to V_{DD}.
   - The nMOS evaluation transistor is OFF, preventing any discharge.
   - The output is temporarily set to HIGH regardless of input values.
2. **Evaluation Phase** ($\phi = 1$)
   - The pMOS precharge transistor turns OFF.
   - The nMOS evaluation transistor turns ON, allowing the nMOS logic block to evaluate the function.
   - If the input logic network forms a conducting path to ground, the output discharges to LOW.
   - If no conducting path exists, the output remains at its precharged HIGH state.

This approach reduces the number of transistors needed, since a pull-up network is not required.

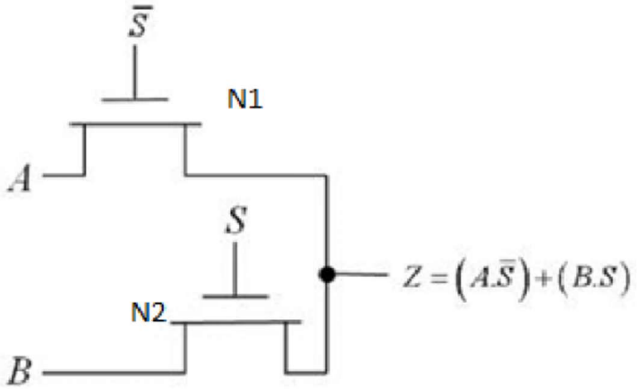


7 c. Design a CVSL (Cascade Voltage Switch Logic) based XOR gate.

4-input CVSL XOR gate



8 a. **Design a 2 : 1 multiplexer using pass transistor logic.**



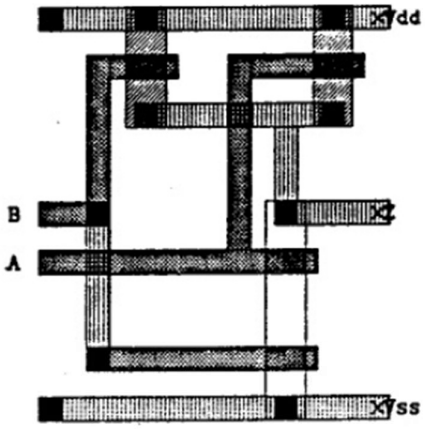
S-select line	Outputs
0	A
1	B

8 b. **Draw and explain the layout diagram of a 2 input NAND gate.**

NAND Gate Layout

Basic Layout Translation

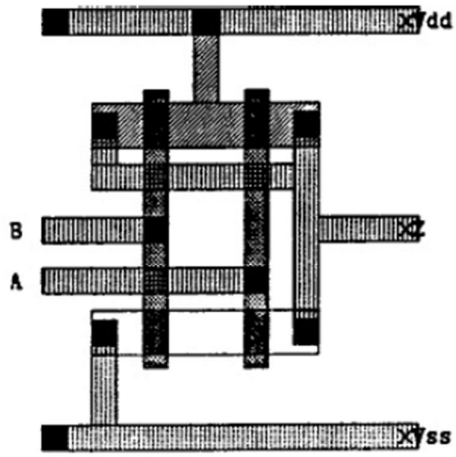
- A 2-input NAND gate can be implemented using a combination of series nMOS transistors and parallel pMOS transistors.
- Figure below represents the direct translation of schematic into layout of a 2-input NAND gate.



Basic layout translation of a 2-input NAND gate

Horizontal Transistor Orientation

- By orienting the transistors horizontally, we obtain the layout shown in figure below, which is cleaner and more compact.



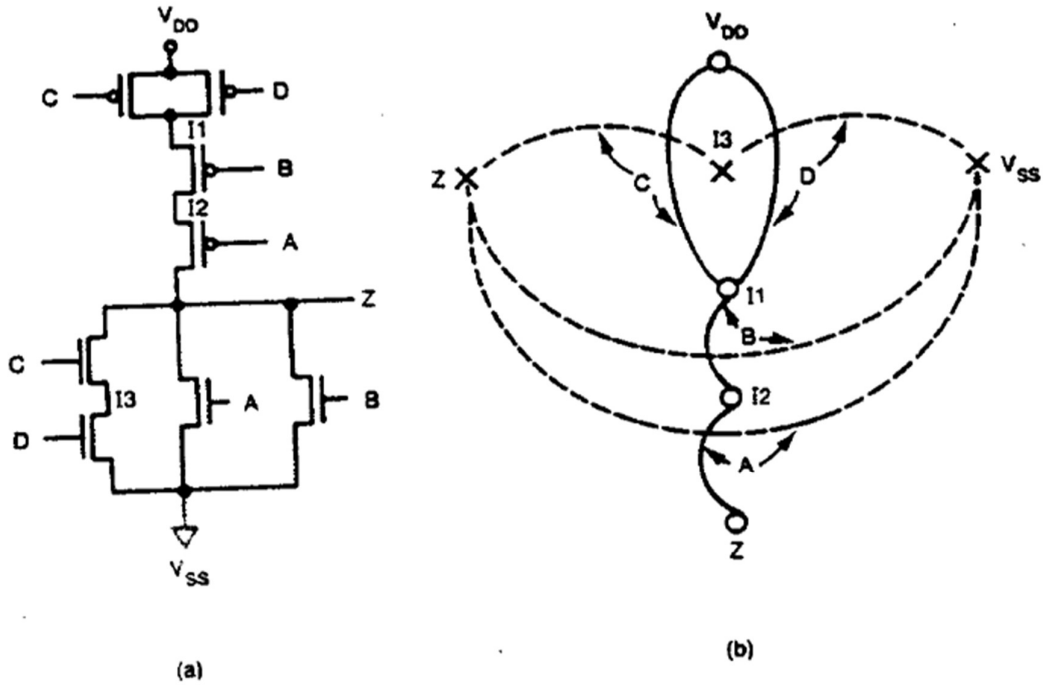
Optimized layout for NAND Gate

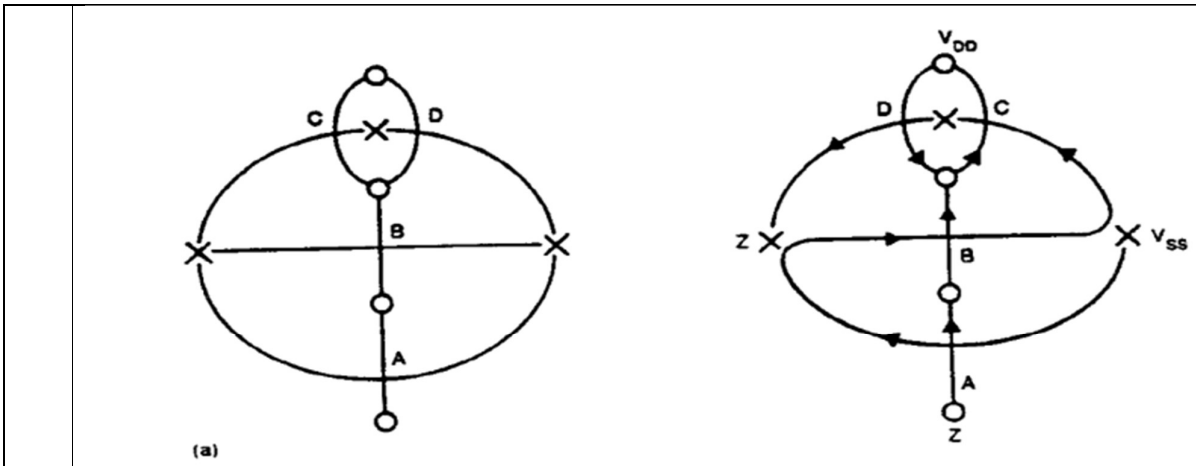
Design Style

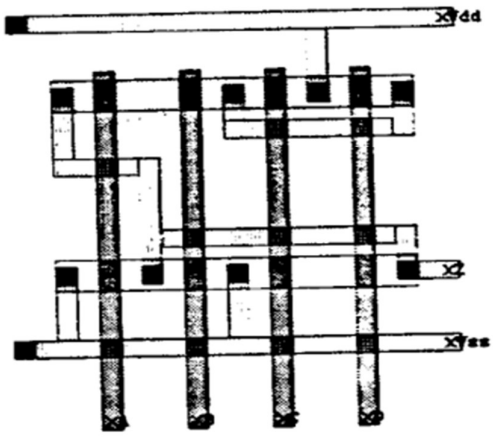
For multiple-input static gates, the following layout style is adopted:

- Transistors are oriented horizontally.
- Polysilicon gate signals run vertically.
- In cases where deviations from this style occur, specific design reasons will be provided.
- The NAND gate could be rotated by 90° to have vertical metal and horizontal polysilicon connections.

8 c. Design a schematic and layout for $Z = \overline{(A + B + CD)}$ using Euler's graph.



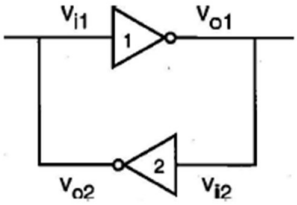

C
D
B
A
(a)
V_{DD}
D
C
Z
B
V_{SS}
A
Z


Vdd
Z
Vss
(b)

9 a.	With appropriate neat diagram of two inverter bistable element, explain in detail the voltage transfer characteristics (VTC) and potential energy analogy.

Cross-Coupled Inverter

Two inverters are connected in a feedback loop as shown in figure below.



Cross-Coupled Inverter

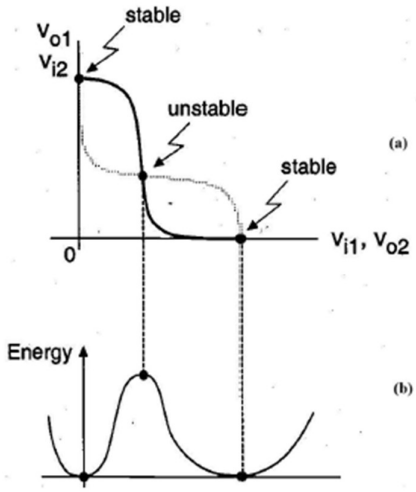
In this configuration:

- Output of Inverter 1 is connected to the input of Inverter 2
- Output of Inverter 2 is connected to the input of Inverter 1

Thus, we have:

$$v_{O1} = v_{I2}, \quad v_{O2} = v_{I1}$$

2.1.1 Voltage Transfer Characteristics (VTC)



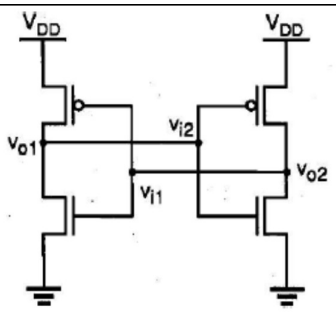
(a) VTC of Cross - Coupled Inverter; (b) Potential energy landscape

The voltage transfer curves (VTC) of both inverters can be plotted on the same graph as sown in above figure(a). The intersection points indicate possible operating points of the circuit.

- There are **three intersection points**
- Two of them are **stable**
- One is **unstable**

Stability analysis:

- At stable points: inverter gain $< 1 \Rightarrow$ small disturbances decay.
- At the unstable point: inverter gain $> 1 \Rightarrow$ disturbances are amplified.

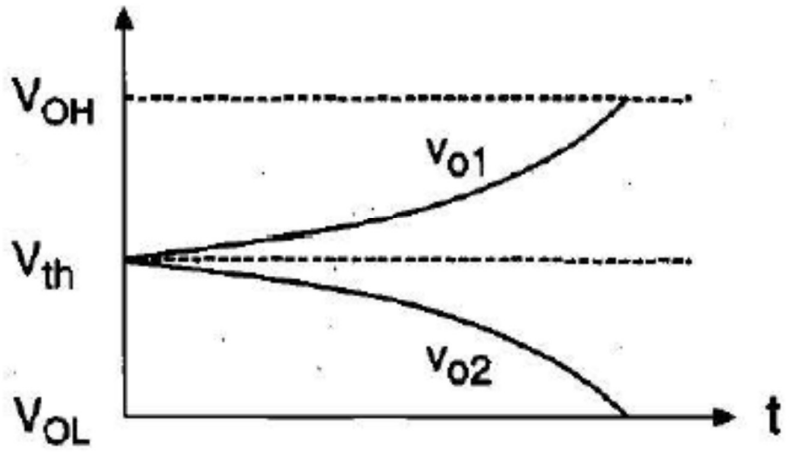


The bistable nature of a cross-coupled inverter circuit can be understood not only through voltage transfer characteristics but also through a qualitative analysis of the total potential energy levels at different operating points refer figure (b).

- The circuit exhibits three possible operating points:
  - Two **stable** operating points
  - One **unstable** operating point
- At the two stable points, the **total potential energy** is at a **minimum**. This occurs when the **voltage gains** of both inverters are approximately zero.
- At the intermediate operating point, the **potential energy is at a maximum**. Here, both inverters exhibit **maximum voltage gain**, making the system highly sensitive to small perturbations.
- A small disturbance at the unstable point causes the system to transition into one of the two stable states.

If the circuit is initialized exactly at the unstable point, any small **voltage perturbation** or **noise** will move the system away from it. Due to the **positive feedback**:

- The small disturbance gets amplified.
- The outputs of the inverters **diverge rapidly**.
- The system settles in one of two stable states (refer the figure shown below):
  - One output reaches **VOH** (logic high).
  - The other output reaches **VOL** (logic low).



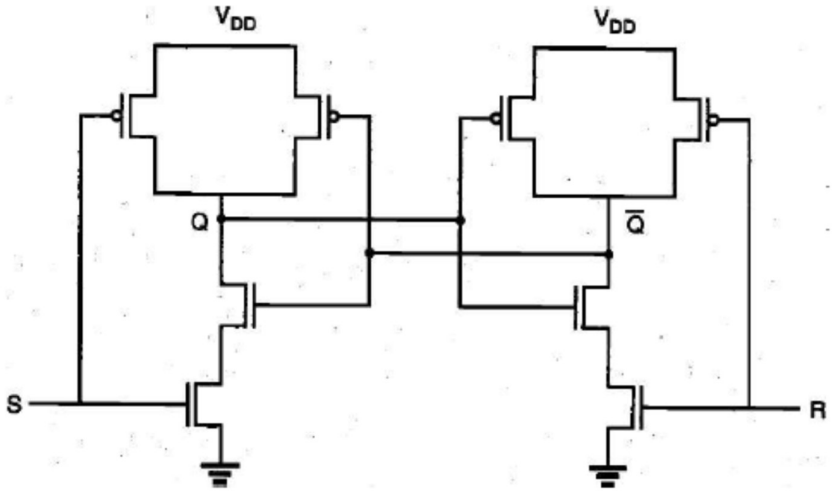
9 b.	Explain the operation of SR latch using CMOS NAND2 gates and switch level diagram.

To enable external control and allow a change of state, additional switching elements (inputs) must be added. The resulting circuit is a CMOS SR Latch (see figure below), which includes:

- S (Set) input
- R (Reset) input

This circuit is often referred to as an SR flip-flop, as it can toggle between two stable states.

The CMOS NAND - based SR latch is shown in figure below.



- It uses two NAND2 gates with cross-coupled feedback
- Inputs: S, R (active-low)
- Outputs: Q, $\overline{Q}$

NAND SR Latch Behavior

1. Set State:

- $S = 0,\ R = 1$
- $\Rightarrow Q = 1,\ \overline{Q} = 0$

2. Reset State:

- $S = 1,\ R = 0$
- $\Rightarrow Q = 0,\ \overline{Q} = 1$

3. **Hold State:**

- $S = 1,\ R = 1$
- $\Rightarrow$ Previous state is held

4. **Invalid State:**

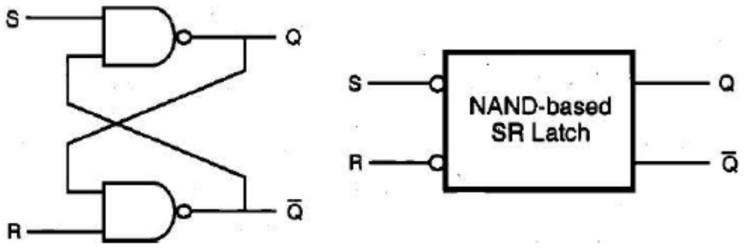
- $S = 0,\ R = 0$
- $\Rightarrow Q = \overline{Q} = 1$ (invalid)

The truth table is shown below:

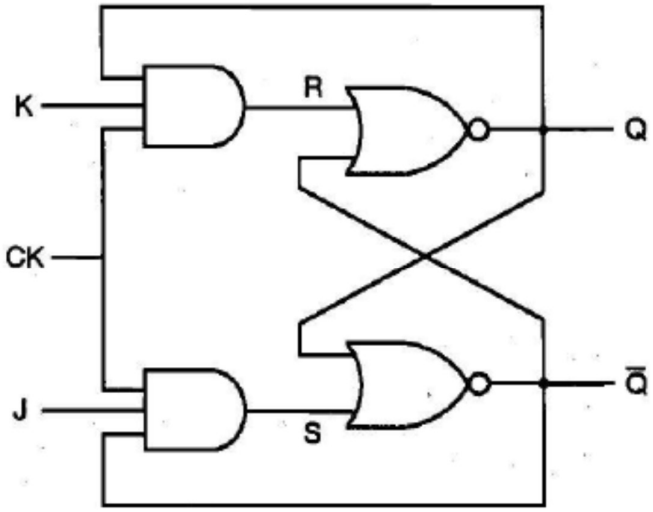
Table 4: Truth table of NAND - based SR latch

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
1	1	Q_n	$\overline{Q}_n$	Hold (no change)
0	1	1	0	Set
1	0	0	1	Reset
0	0	1	1	Not Allowed

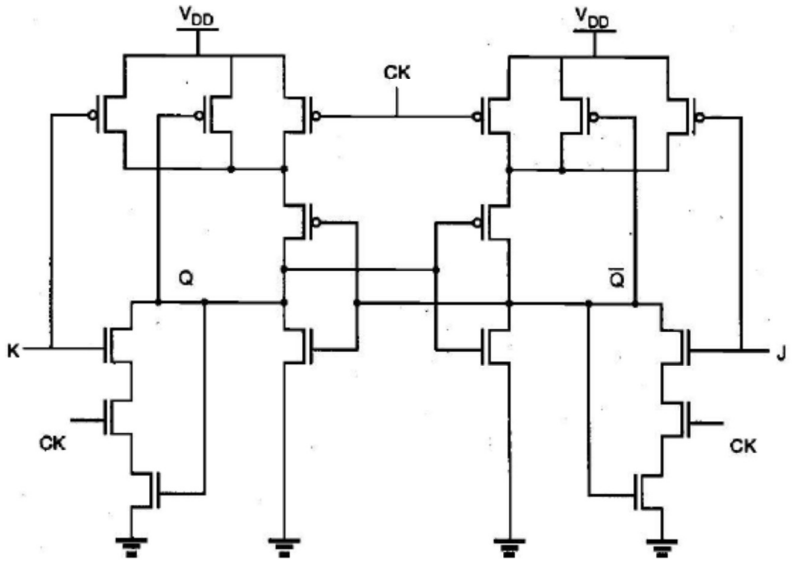
The gate-level schematic and the corresponding block diagram representation of the NAND-based SR latch circuit are shown in figure below:



9 c.	With neat appropriate diagrams, explain the clocked JK – Latch using NOR2 gates.



- This version, as opposed to the all-NAND realization, presents the following advantages:
  - The circuit employs a **CMOS realization** with an **AOI (AND-OR-Invert)** structure.
  - The AOI-based design results in a **lower transistor count**.
  - Consequently, the circuit becomes **more compact and efficient**.
- The AOI realization of JK latch is shown in figure below:



- This implementation is especially favorable in VLSI designs where area and power efficiency are critical.

10 a.	What is structured design strategy? Explain the factors modularity, regularity and locality.

A primary aim of the Mead and Conway text was to allow system designers the option of implementing high performance systems directly in silicon. From this point of view, it is imperative that the complexity of designing an IC or complete system be reduced. After all, if teams of expert industrial designers take man-years to finish chip designs, why should one expect a team of nonexperts to perform any better? Methods of dealing with complex design problems have been developed for large software problems. By adapting (or readapting) these to the IC design environment, we can not only formulate methods to deal with the apparent complexity of the IC design process to a novice, but also propose methods by which experts can cope with the ever increasing complexity of designing circuits with millions of devices.

Modularity

Hierarchy involves dividing a system into a set of submodules. If these modules are "well formed" the interaction with other modules can be well characterized. The notion of "well formed" may differ from situation to situation but a good starting point are those criteria placed on a "well formed" software subroutine. First of all, a well defined interface is required. This is an argument list with variable types in the software case. In the IC case this corresponds to a well defined physical interface that indicates the position, name, layer type, size, and signal type of external interconnections.

6.2.2.3 Regularity

The use of iteration to form arrays of identical cells is an example of the use of regularity in an IC design. However, extended use may be made of regular structures to simplify the design process. For instance, if one was constructing a "data-path," the interface between modules (power, ground, clocks, busses) might be common but the internal details of modules may differ according to function. Regularity can exist at all levels of the design hierarchy. At the circuit level, uniform transistors might be used rather than the manual optimization of each device. At the logic module level, identical gate structures might be employed. At higher levels, one might construct architectures that use a number of identical processor structures.

Locality

By defining well-characterized interfaces for a module, we are effectively stating that the other internals of the module are unimportant to any exterior interface. In this way we are performing a form of "information hiding" that reduces the apparent complexity of that module. In the software world this is paralleled by the reduction of global variables to a minimum (hopefully to zero). Using this model, for instance, we would not physically overlay connections to a physical module, as this may modify the internal structure and operation of a previously defined module.

10 b. Distinguish self-test and built-in test with examples.

A "self-test" is a broad concept of a device testing itself, while a Built-In Self-Test (BIST) is a specific engineering methodology where a device's hardware and software are intentionally designed to perform tests internally, reducing reliance on external test equipment and significantly improving fault coverage for complex integrated circuits (ICs). BIST is a design-for-test (DFT) technique that embeds a test pattern generator and response analyzer within the chip to detect internal failures, making it cost-effective for complex designs and enhancing system reliability.

One method of incorporating a built-in test module is to use signature analysis or cyclic redundancy checking. This involves the use of a linear feedback shift register shown in Fig. 6.19. After initialization, the value in the register will be a function of the value and number of latch inputs and the counting function of the signature analyzer. A good part will have a particular number or signature in the register. A bad part will have a different number in the register. Signature analysis can be merged with the LSSD technique to create a structure known as BILBO — for Built-In Logic Block Observation [KoMZ79]. This is outlined in Fig. 6.20.

A 3-bit register is shown with the associated circuitry. In mode A ($C_0 = C_1 = 1$), the registers act as conventional parallel registers. In mode B ($C_0 = C_1 = 0$), the registers act as scan registers. In mode C ($C_0 = 1$ $C_1 = 0$), the registers act as a signature analyzer or pseudo-random sequence generator (PRSG). The registers are reset if $C_0 = 0$ and $C_1 = 1$. Thus a complete test generation and observation arrangement can be implemented as shown in Fig. 6.21. In this case two sets of registers have been added in addition to some random logic to effect the test structure.

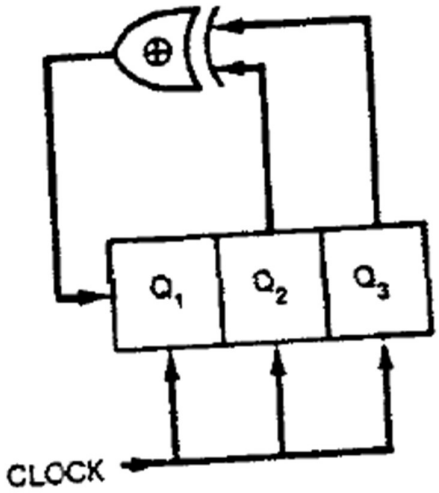
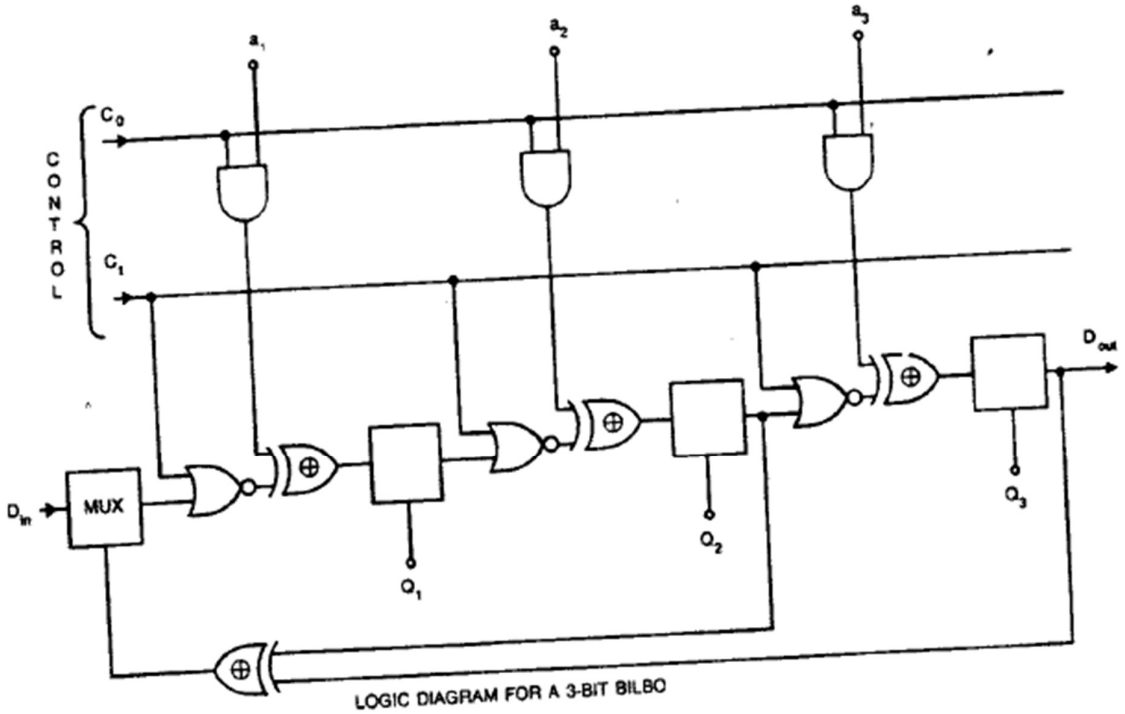


FIGURE 6.19. A linear feedback shift register



LOGIC DIAGRAM FOR A 3-BIT BILBO

10 c. Explain with neat diagram, Gate Array Design flow.

A typical flowchart used in the IGC-20000D gate array product is shown in Fig. The customer is responsible for creating a logic schematic and a set of test vectors, which are used initially to verify the customer's logic. This logic schematic is then converted to CMOS gate-array macros After

simulation, the CMOS cells are placed on the appropriate array and automatically routed. Any necessary revisions are communicated to the customer and this procedure is repeated until an acceptable CMOS implementation is found. Final placement and routing precedes a final simulation with all parasitics. The array is then manufactured and tested with a customer-generated test vector set.