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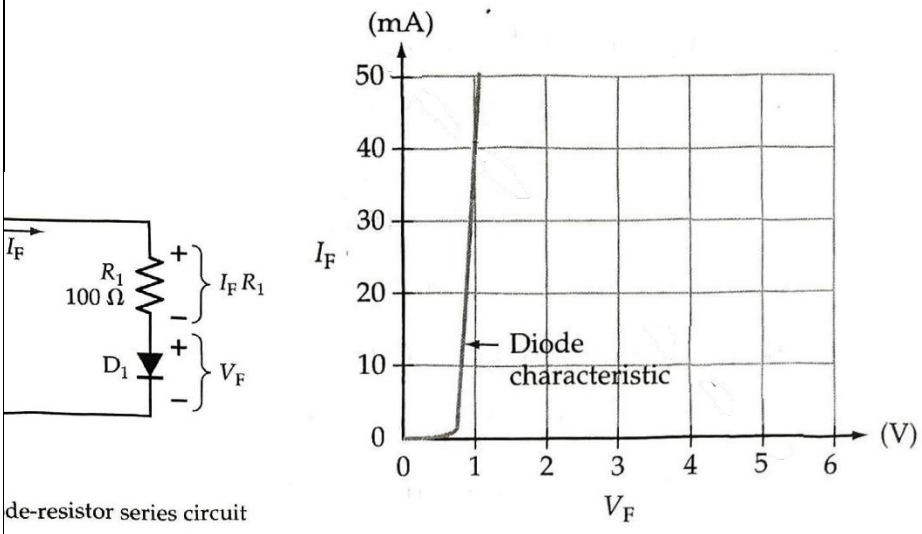
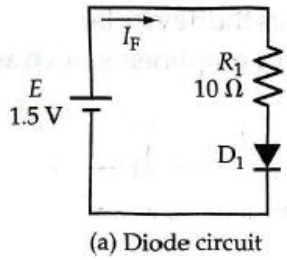
Internal Assessment Test 1 – May 2025

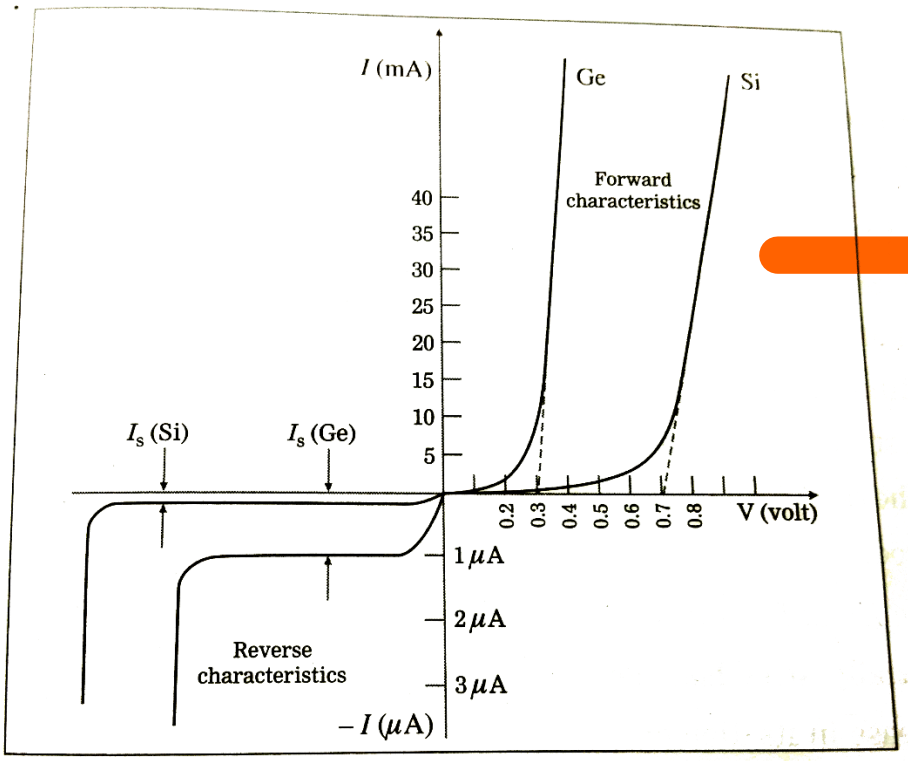
Sub:	Basic Electronics					Code:	BBEE203	Branch	EC
Date:	06/05/2025	Duration:	90 min's	Max Marks:	50	Sem/Sec:	2nd Sem (Secs: M,N,O,P)		OBE

	Answer any FIVE FULL Questions	Marks	CO	RBT
1.	a. Explain the forward and reverse characteristics of a silicon diode and germanium diode. b. Draw the dc load line for the circuit in Fig. on the diode forward characteristic and plot the position of Q-Point.  de-resistor series circuit	5+5	CO1	L3
2.	a. Calculate I_F for the diode circuit in Fig. assuming that the diode has $V_F = 0.7$ V and $r_d = 0$. Then recalculate the current taking $r_d = 0.25\Omega$.  (a) Diode circuit b. Write short notes on Half wave rectifier with circuit diagrams and waveforms	6+4	CO1	L2
3.	a) Discuss the working of the Bridge rectifier with neat circuit diagrams.	7+3	CO1	L3

	b) Determine the peak output voltage and current for a bridge rectifier circuit when the secondary RMS voltage is 30V, R_L=300Ω and the diode forward drop is 0.7V.			
4.	Illustrate RC-π filter in detail.	10	CO1	L2
5. a) b)	Perform subtraction using 2's complement (i) (51)10-(24)10 (ii) (11011)2 - (11101)2 Perform subtraction using 1's complement (i) (79)10-(246)10 (ii) (11011)2 - (11101)2	06 + 04	CO3	L3
6.	a. Build the equation Y=AB+CD+E to realize using NAND Gates b. Express the Boolean expression F=X'Y+XZ'+(X+Y+Z')' using • Sum of Minterms (SOP) • Product of Maxterms (POS)	4+6	CO3	L3
7.	Design a full adder and implement using basic logic gates.	10	CO3	L3
8.	State and prove De Morgan's Law for a function of three variables.	10	CO3	L2
9.	A 5V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5V to a load having a resistance of 500 Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9V.	10	CO1	L3

Solution and Scheme of IAT-1 for Basic Electronics

a) Explain the forward and reverse characteristics of a silicon diode and germanium diode.



3 Marks

Junction diode characteristics, Ge and Si

Solution:

2 Marks

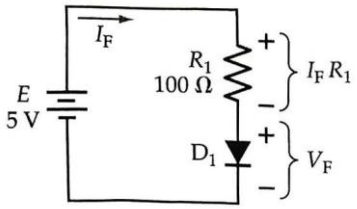
PN- Junction diode characteristics, Ge and Si Explanation:

(1) Forward bias characteristics : There is forward current only after the barrier potential of the pn-junction is overcome. Then there is an exponential rise in the current beyond the knee region. The forward - bias voltage required to reach the region of upward swing is called the threshold voltage VT or cut in voltage. When rounded off to the nearest , the threshold voltage is 0.3 V for a germanium diode and 0.7 V for a silicon diode.

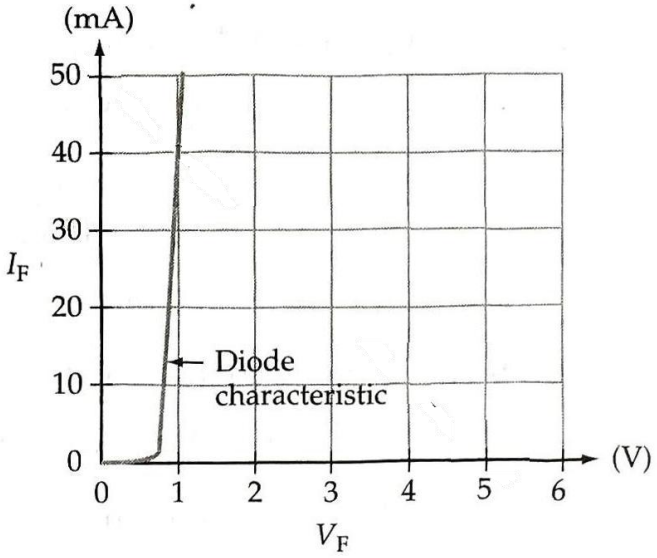
(2) Reverse bias characteristics : In the reverse bias, the potential barrier at the junction is large and the current due to majority carriers in each region is zero. However, minority charge carriers are able to cross the junction and constitute a very small current in the reverse direction. This reverse current quickly reaches its maximum or saturation value and remains fairly constant with increase in the reverse - bias voltage. It is called the reverse saturation current Is, which is typically a few nanoamperes for a silicon diode and a few microamperes for a germanium diode. Too high a negative voltage results in a sharp change in the reverse - bias characteristics. At a certain characteristic negative voltage, called the peak inverse voltage (PIV) or

breakdown voltage, the current in the reverse direction increases very rapidly. In general, a silicon diode has a higher PIV rating (~1000V) than a germanium diode (~400V).

b) Draw the dc load line for the circuit in Fig. on the diode forward characteristic and plot the position of Q-Point.



(a) Diode-resistor series circuit



Solution

Substitute $I_F = 0$ into $E = (I_F R_1) + V_F$ (2-3)

$$E = (I_F R_1) + V_F = 0 + V_F$$

or $$V_F = E = 5\text{ V}$$

1 Marks

Plot point A on the diode characteristic at

$$I_F = 0 \text{ and } V_F = 5\text{ V}$$

Now substitute $V_F = 0$ into Eq. 2-3,

$$E = (I_F R_1) + 0$$

giving $$I_F = \frac{E}{R_1} = \frac{5\text{ V}}{100\ \Omega}$$

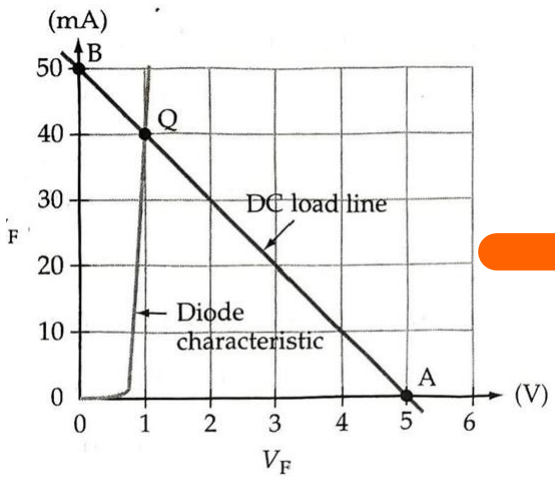
$$= 50\text{ mA}$$

2 Marks

Plot point B on the diode characteristic at

$$I_F = 50\text{ mA} \text{ and } V_F = 0$$

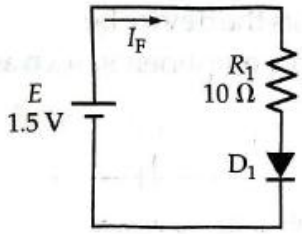
Draw the dc load line through points A and B.



(b) Plotting the dc load line on the diode characteristics

2 Marks , Q (1V,40mA)

2



(a) Diode circuit

a) Calculate I_F for the diode circuit in Fig. assuming that the diode has $V_F = 0.7$ V and $r_d = 0$. Then recalculate the current taking $r_d = 0.25\Omega$.

Solution

Substituting V_F as the diode equivalent circuit (Fig. 2-12b),

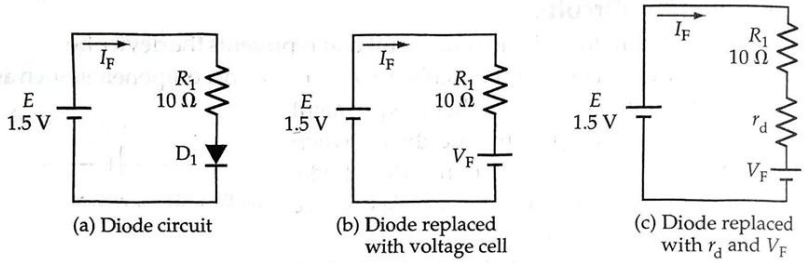
$$I_F = \frac{E - V_F}{R_1} = \frac{1.5\text{ V} - 0.7\text{ V}}{10\ \Omega}$$
$$= 80\text{ mA}$$

2 Marks

Substituting V_F and r_d as the diode equivalent circuit (Fig. 2-12c),

$$I_F = \frac{E - V_F}{R_1 + r_d} = \frac{1.5\text{ V} - 0.7\text{ V}}{10\ \Omega + 0.25\ \Omega}$$
$$= 78\text{ mA}$$

3 Marks

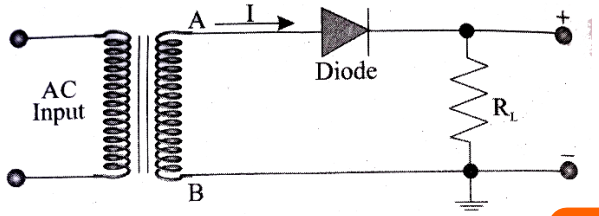


(a) Diode circuit (b) Diode replaced with voltage cell (c) Diode replaced with r_d and V_F

Figure 2-12 Diode circuits for Ex. 2-5.

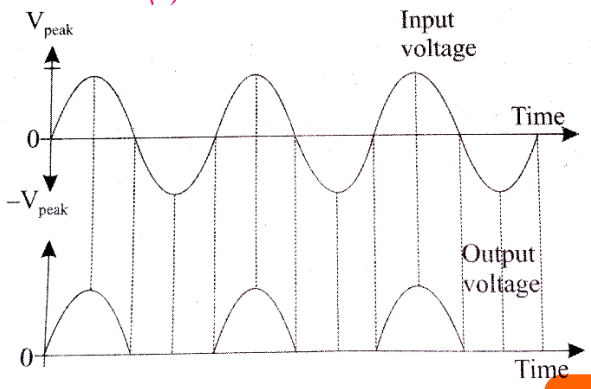
b) Write short notes on Half wave rectifier with circuit diagrams and waveforms

Solution: Rectification is the process of converting alternating current into direct current is called rectification. In half wave rectifier circuit , either a positive half of the negative half of the AC input is passed through while the other half is blocked . Only one half of the input wave reaches the output . A p-n junction can be used as half wave rectifier .



(a) Half wave rectifier circuit

2 Marks



(b) input and output waveforms

2 Marks

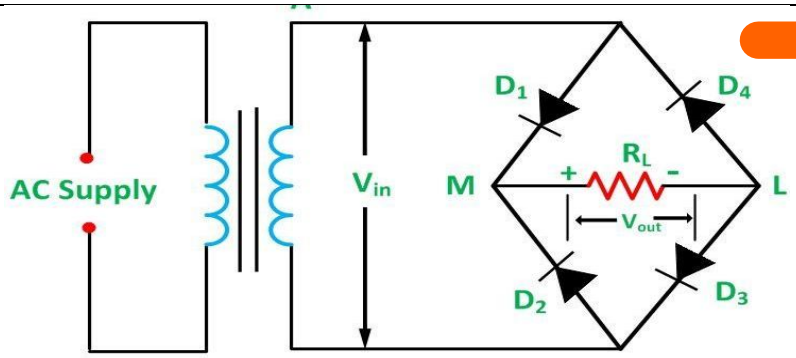
When the positive half cycle of the AC input signal passes through the circuit , terminal A become positive with respect to terminal B. The diode is forward biased and hence it conducts. The current flows through the load resistance RL and AC voltage developed across RL constitutes the output voltage V0 and the wavelength of the diode is shown in the fig (b) When the negative half cycle of the AC input signal passes through the circuit , terminal a is negative with respect to terminal B . Now the diode is reverse biased and does not conduct and hence no current passes through RL . The reverse saturation current in a diode is negligible. Since there is no voltage drop across RL , the negative half cycle of AC supply is suppressed at the output . The output of the half wave rectifier is not a steady DC voltage but a pulsating wave . The efficient of half wave rectifier is 40.6% .

1 Marks

3

a) Discuss the working of the Bridge rectifier with neat circuit diagrams.

Solution: In Full Wave Bridge Rectifier, an ordinary transformer is used in place of a center-tapped transformer. The circuit forms a bridge connecting the four diodes D_1, D_2, D_3, and D_4. The circuit diagram of the Full Wave Bridge Rectifier is shown below.



2 Marks

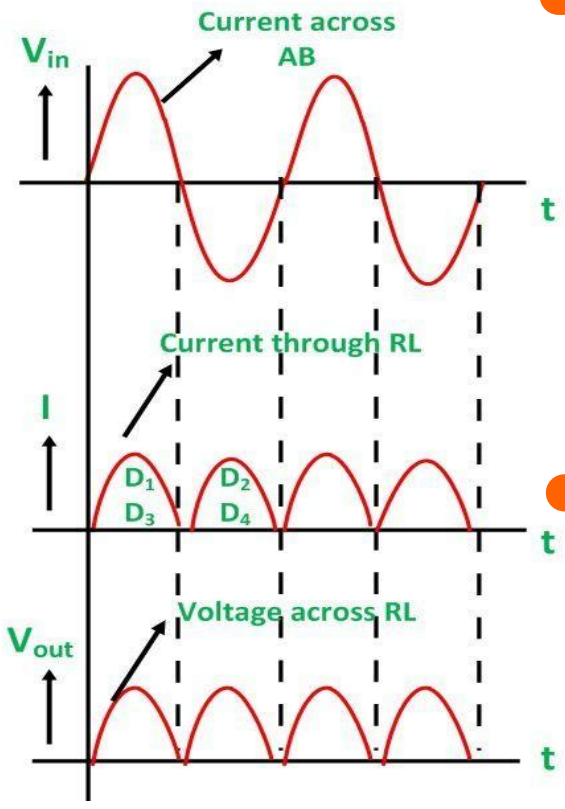
The AC supply which is to be rectified is applied diagonally to the opposite ends of the bridge. Whereas, the load resistor R_L is connected across the remaining two diagonals of the opposite ends of the bridge.

Operation of Full Wave Bridge Rectifier

1 Marks

When an AC supply is switched ON, the alternating voltage V_{in} appears across the terminals AB of the secondary winding of the transformer which needs rectification. During the positive half cycle of the secondary voltage, end A becomes positive, and end B becomes negative as shown in the figure below.

The diodes D_1 and D_3 are forward biased and the diodes D_2 and D_4 are reversed biased. Therefore, diode D_1 and D_3 conduct, and diode D_2 and D_4 do not conduct. The current (i) flows through diode D_1, load resistor R_L (from M to L), diode D_3, and the transformer secondary. The waveform of the full-wave bridge rectifier is shown below.



1 Marks

1 Marks

b) Determine the peak output voltage and current for a bridge rectifier circuit when the secondary RMS voltage is 30V, R_L=300Ω and the diode forward drop is 0.7V.

To determine the **peak output voltage** and **peak output current** for a **bridge rectifier** with the following specifications:

- Secondary RMS Voltage, $V_{\text{RMS}} = 30\ \text{V}$
- Load Resistance, $R_L = 300\ \Omega$
- Diode Forward Voltage Drop (each diode), $V_D = 0.7\ \text{V}$

Step 1: Convert RMS to Peak Voltage

For a sinusoidal AC voltage:

$$V_{\text{peak}} = V_{\text{RMS}} \times \sqrt{2} = 30 \times 1.414 = 42.43\ \text{V}$$

1 Marks

Step 2: Account for Diode Drops

In a **bridge rectifier**, **two diodes** conduct in each half-cycle. So, the total forward voltage drop is:

$$V_{\text{drop}} = 2 \times 0.7 = 1.4\ \text{V}$$

2 Marks

Step 3: Calculate Peak Output Voltage

$$V_{\text{out, peak}} = V_{\text{peak}} - V_{\text{drop}} = 42.43 - 1.4 = 41.03\ \text{V}$$

Step 4: Calculate Peak Output Current

2 Marks

$$I_{\text{peak}} = \frac{V_{\text{out, peak}}}{R_L} = \frac{41.03}{300} \approx 0.1368\ \text{A} = 136.8\ \text{mA}$$

4

Illustrate RC-π filter in detail.

Solution:

An RC-π filter is a low-pass filter commonly used in power supply circuits, particularly in voltage regulators and ripple filters. The name "π" comes from its topology, which resembles the Greek letter π. It uses resistors (R) and capacitors (C) in a specific configuration to reduce AC ripple and allow DC to pass through.

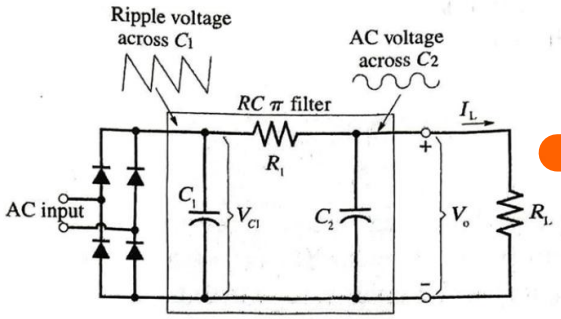
RC-π Filter Overview

An RC-π filter typically consists of:

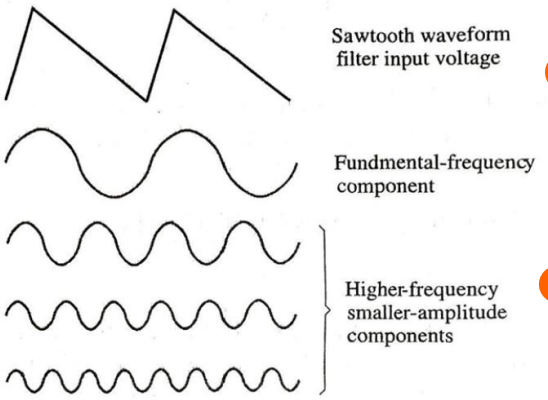
Two capacitors (C1 and C2) connected from the input and output lines to ground.

One resistor (R) in between the two capacitors and in series with the line.

It looks like this in a circuit diagram:



(a) *RC* π filter circuit



(b) The sawtooth waveform at the filter input consists of a fundamental-frequency component and a number of smaller-amplitude, higher-frequency harmonics

Figure 3-20 When a resistor and capacitor (R_1 and C_2) are connected as a voltage divider to a power supply reservoir capacitor (C_1), the combination is an *RC* π filter. The π filter attenuates the ac components that constitute the ripple voltage.

3 Marks

1 Marks

1 Marks

Working Principle

The first capacitor (C1) shunts high-frequency AC (like ripple) to ground.

The resistor (R) then limits the remaining AC component by forming an RC time constant with C1 and C2.

The second capacitor (C2) further filters any residual AC signal, providing a smoother DC at the output.

1 Marks

This cascade of shunting and series impedance effectively attenuates unwanted frequencies.

It determines how much high-frequency noise is filtered out.

1 Marks

Ripple Reduction:

The more the capacitance and resistance (within reasonable values), the greater the attenuation of ripple voltage.

2 Marks

Load Consideration:

Too large a resistor may reduce the DC output due to voltage drop, so it's a balance between filtering and

output voltage regulation.

Applications 1 Marks

Power supply filters (after rectifiers)

Audio equipment to eliminate high-frequency hum

Analog circuits needing clean DC power

5. a) **Perform subtraction using 2's complement**

(i) (51)10-(24)10 (ii) (11011)2 - (11101)2

1. Subtraction using 2's Complement

(i) $(51)_{10} - (24)_{10}$

Step 1: Convert to 8-bit binary

- $51_{10} = 00110011$
- $24_{10} = 00011000$

1 Marks

Step 2: 2's complement of 24

- Invert: 11100111
- Add 1: $11100111 + 1 = 11101000$

Step 3: Add to 51

1 Marks

$$00110011 + 11101000 = 10011011$$

This gives **a carry out** (since result is 9 bits), discard carry:

$$10011011 \Rightarrow \boxed{0011011} = 27_{10}$$

Correct Answer: $(51 - 24) = \boxed{27}$

0.5 Marks

(ii) $(11011)_2 - (11101)_2$

Let's align to 5-bit binary:

- $A = 11011$
- $B = 11101$

Step 1: 2's complement of $B = 11101$

- Invert: 00010
- Add 1: $00010 + 1 = 00011$

1 Marks

Step 2: Add to A**:**

$$11011 + 00011 = 11110$$

No carry-out → result is **negative**

1 Marks

Take 2's complement of result:

- Invert: 00001
- Add 1: 00010 → decimal 2

0.5 Marks

So, result = **−2**

Correct Answer: $(11011)_2 - (11101)_2 = \boxed{-2}$

b) **Perform subtraction using 1's complement**

(i) (79)10-(246)10 (ii) (11011)2 - (11101)2

(i) $(79)_{10} - (246)_{10}$

Use 8-bit binary:

- $79 = 01001111$
- $246 = 11110110$

Step 1: 1's complement of 246

- Invert: 00001001

Step 2: Add to 79

$$01001111 + 00001001 = 01011000$$

No carry → result is **negative**, take 1's complement of result:

- Invert $01011000 \rightarrow 10100111 = 167$

✅ **Correct Answer:** $(79 - 246) = \boxed{-167}$

1 Marks

1 Marks

0.5 Marks

(ii) $(11011)_2 - (11101)_2$

5-bit binary:

- $A = 11011$
- $B = 11101$

Step 1: 1's complement of B

- Invert $11101 \rightarrow 00010$

Step 2: Add to A:

$$11011 + 00010 = 11101$$

No carry → result is negative → take 1's complement:

- Invert $11101 \rightarrow 00010 = 2$

✅ **Correct Answer:** $(11011)_2 - (11101)_2 = \boxed{-2}$

1 Marks

1 Marks

0.5 Marks

6.

a) Build the equation Y=AB+CD+E to realize using NAND Gates

Solution

Given, F = AB + CD + E

To implement it with the minimum number of NAND gates

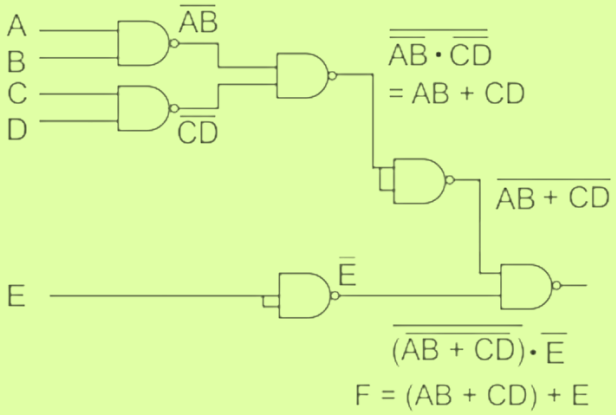
2 Marks

Concept

Bubbled input AND gate = NOR gate

Bubbled input OR gate = NAND gate

Let us observe the function implementation with help of 2-input NAND gates



3 Marks

We can observe that a minimum of 6 two-input NAND gates are required to implement the function

2 Marks

b) Express the Boolean expression F=X'Y+XZ'+(X+Y+Z')' using

- **Sum of Minterms (SOP)**
- **Product of Maxterms (POS)**

$$F = X'Y + XZ' + (X + Y + Z')'$$

in **Sum of Minterms (SOP)** and **Product of Maxterms (POS)** form.

- **Step 1: Apply De Morgan's Law**

$$(X + Y + Z')' = X'Y'Z$$

So:

$$F = X'Y + XZ' + X'Y'Z$$

1 Marks

- **Step 2: Expand all terms to 3-variable minterms**
- $X'Y = X'YZ + X'YZ'$
- $XZ' = XYZ' + XY'Z'$
- $X'Y'Z$ stays as is

So:

$$F = X'YZ + X'YZ' + XYZ' + XY'Z' + X'Y'Z$$

1 Marks

- **Step 3: List minterms (by binary indices of variables X Y Z):**
- $X'Y'Z \rightarrow$ m1
- $X'YZ' \rightarrow$ m2
- $X'YZ \rightarrow$ m3
- $XY'Z' \rightarrow$ m4
- $XYZ' \rightarrow$ m6

1 Marks

☑ **SOP Answer:**

$$F = \sum m(1, 2, 3, 4, 6)$$

☑ **POS Answer:**

Missing minterms: 0, 5, 7

$$F = \prod M(0, 5, 7)$$

2 Marks

☑ **Final Answer:**

- SOP: $\boxed{F = \sum m(1, 2, 3, 4, 6)}$
- POS: $\boxed{F = \prod M(0, 5, 7)}$

7.	**Design a full adder and implement using basic logic gates**
8.	**State and prove De Morgan's Law for a function of three variables.**

Input			Output	
A	B	C_in	Sum	C_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

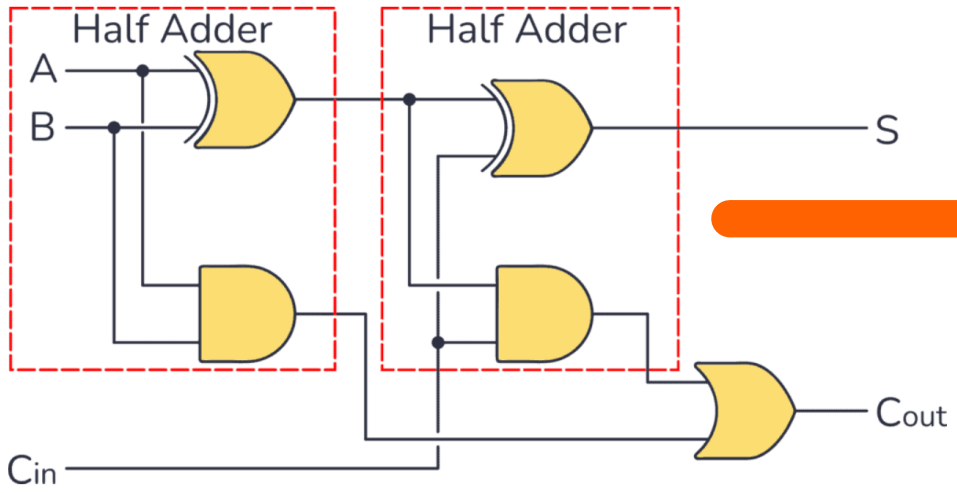
Solution:

3 Marks

$s = A \oplus B \oplus C_{in}$

$Cout = AB + AC_{in} + BC_{in}$

3 Marks



4 Marks

Solution:

De Morgan's Laws are fundamental rules in Boolean algebra and digital logic design. They express the relationship between the complement of logical operations (AND, OR) and can be extended to any number of variables.

2 Marks

De Morgan's Laws for Three Variables

Let A, B, and C be three Boolean variables. De Morgan's laws for three variables are:

1. **First Law:**

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

2. **Second Law:**

$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

2 Marks

*

Proof Using Truth Table

Let's prove both laws using a truth table.

A	B	C	$A \cdot B \cdot C$	$\overline{A \cdot B \cdot C}$	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{A} + \overline{B} + \overline{C}$	$A + B + C$	$\overline{A + B + C}$	$\overline{A} \cdot \overline{B} \cdot \overline{C}$
0	0	0	0	1	1	1	1	1	0	1	1
0	0	1	0	1	1	1	0	1	1	0	0
0	1	0	0	1	1	0	1	1	1	0	0
0	1	1	0	1	1	0	0	1	1	0	0
1	0	0	0	1	0	1	1	1	1	0	0
1	0	1	0	1	0	1	0	1	1	0	0
1	1	0	0	1	0	0	1	1	1	0	0
1	1	1	1	0	0	0	0	0	1	0	0

From the table, you can observe:

- Column 5 $\overline{A \cdot B \cdot C}$ = Column 9 $\overline{A} + \overline{B} + \overline{C}$
- Column 12 $\overline{A + B + C}$ = Column 13 $\overline{A} \cdot \overline{B} \cdot \overline{C}$

Hence, **De Morgan's Laws for three variables are proven true.**

6 Marks

9 **A 5V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5V to a load having a resistance of 500 Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9V.**

Step 1: RS (max)

At the threshold of regulation, all current from the source goes **only to the load**:

$$R_{S_{max}} = \frac{V_{in} - V_Z}{I_L} = \frac{4}{0.01} = 400\,\Omega$$

4 Marks

Step 2: RS (min)

As before (when all current goes to the zener):

$$R_{S_{min}} = \frac{V_{in} - V_Z}{I_{Zmax}} = \frac{4}{0.1} = 40\,\Omega$$

4 MArks

Step 3: RS (midpoint)

$$R_{S_{mid}} = \frac{R_{S_{min}} + R_{S_{max}}}{2} = \frac{40 + 400}{2} = \boxed{220\,\Omega}$$

2Marks