USN

CMRIT

Internal Assessment Test 2 – June 2025

Sub:	Basic Electronics					Code:	BBEE203	Branch	EC
Date:	19/06/2025	Duration:	90 min's	Max Marks:	50	Sem/Sec:	2nd Sem (Secs: M,N,O,P)	OBE	

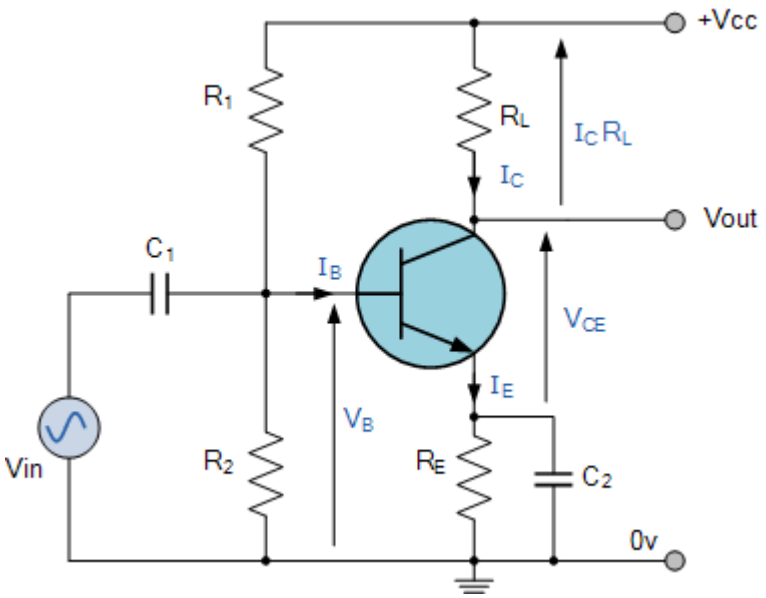
Answer any FIVE FULL Questions

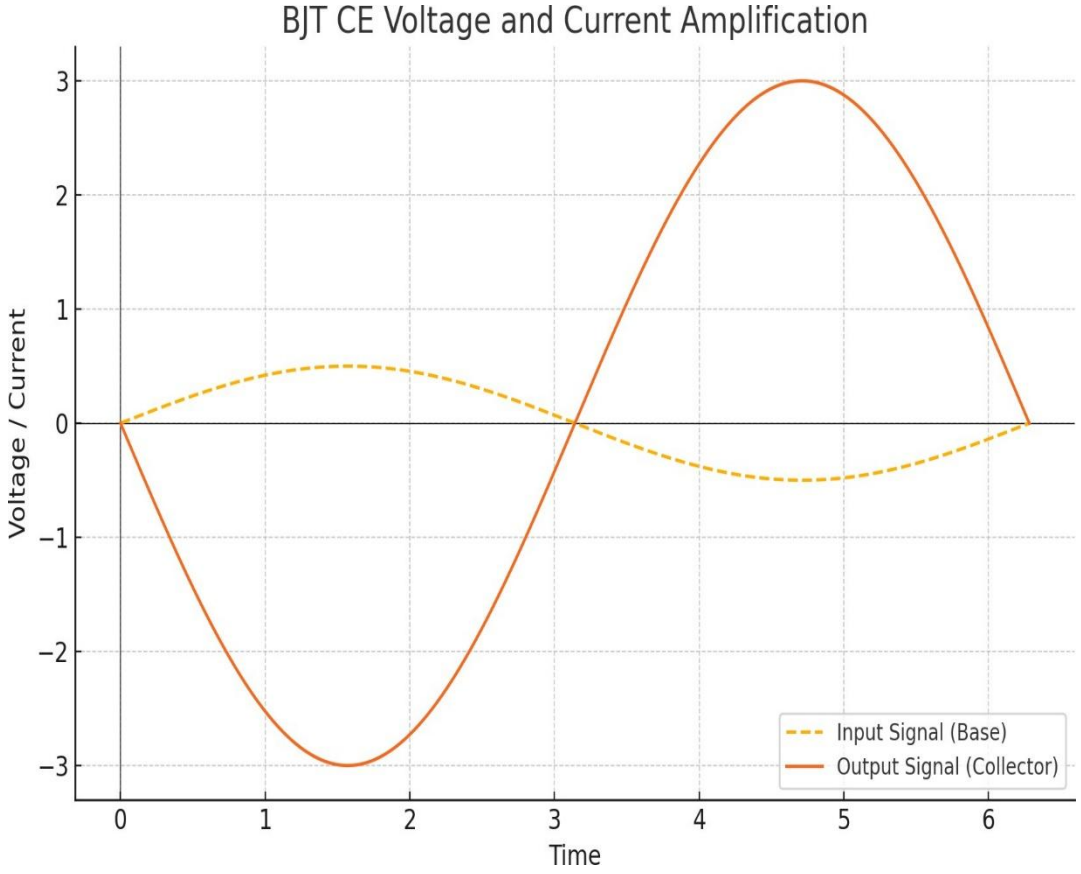
		Marks	CO	RBT
1.	Consider a BJT Common Emitter Circuit, Explain how Voltage amplification and Current Amplification are obtained.	10	CO2	L3
2.	Write a short note on 1. Enhancement type MOSFET. 2. Depletion type MOSFET	5+5	CO2	L2
3.	Explain the drain and transfer characteristics of n-channel JFET.	10	CO2	L2
4.	What is Strain Gauge? Explain the Construction of Unbounded strain Gauge.	10	CO5	L2
5.	Describe the procedure for drawing DC-Load Line on transistor CE output Characteristics.	10	CO2	L3
6	(i) Define the following with respect to Op-Amp: a. Input Offset Voltage b. Input Bias Current c. CMRR d. Slew Rate (ii) Define Op-Amp. Mention any 5 ideal characteristics of an Op-Amp.	5+5	CO3	L2
7	Draw the block diagram of Super heterodyne receiver and mention the function of each block.	10	CO5	L3
8	Describe the working of LVDT.	10	CO5	L2

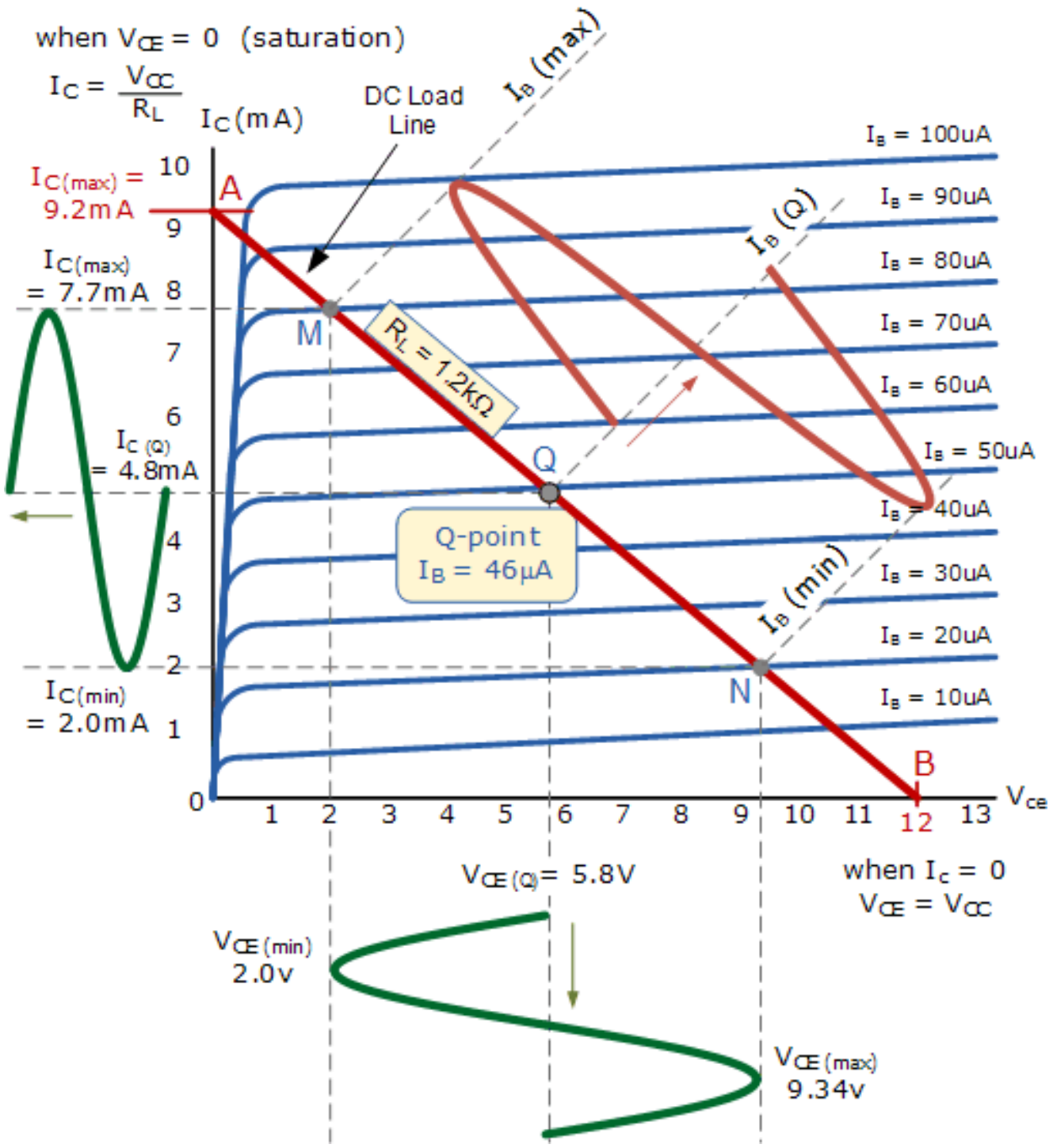
CI CCI HOD 12/6/2025

1. BJT Common Emitter: Voltage and Current Amplification

In a Common Emitter (CE) BJT configuration, small base current changes cause large collector current variations. Voltage amplification occurs because this large collector current flows through a high collector resistance (Rc), producing significant voltage gain across Rc. Current amplification is realized as the output current (Ic) is a multiple (beta times) of the base current (Ib).


+Vcc
R1
RL
IC RL
IC
Vout
C1
IB
VCE
IE
VB
Vin
R2
RE
C2
0v

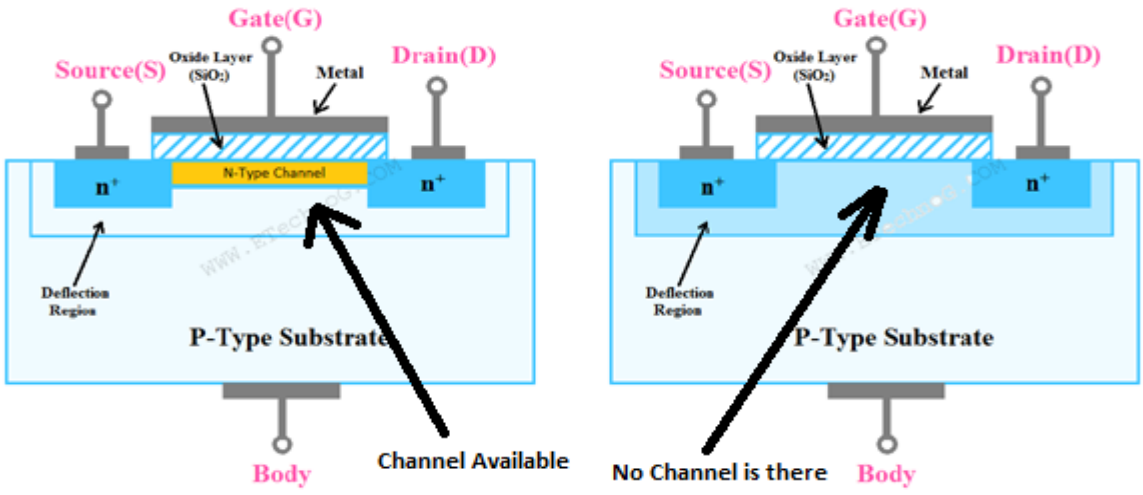

BJT CE Voltage and Current Amplification
Voltage / Current
Time
Input Signal (Base)
Output Signal (Collector)
3
2
1
0
−1
−2
−3
0
1
2
3
4
5
6



2. Depletion-type MOSFET and Enhancement-type MOSFET

Depletion-Type MOSFET: Normally ON at Vgs = 0V; applying a negative gate voltage reduces drain current by depleting carriers in the channel.

Enhancement-Type MOSFET: Normally OFF; a positive Vgs is required to induce a channel for conduction. Commonly used in digital logic and power applications.

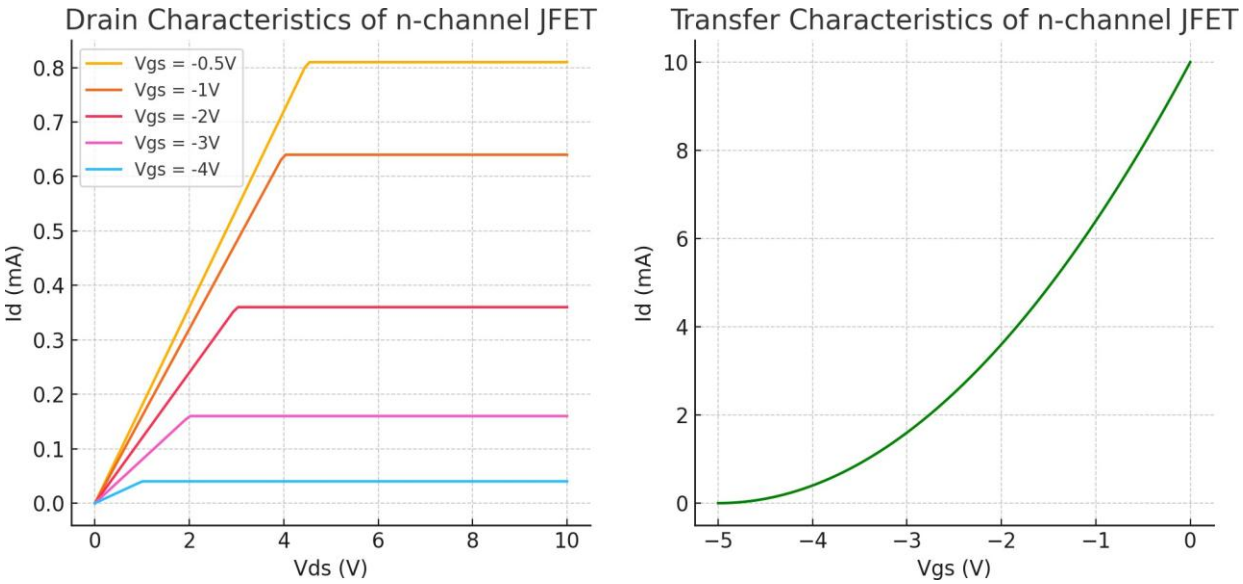


Depletion Type MOSFET **Enhancement Type MOSFET**

3. Drain and Transfer Characteristics of an n-channel JFET

The JFET operates by using a gate-source voltage to control the drain current. Drain characteristics: As Vds increases, Id increases and then saturates.

Transfer characteristics: Shows Id vs. Vgs; Id decreases parabolically with more negative Vgs.



4. Strain Gauge and Construction of an Unbounded Strain Gauge

A strain gauge measures the strain of a structure. When the structure deforms, the gauge stretches, changing its resistance. Unbounded strain gauges consist of wire elements connected between insulating materials. These gauges convert mechanical strain to electrical signals.

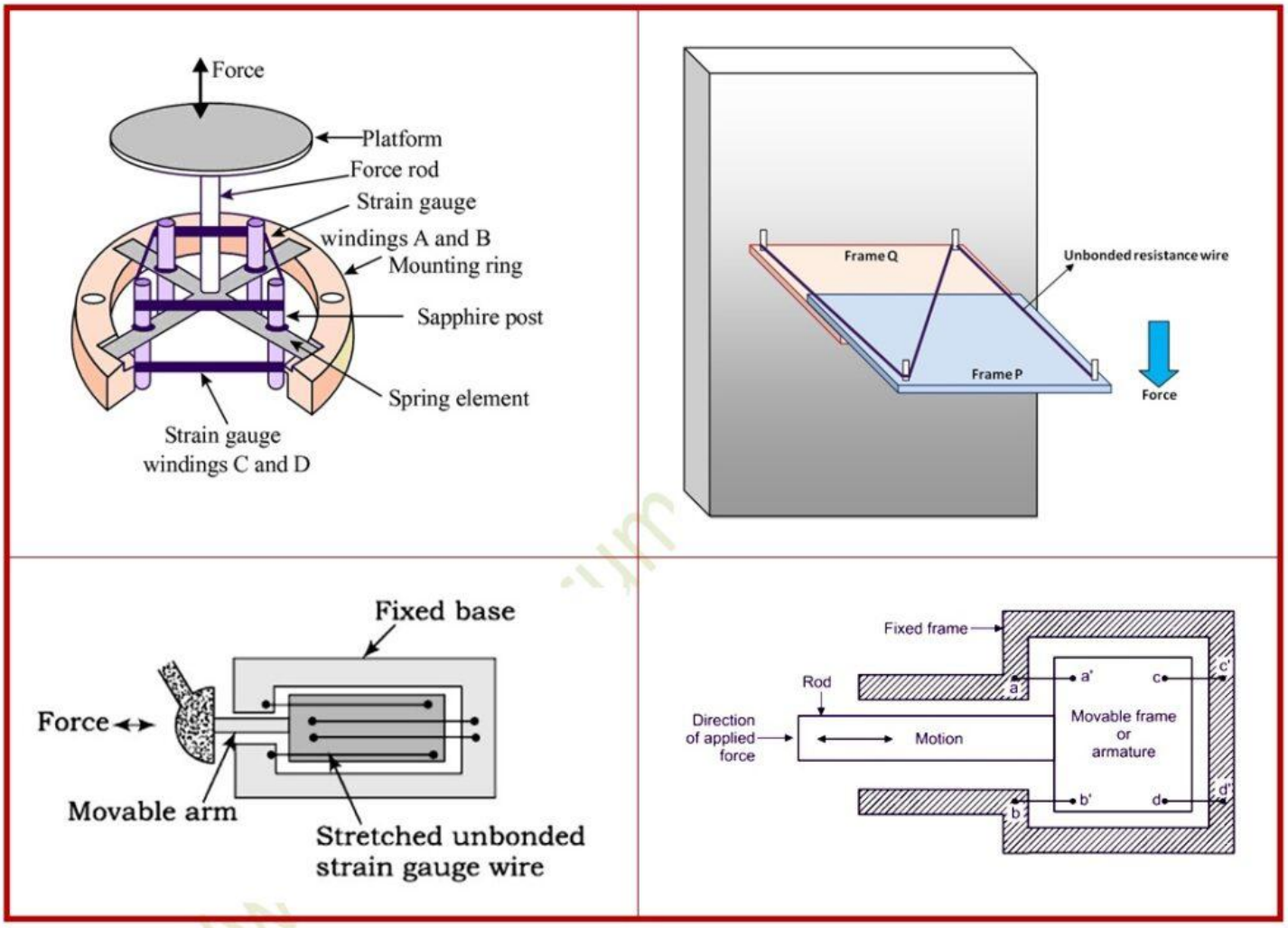


Figure- Different Configurations of Unbonded strain gauge

5. Procedure for Drawing the DC Load Line on CE Output Characteristics

The **DC Load Line** represents all possible combinations of collector-emitter voltage (V_{CE}) and collector current (I_C) for a fixed base current in a **common emitter (CE)** BJT amplifier.

Step-by-Step Procedure:

1. **Start with the DC supply voltage:**

$$V_{CC} = \text{Supply Voltage to the collector (e.g., 12V)}$$

2. **Using Kirchhoff's Voltage Law (KVL):**

$$V_{CC} = I_C \cdot R_C + V_{CE} \Rightarrow V_{CE} = V_{CC} - I_C \cdot R_C$$

   This is the equation of a straight line — the **DC load line**.

3. **Determine the endpoints of the load line:**

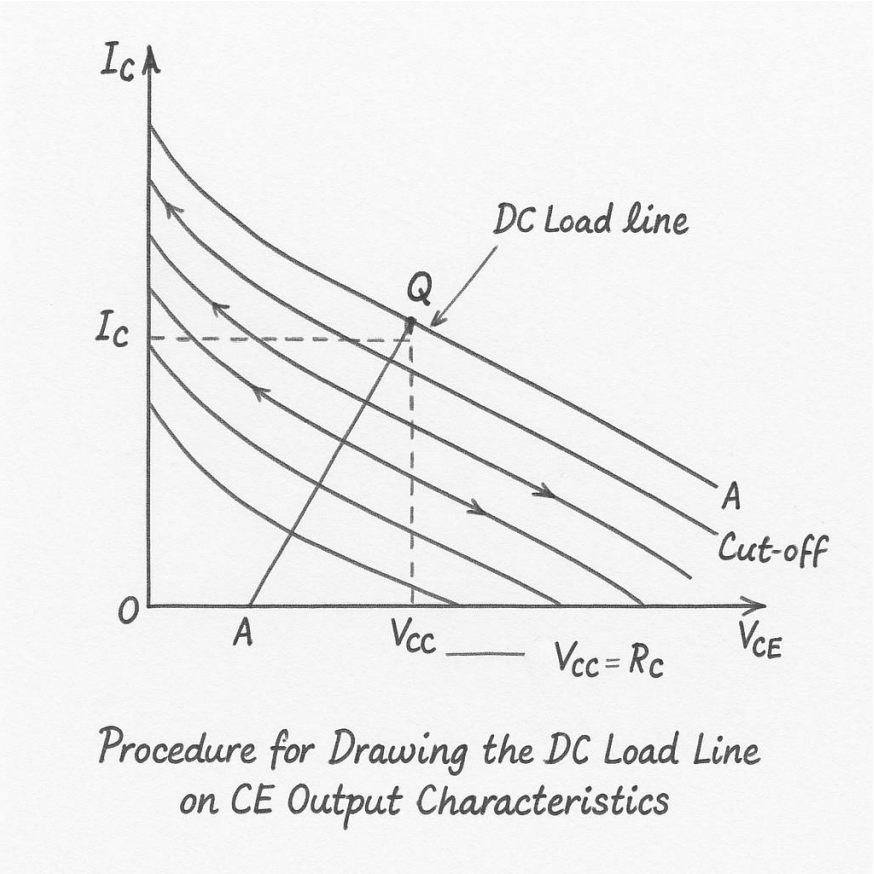
   - **Point A (cut-off):**
     When $I_C = 0 \Rightarrow V_{CE} = V_{CC}$
     (No collector current, transistor OFF)
   - **Point B (saturation):**
     When $V_{CE} = 0 \Rightarrow I_C = V_{CC}/R_C$
     (Maximum collector current, transistor fully ON)

4. **Plot these two points on the output characteristics graph:**

   - X-axis: V_{CE}
   - Y-axis: I_C

   Draw a straight line connecting these two points — that's your **DC load line**.

5. **Q-point (Quiescent Point):**
   Choose a **base current** I_B, and find the corresponding intersection of the transistor's output characteristic curve with the DC load line. This is the operating point (Q-point) where the transistor stays for small input signals.



Procedure for Drawing the DC Load Line on CE Output Characteristics

6. (i) Definitions Related to Operational Amplifiers

a. Input Offset Voltage

Definition:

Input Offset Voltage is the small differential DC voltage required between the inverting (-) and non-inverting (+) terminals of an op-amp to make the output voltage exactly zero (0 V) when it ideally should be zero without any input.

Explanation:

In a perfect op-amp, applying 0 V at both inputs should yield 0 V at the output. However, due to mismatches in the internal transistor pairs, a small offset voltage (typically in microvolts to millivolts) is required to bring the output to zero. This parameter affects precision in applications like instrumentation and DC amplifiers.

> **Example:**
> If an op-amp has an input offset voltage of 2 mV, you must apply +2 mV to the inverting input relative to the non-inverting input to achieve 0 V output.

b.

Definition:

Input Bias Current is the average of the DC currents entering the inverting and non-inverting input terminals of an op-amp.

Formula:

$$I_{\text{Bias}} = \frac{I_{B+} + I_{B-}}{2}$$

Explanation:

Even though op-amp inputs are ideally assumed to have infinite impedance (and hence zero input current), in practice, small bias currents (typically in nanoamperes or picoamperes) flow into the inputs due to the base currents of internal transistors. These currents can cause voltage drops across external resistors, affecting accuracy.

> **Example:**
> If $I_{B+} = 90\,\text{nA}$ and $I_{B-} = 110\,\text{nA}$,

$$I_{\text{Bias}} = \frac{90 + 110}{2} = 100\,\text{nA}$$

c. CMRR (Common-Mode Rejection Ratio)

Definition:

CMRR is the ability of an op-amp to reject **common-mode signals**, i.e., the signals that are present **equally** on both the inverting and non-inverting inputs.

Formula:

$$\text{CMRR} = \frac{A_{\text{Differential}}}{A_{\text{Common}}} \quad (\text{expressed in dB as:}) \quad \text{CMRR}_{\text{dB}} = 20 \log_{10} (\text{CMRR})$$

Explanation:

A high CMRR means the op-amp amplifies only the **difference** between its inputs and ignores any signal common to both. It's critical in differential signal processing and noise rejection.

> **Example:**
> If the differential gain is 100,000 and the common-mode gain is 1,

$$\text{CMRR} = 100{,}000 \Rightarrow \text{CMRR}_{\text{dB}} \approx 100\,\text{dB}$$

d. Slew Rate

Definition:
Slew Rate is the **maximum rate of change** of the op-amp's output voltage per unit time, typically given in **volts per microsecond (V/µs)**.

Formula:

$$\text{Slew Rate} = \frac{dV_{\text{out}}}{dt}$$

Explanation:
It determines how fast the output of the op-amp can respond to rapid changes in the input. If the input signal changes faster than the op-amp's slew rate, the output becomes **distorted** or **slowed down**.

> **Example:**
> If an op-amp has a slew rate of 0.5 V/µs, it can swing its output from 0 V to 5 V in **10 µs**.

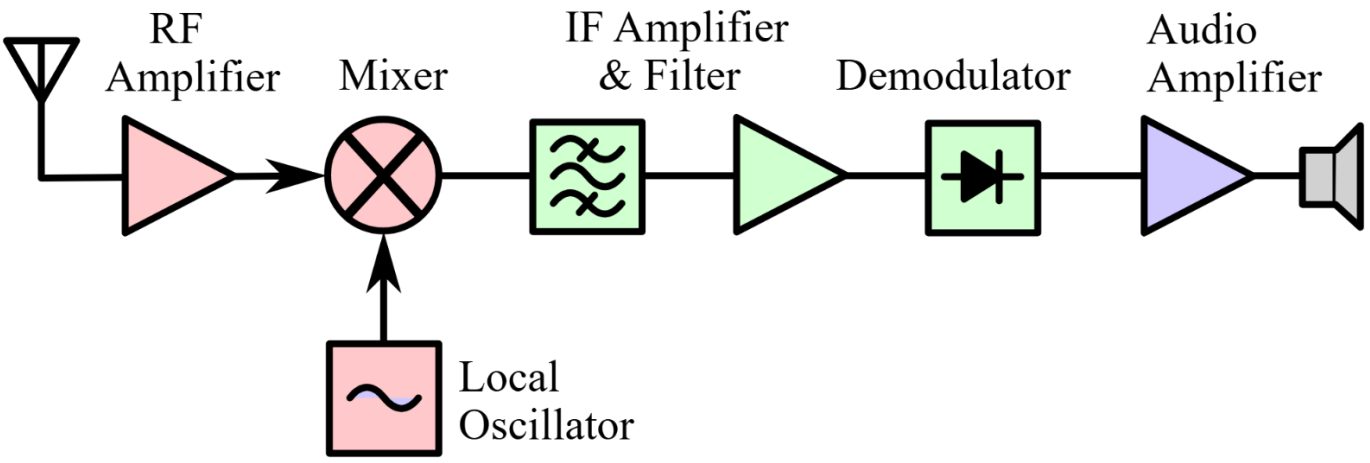
6 (ii). Op-Amp Definition and Ideal Characteristics

An op-amp is a high-gain differential amplifier with infinite input impedance and zero output impedance. Ideal characteristics:

1. Infinite gain
2. Infinite input impedance
3. Zero output impedance
4. Infinite CMRR
5. Infinite Slew Rate

7. Superheterodyne Receiver Block Diagram

The superheterodyne receiver converts high-frequency RF signals to a lower IF (Intermediate Frequency) for easier processing. Blocks include:



Here's a short explanation of each block:

1. **Antenna**: Captures the incoming radio frequency (RF) signal.
2. **RF Amplifier**: Boosts the weak RF signal for better processing.
3. **Mixer**: Combines the RF signal with a signal from the local oscillator to convert it to an intermediate frequency (IF).
4. **Local Oscillator**: Generates a stable frequency that mixes with the RF signal in the mixer.
5. **IF Filter**: Selects the desired intermediate frequency and removes unwanted frequencies.
6. **IF Amplifier**: Amplifies the filtered IF signal.
7. **Detector (Demodulator)**: Extracts the original audio signal from the modulated IF signal.
8. **Audio Amplifier**: Increases the strength of the audio signal for output.
9. **Speaker**: Converts the amplified audio signal into sound.

8. Working of LVDT (Linear Variable Differential Transformer)

LVDT is a sensor that converts linear displacement into an electrical signal. It has a primary coil, two secondary coils, and a movable magnetic core. When the core moves, it unbalances the induced voltage between the secondaries, giving an output proportional to displacement.

Working of LVDT (Linear Variable Differential Transformer):

The Linear Variable Differential Transformer (LVDT) is an electromechanical transducer that converts linear displacement into an electrical signal. It operates on the principle of mutual inductance. The basic structure of an LVDT consists of a primary winding and two secondary windings wound symmetrically on a cylindrical former. A movable soft iron core is placed inside the former and is free to move along the axis of the coil.

When an alternating current (AC) is applied to the primary winding, it induces voltages in both secondary windings through mutual induction. The two secondary windings are connected in series opposition (differentially). At the null position, when the core is at the center, the mutual inductance of both secondary windings is equal, and the induced voltages are equal and opposite. Therefore, the net output voltage is zero.

When the core moves to one side (say left), the mutual inductance with one secondary winding increases while it decreases with the other. This results in an increased voltage in one winding and a decreased voltage in the other, leading to a net output voltage that is proportional to the displacement and phase with respect to the input. Similarly, when the core moves in the opposite direction (right), the output voltage again increases but with a phase shift of 180°, indicating the direction of displacement.

The magnitude of the output voltage is directly proportional to the distance the core has moved, and the phase indicates the direction. This makes the LVDT highly accurate and reliable for linear displacement measurements in various industrial and scientific applications.