		Module – 1	M	L	C
Q.1	a.	Explain the forward and reverse characteristics of semiconductor diode.	08	L2	CO1
	b.	Explain positive half wave rectifier with input and output waveforms.	06	L2	CO1
	c.	Explain Zener diode of voltage regulator with no load.	06	L2	CO1

a.

1. Forward Characteristics (Forward Bias)

Biasing condition:

- **P-side connected to +ve of supply**, **N-side connected to –ve of supply**.
- The external voltage reduces the barrier potential (≈ 0.7 V for silicon, ≈ 0.3 V for germanium).

What happens inside the diode:

- The depletion region **narrows**.
- More majority carriers (electrons from N-side, holes from P-side) cross the junction.
- After the barrier is overcome, current increases rapidly.

I–V characteristic:

- For **V < threshold (cut-in)**: current is very small (almost negligible).
- At **V ≈ threshold** (0.7 V Si / 0.3 V Ge): diode begins to conduct significantly.
- For **V > threshold**: current rises **exponentially** with applied voltage.

Key features:

- **Cut-in voltage** (or threshold voltage) – minimum forward voltage to start significant conduction.
- **Forward resistance** – very small (a few ohms) after conduction starts.

---

2. Reverse Characteristics (Reverse Bias)

Biasing condition:

- **P-side connected to –ve of supply**, **N-side connected to +ve of supply**.
- The external voltage **increases** the barrier potential.

What happens inside the diode:

- Depletion region **widens**.
- Majority carriers are pushed **away** from the junction.
- Only **minority carriers** contribute to current flow (very small).

I–V characteristic:

- A very **small constant current** flows — the **reverse saturation current IsI_sIs**.
- This current is almost **independent of voltage**, but **doubles for every ~10 °C rise** in temperature.
- When reverse voltage exceeds **breakdown voltage (V_BR)**:
    - **Zener breakdown** (in heavily doped diodes at low voltages, <5V).
    - **Avalanche breakdown** (in lightly doped diodes at higher voltages).
    - Diode conducts heavily in reverse direction — if uncontrolled, it can **burn out**.

Key features:

- **Reverse saturation current**: very small leakage.
- **Breakdown region**: large reverse current; Zener diodes exploit this safely.
- **Reverse resistance**: extremely high (megaohms) before breakdown.

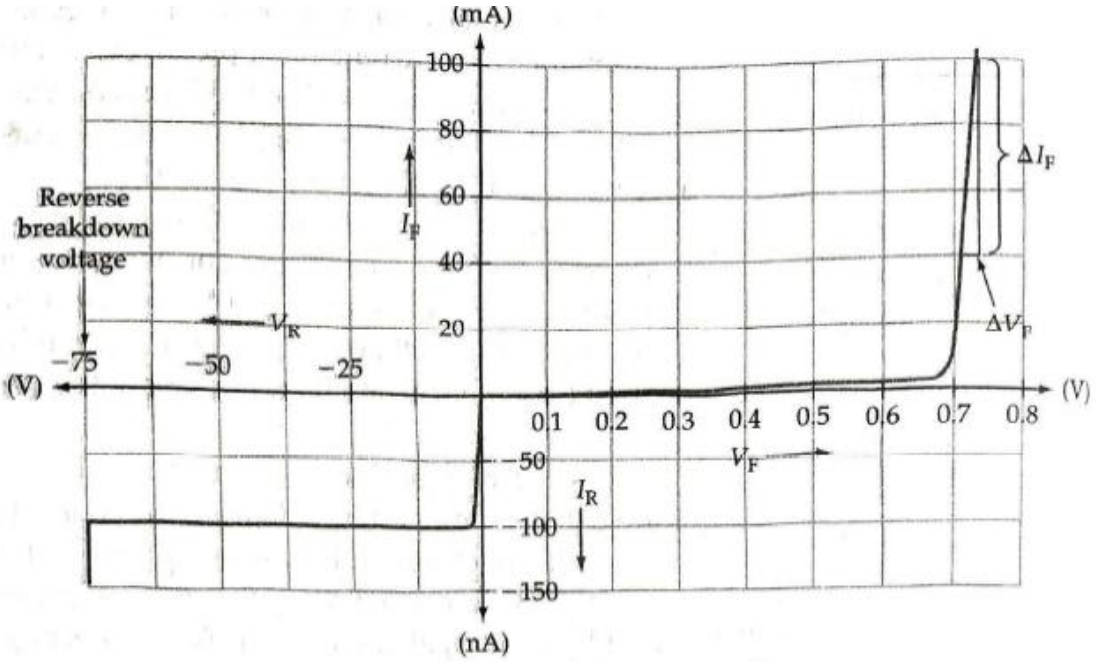


Figure 2-4 Typical forward and reverse characteristics for a silicon diode. There is a substantial forward current (I_F) when the forward voltage (V_F) exceeds approximately 0.7 V.

b.

Positive Half-Wave Rectifier

A diode *positive half-wave rectifier* circuit is shown in Fig. 3-1a. An alternating input voltage is applied via a transformer (T_1) to a single diode connected in series with a load resistor R_L. The transformer is normally necessary to *dc-isolate* the rectifier circuit from the ac supply. The diode is forward-biased during the positive half cycles of the input waveform, and reverse-biased during the negative half cycles. Substantial current flows through R_L only during the positive half cycles of the input. For the duration of the negative half cycles, the diode behaves almost as an open switch. The output voltage waveform developed across R_L is a series of positive half cycles of alternating voltage with intervening very small negative voltage levels produced by the diode reverse saturation current.

When the diode is forward-biased (see Fig. 3-1b), the voltage drop across it is V_F, and the output voltage is (input voltage) $-V_F$. So, the peak output voltage is

$$V_{po} = V_{pi} - V_F \tag{3-1}$$

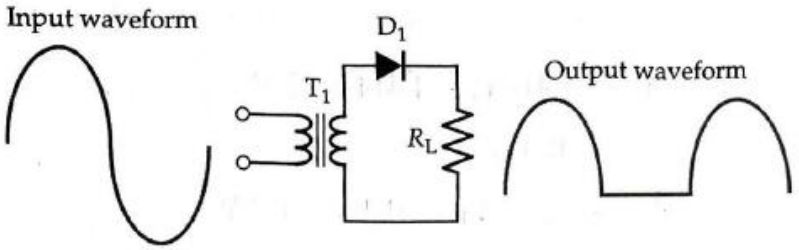
Note that $V_{pi} = 1.414V_i$, where V_i is the rms level of the sinusoidal input voltage to the rectifier circuit (from the transformer output).

The diode peak forward current is

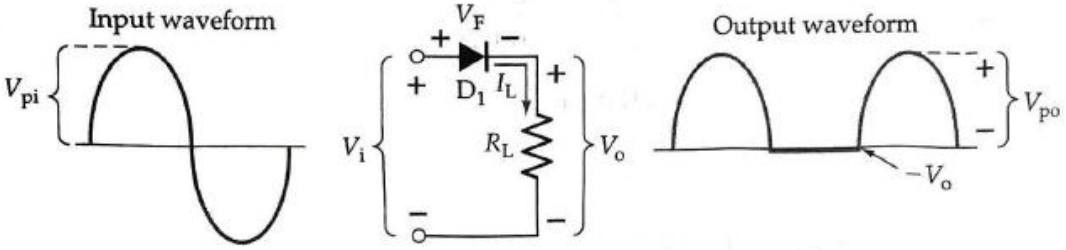
$$I_p = \frac{V_{po}}{R_L} \tag{3-2}$$

During the negative half-cycle of the input (Fig. 3-1c), the reverse-biased diode offers a very high resistance. So there is only a very small reverse current (I_R), giving an output voltage

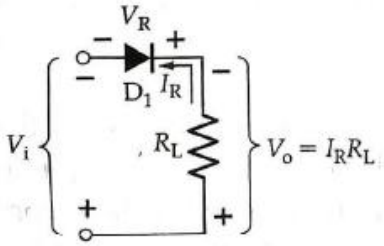
$$-V_o = -I_R R_L \tag{3-3}$$



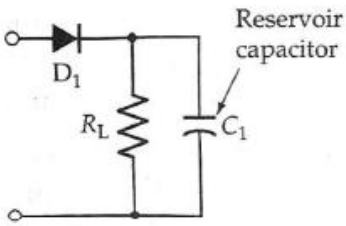
(a) Transformer-coupled half-wave rectifier circuit



(b) Half-wave rectifier circuit with input and output waveforms



(c) Effect of negative input



(d) Use of a reservoir capacitor

Figure 3-1 Positive half-wave rectifier circuit. The diode is forward-biased during the positive half-cycle of the applied waveform and reverse biased during the negative half-cycle.

While the diode is reverse-biased, the peak voltage of the negative half-cycle of the input is applied to its terminals. Thus the *peak reverse voltage*, or *peak inverse voltage (PIV)*, applied to the diode is

$$V_R = \text{PIV} = V_{pi} \tag{3-4}$$

c.

Regulator Circuit with No Load

The most important application of Zener diodes (discussed in Section 2-9) is in dc voltage regulator circuits. These can be the simple regulator circuit shown in Fig. 3-30 or the more complex regulators discussed in Chapter 18. The circuit in Fig. 3-30 is usually employed as a voltage reference source that supplies only a very low current (much lower than I_Z) to the output. Resistor R_1 in Fig. 3-30 limits the Zener diode current to the desired level. I_Z is calculated as follows:

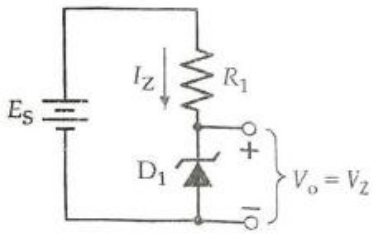


Figure 3-30 Zener diode used as a reference voltage source, or voltage regulator.

$$I_Z = \frac{E_S - V_Z}{R_1} \tag{3-41}$$

The Zener current may be just greater than the diode knee current (I_{ZK}). However, for the most stable reference voltage, I_Z should be selected as I_{ZT} (the specified test current). Example 3-16 demonstrates the circuit design procedure.

		OR			
Q.2	a.	Explain RC π filter.	08	L2	CO1
	b.	What is DC load line? Explain DC load line analysis for semiconductor diode.	08	L2	CO1
	c.	Write down the characteristics of Zener diode.	04	L2	CO1

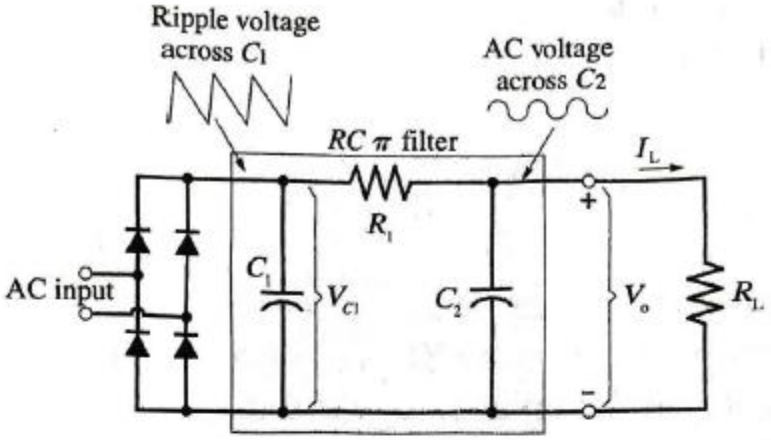
a.

RC π FILTER

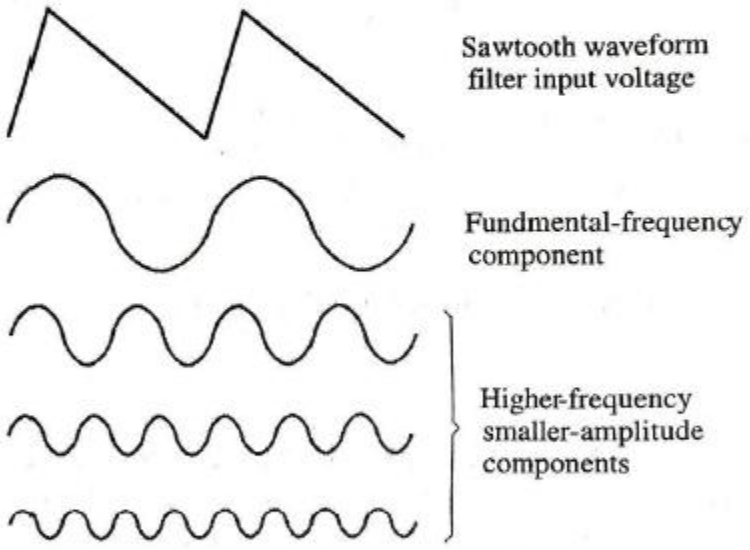
The ripple voltage that appears across the reservoir capacitor in a rectifier power supply can be attenuated by the use of an additional resistor and capacitor, which together function as an ac voltage divider. Figure 3-20a shows the circuit, C_1 being the reservoir capacitor, and R_1 and C_2 the additional components. The combination of C_1, R_1, and C_2 is referred to as a *π filter*, because of the π-shaped arrangement of the circuit components.

Assuming a constant output load current, the reservoir capacitor continues to charge and discharge, producing a sawtooth (ripple) waveform across C_1 regardless of the presence of the additional components. As illustrated in Fig. 3-20b, the sawtooth waveform is composed of a *fundamental ac* voltage (same frequency as the ripple) and a number of smaller-amplitude, higher-frequency harmonic components. Due to their higher frequencies, the harmonic components are more severely attenuated than the fundamental frequency component by the voltage division across R_1 and C_2. This combined with the smaller input amplitude of the harmonics means that the waveform developed across C_2 (the filter output) is essentially an attenuated version of the sinusoidal fundamental component. By Fourier analysis, the peak value of the fundamental component of the sawtooth waveform can be shown to be

$$v_p = \frac{V_r}{\pi} \tag{3-25}$$



(a) $RC\ \pi$ filter circuit



(b) The sawtooth waveform at the filter input consists of a fundamental-frequency component and a number of smaller-amplitude, higher-frequency harmonics

Figure 3-20 When a resistor and capacitor (R_1 and C_2) are connected as a voltage divider to a power supply reservoir capacitor (C_1), the combination is an $RC\ \pi$ filter. The π filter attenuates the ac components that constitute the ripple voltage.

where V_r is the ripple voltage peak-to-peak amplitude.

The ac voltage developed across C_2 is the filter ac output and is given by

$$v_o = \frac{v_i X_{C2}}{\sqrt{R_1^2 + X_{C2}^2}} \quad (3\text{-}26)$$

where v_i is the filter ac input voltage applied across capacitor C_1.

From Eq. 3-26,

$$X_{C2} = \frac{R_1}{\sqrt{(v_i/v_o)^2 - 1}} \quad (3\text{-}27)$$

If $(v_i/v_o)^2 >> 1$,

$$X_{C2} \approx R_1/(v_i/v_o) \quad (3\text{-}28)$$

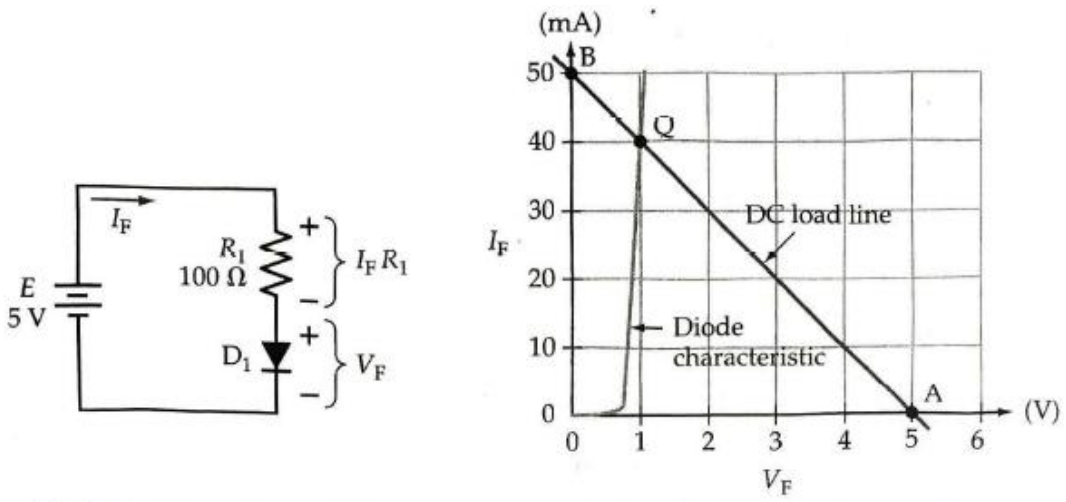
1. What is a DC load line?

- It's a **graphical method** to analyze a nonlinear device (like a diode or transistor) connected to a DC power source with a resistor.
- The **load line represents all possible combinations of current (I) and voltage (V)** in the circuit **due to the external supply and resistor**, **before** considering the diode's own characteristics.
- When you plot the diode's **I–V characteristic curve** on the same graph, the **operating point (Q-point)** is simply **where the two curves intersect**.

2-4 DC LOAD LINE ANALYSIS

DC Load Line

Figure 2-13a shows a diode in series with a 100 Ω resistor (R_1) and a supply voltage (E). The polarity of E is such that the diode is forward-biased, so that there is a diode forward current (I_F). As already discussed, the circuit current can be determined approximately by assuming a constant diode forward voltage drop (V_F). When the precise levels of the diode current and voltage must be calculated, *graphical analysis* (also termed *dc load line analysis*) is employed.



(a) Diode-resistor series circuit

(b) Plotting the dc load line on the diode characteristics

Figure 2-13 Drawing a dc load line on the diode characteristic.

For graphical analysis, a dc load line is drawn on the diode forward characteristics (Fig. 2-13b). This is a straight line that illustrates all dc conditions that could exist within the circuit. Because the load line is always straight, it can be constructed by plotting any two corresponding current and voltage points and then drawing a straight line through them. To determine two points on the load line, an equation relating voltage, current, and resistance is first derived for the circuit. From Fig. 2-13a,

$$E = (I_F R_1) + V_F \tag{2-3}$$

Any two convenient levels of I_F can be substituted into Eq. 2-3 to calculate corresponding V_F levels, or vice versa. As demonstrated in Ex. 2-6, it is convenient to calculate V_F when $I_F = 0$, and to determine I_F when $V_F = 0$.

c.

1. What is a Zener diode?

- Like a normal diode, it conducts strongly in **forward bias** (after ~0.7 V for Si).
- In **reverse bias**, it behaves differently:

    - For low voltages, only a tiny leakage current flows.
    - When the reverse voltage reaches a certain **critical value (Zener voltage VZV_ZVZ)**, the diode enters **breakdown** and conducts heavily **without damage** (if current is limited by a resistor).

This controlled reverse conduction is its key feature.

---

2. Zener diode I–V characteristics

Forward bias (positive voltage to anode)

- Behaves like an ordinary diode.
- Current is negligible until about **0.7 V (Si)** or **0.3 V (Ge)**.
- After this, current rises exponentially with voltage.
- This region is **rarely used** in Zener applications.

Reverse bias (positive voltage to cathode)

- **Leakage region:**
    - For voltages less than VZV_ZVZ, only a **tiny reverse saturation current** flows.
- **Breakdown region:**
    - When VR=VZV_R = V_ZVR=VZ, the diode starts to conduct **heavily in reverse**.
    - The voltage across the diode stays **nearly constant at VZV_ZVZ** even if current changes widely — this is the **voltage regulation property**.
- **Excess current protection:**
    - A series resistor must be used to prevent current exceeding the diode's rated maximum (called **I_Z(max)**), otherwise it will overheat.

---

3. Types of breakdown in Zener diodes

- **Zener breakdown (V_Z < 5 V):**
    - Occurs in heavily doped diodes.

    - Due to strong electric fields causing quantum tunneling of carriers.
    - Sharp, well-defined breakdown voltage.
- **Avalanche breakdown (V_Z > 5 V):**
    - Occurs in lightly doped diodes.
    - Carriers gain high energy and knock loose more carriers (impact ionization).
    - Slightly softer breakdown, but still stable if current is controlled.

---

4. Key features of the reverse characteristic

- **Zener voltage (V_Z):**
    - The nearly constant voltage maintained during breakdown.
- **Dynamic resistance (r_z):**
    - A small slope in the breakdown region (not perfectly flat).
- **Zener knee current (I_Z(min)):**
    - Minimum current required to keep the diode in the breakdown region and maintain voltage regulation.
- **Maximum Zener current (I_Z(max)):**
    - Maximum safe current to prevent overheating.

---

5. Applications (why this is useful)

- **Voltage regulation:** Keeps output voltage constant despite supply variations.
- **Reference voltage:** Provides precise voltage in circuits.
- **Waveform clipping/clamping:** Limits voltage to a preset level to protect circuits.
- **Switching:** Used in over-voltage protection devices.

---

6. Visual description of the I–V curve

1. **Forward bias (right side of graph):** Like a normal diode — little current until ~0.7 V, then exponential rise.

2. **Reverse bias (left side):**
    - Flat, tiny current until the **breakdown knee (V_Z)**.
    - Then current jumps up steeply, but **voltage remains almost constant at V_Z**.

If I were drawing it:

- Horizontal axis = Voltage (positive right, negative left).
- Vertical axis = Current (positive up, negative down).
- Sharp vertical rise in current at negative V_Z, indicating controlled breakdown.

Module – 2

Q.3	a.	Explain BJT current amplification for increasing and decreasing IB level.	08	L2	CO2
	b.	Explain common base input characteristics of BJT.	06	L2	CO2
	c.	With a neat diagram explain the working of n channel JFET.	06	L2	CO2

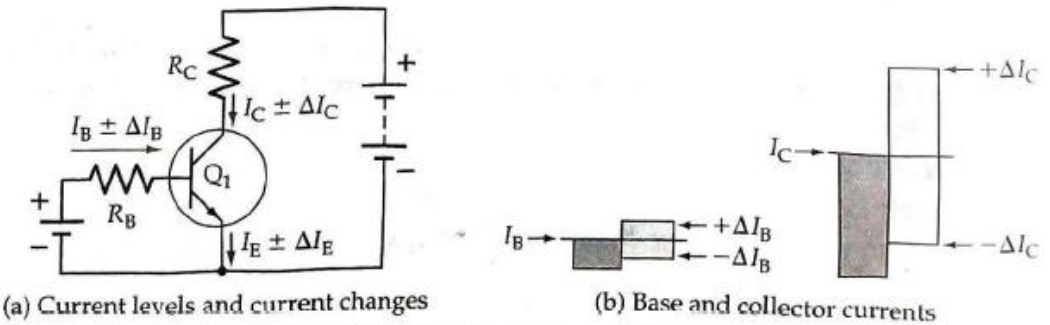
A

Current Amplification

The equations derived in Section 4-2 demonstrate that a transistor can be used for current amplification. A small change in the base current (ΔI_B) produces a large change in collector current (ΔI_C) and a large emitter current change (ΔI_E) (see Figs 4-16a and b). Rewriting Eq. 4-5, the current gain from the base to collector can be stated in terms of current level changes.

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

The increasing and decreasing levels of input and output currents may be defined as alternating quantities. In this case, small (lower-case) letters are used for the subscripts. Thus, I_b is an ac base current, I_c is an ac collector



(a) Current levels and current changes (b) Base and collector currents

Figure 4-16 BJT current amplification. Increasing and decreasing the I_B levels produces much larger changes in I_C and I_E.

current, and I_e is an ac emitter current. The alternating current gain from base to collector may now be stated as

$$\beta_{ac} = \frac{I_c}{I_b} \tag{4-7}$$

As in the case of dc current gain, two parameter symbols are available for common-emitter ac current gain: β_{ac} and h_{fe}. Either symbol may be used, but, once again, h_{fe} *is the symbol employed on transistor data sheets.*

B

Common-Base Circuit

When a diode (a two-terminal device) is investigated, several levels of forward or reverse voltage are applied and the corresponding current levels are measured (see Section 2-8). The characteristics of the device are then drawn by plotting the graph of current versus voltage. Because a transistor is a three-terminal device, there are three possible connection arrangements (configurations) for investigating its characteristics. Three sets of characteristics may be constructed for each of these configurations.

Figure 4-22 shows a *pnp* transistor with its base terminal common to both the input (emitter-base) terminals and the output (collector-base) terminals. The transistor is said to be connected in *common-base* configuration. Voltmeters

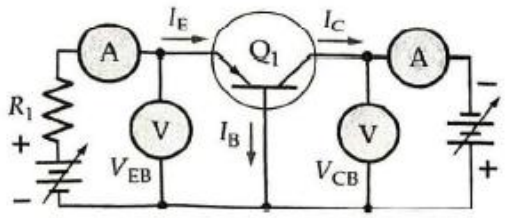


Figure 4-22 Circuit for investigating BJT common-base characteristics. The base is common to the input voltage (V_{EB}) and the output voltage (V_{CB}).

and ammeters are included to measure the input and output voltages and currents. Note the presence of resistor R_1 to assist in controlling the emitter current.

Common-Base Input Characteristics

To investigate the input characteristics, the output voltage (V_{CB}) in Fig. 4-22 is kept constant, and the input voltage (V_{EB}) is set at several convenient levels. At each input voltage, the corresponding input current (I_E) is recorded. The I_E and V_{EB} levels are then plotted to give the common-base input characteristics shown in Fig. 4-23.

Because the emitter-base junction is forward-biased, the characteristics are essentially those of a forward-biased *pn*-junction. Figure 4-23 also shows that for a given input voltage (V_{EB}), more input current flows when higher levels of collector-base (V_{CB}) voltage are used. This is because larger collector-base (reverse-bias) voltages cause the depletion region at the collector-base junction to penetrate deeper into the base of the transistor, thus shortening the distance and reducing the resistance between the emitter-base and collector-base depletion regions.

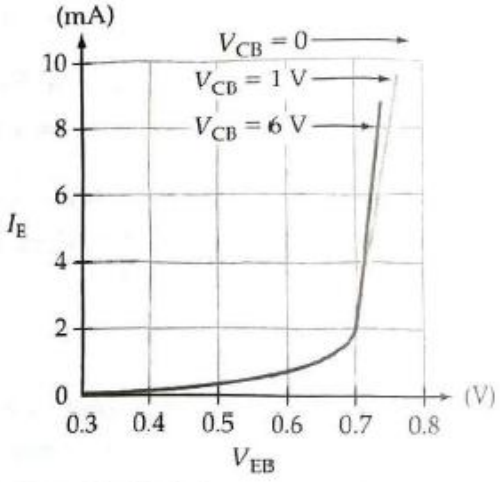


Figure 4-23 The common-base input characteristics for a BJT are (input) emitter current I_E plotted versus (input) base-emitter voltage V_{EB}. The characteristics are similar to those of a forward biased *pn*-junction.

C

n-Channel JFET

The operating principle of an *n-channel junction field effect transistor* (JFET) is illustrated by the block representation in Fig. 9-1a. A piece of *n*-type semiconductor material, referred to as the *channel*, is sandwiched between two smaller pieces of *p*-type (the *gates*). The ends of the channel are designated the *drain* (*D*) and the *source* (*S*), and the two pieces of *p*-type material are connected together and their terminal is named the *gate* (*G*).

With the gate left unconnected and a drain-source voltage (V_D) applied (positive at the drain, negative at the source), a *drain current* (I_D) flows, as shown in Fig. 9-1a. When a gate-source voltage (V_{GS}) is applied with the gate negative with respect to the source (Fig. 9-1b), the gate-channel *pn*-junctions are reverse biased. The channel is more lightly doped than the gate material, so the depletion regions penetrate deep into the channel. Because the depletion regions are regions depleted of charge carriers, they behave as insulators. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced. When the negative gate-source bias voltage is further increased, the depletion regions meet at the centre of the channel (Fig. 9-1c), and I_D is cut off.

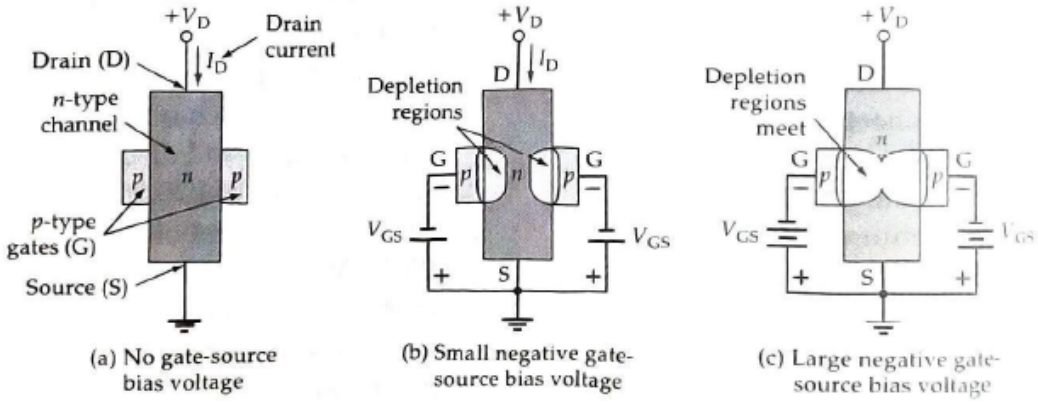


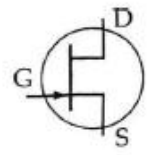
Figure 9-1 An *n*-channel JFET consists of an *n*-type channel with *p*-type gate regions on each side.

An ac signal applied to the gate causes the reverse gate-source voltage to increase as the instantaneous level of the signal goes negative, and to decrease when the signal is positive-going. This causes the gate-channel depletion regions to widen and decrease successively. When the signal goes negative, the depletions widen, the channel resistance is increased, and the drain current decreases. As the signal goes positive, the depletion regions recede, the channel resistance is reduced, and the drain current increases. It is

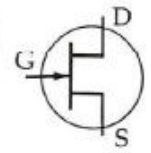
seen that the FET gate-source voltage controls the drain current. The gate-channel *pn*-junctions are maintained in reverse bias, so the gate current is normally extremely low, much lower than the base current for a BJT.

The name *field effect transistor* comes from the fact that the depletion regions in the channel are produced by the electric field at the reverse-biased gate-channel junctions. The term *unipolar device* is sometimes applied to a *FET*, because, unlike a bipolar transistor, the current consists of only one type of charge carrier: electrons in the case of an *n*-channel device.

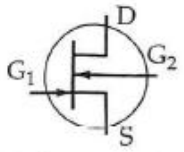
Circuit symbols for an *n*-channel JFET are shown in Fig. 9-2. As in the case of all semiconductor device symbols, the arrowhead points from *p*-type to *n*-type. For an *n*-channel device, the arrowhead points from the *p*-type gate to the *n*-type channel. This is the direction of conventional current flow if the junctions become forward biased. Some device manufacturers use the symbol in Fig. 9-2a with the gate directly opposite the source terminal. Others show the gate centralized between the drain and source (Fig. 9-2b). This can sometimes make circuit diagrams confusing unless the drain and source terminals are clearly identified. The symbol in Fig. 9-2c is used when the terminals of the two gate regions are provided with separate connecting leads. In this case, the device is referred to as a *tetrode-connected FET*.



(a) Circuit symbol for *n*-channel JFET



(b) Alternative circuit symbol



(c) Tetrode-connected JFET

Figure 9-2 Circuit symbols for an *n*-channel JFET. Like all semiconductor symbols, the arrowheads point from the *p*-type to the *n*-type material.

		OR			
Q.4	a.	Explain the operation of enhancement MOSFET.	08	L2	CO2
	b.	Draw the DC load line for transistor and identify Q points.	08	L2	CO2
	c.	Describe common emitter input characteristics.	04	L2	CO2

A

Enhancement MOSFET

Figure 9-29 shows the construction of a *metal oxide semiconductor FET (MOSFET)*, also known as an *insulated gate FET*. Starting with a high-resistive *p*-type substrate, two blocks of heavily-doped *n*-type material are diffused into the substrate, and then the surface is coated with a layer of silicon dioxide. Holes are cut through the silicon dioxide to make contact with the *n*-type blocks. Metal is deposited through the holes for source and drain terminals, as illustrated, and a metal plate is deposited on the surface area between drain and source. As will be explained, this plate functions as a gate.

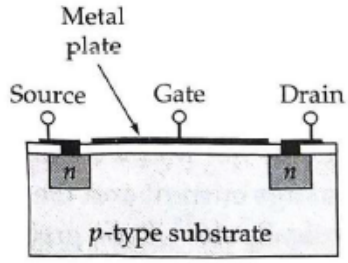
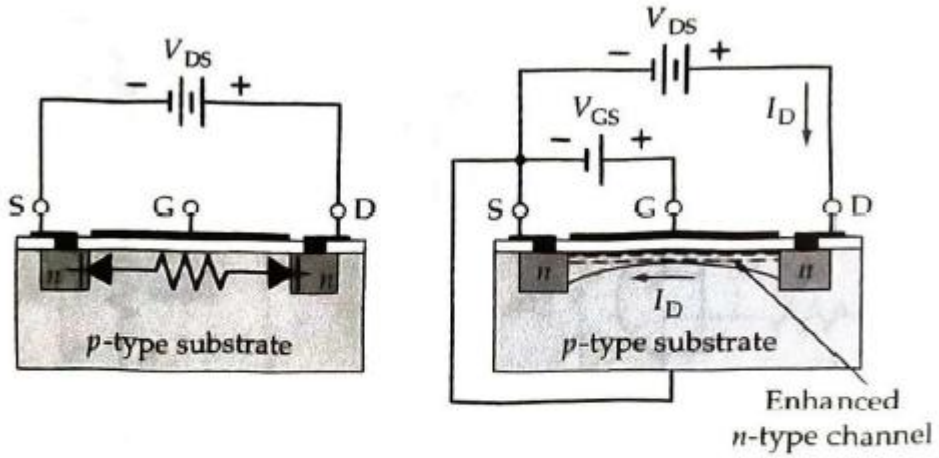


Figure 9-29 Metal oxide semiconductor FET (MOSFET) construction.

Consider the situation illustrated in Fig. 9-30a. The drain terminal of the MOSFET is positive with respect to the source, and the gate is open-circuited.



(a) V_{DS} applied and gate open-circuited

(b) Effect of positive V_{GS}

Figure 9-30 Effect of $+V_{DS}$ on the MOSFET with the gate terminal open-circuited and with $+V_{GS}$ applied to the gate.

The two *n*-type blocks and the *p*-type substrate form back-to-back *pn*-junctions connected by the resistance of the *p*-type material, as illustrated. The *pn*-junction close to the drain terminal is reverse biased, so that only a very small (reverse-leakage) current flows from D to S.

Now assume that the source terminal is connected to the substrate and that a positive gate voltage is applied, as shown in Fig. 9-30b. Negative (minority) charge carriers within the substrate are attracted to the (positive) plate that constitutes the gate. Since these charge carriers (electrons) cannot cross the silicon dioxide to the gate, they accumulate close to the surface of the substrate, as shown. The minority charge carriers constitute an *n*-type channel between drain and source, and as the gate-source voltage is made more positive, more electrons are attracted into the channel, causing the channel resistance to decrease. A drain current flows along the channel between the D and S terminals, and because the channel resistance is controlled by the gate-source voltage (V_{GS}), the drain current is also controlled by V_{GS}. The channel conductivity is said to be *enhanced* by the positive gate-source voltage, and so the device is known as an *enhancement-mode MOSFET (EMOSFET or EMOS transistor)*.

Typical drain and transfer characteristics for an *n*-channel EMOS device are shown in Fig. 9-31. Note that on both characteristics the drain current increases as the positive gate-source bias voltage is increased. Because the gate of the MOSFET is insulated from the channel, there is no gate-source leakage current and the device has an extremely high (gate) input resistance: typically $10^{15}\ \Omega$ or greater. Typical forward transfer admittance values for this type of (low-power) MOSFET range from 1 mS (1 mA/V) to a maximum of perhaps 6 mS, which is similar to JFET Y_{fs} values.

Two graphic symbols for the *n*-channel EMOS transistor are shown in Fig. 9-32. One symbol shows the source and substrate connected internally, while the other has a separate substrate terminal. The line representing the

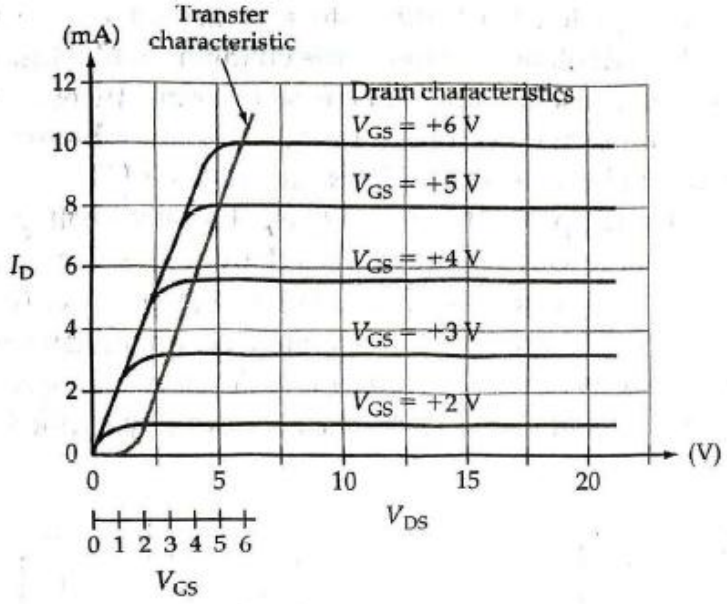


Figure 9-31 Typical drain and transfer characteristics for an *n*-channel EMOS transistor.

device channel is broken into three sections to indicate that the channel does not exist until an appropriate gate voltage is applied. To show that the device has an insulated gate, the gate symbol does not make direct contact with the channel. The arrowhead points from the *p*-type substrate to the *n*-type channel.

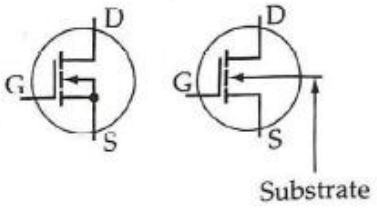
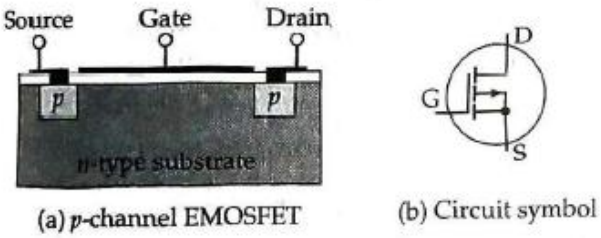


Figure 9-32 Circuit symbols for an *n*-channel EMOSFET.

A *p*-channel EMOS transistor is constructed by starting with an *n*-type substrate and diffusing *p*-type drain and source blocks, as illustrated in Fig. 9-33a. The device characteristics are similar to those in Fig. 9-31, except that all voltage polarities and current directions are reversed. The drain-source voltage is negative, and a negative gate-source voltage is required to create the *p*-type channel. The arrowheads in the circuit symbols are also reversed (see Fig. 9-33b).



(a) *p*-channel EMOSFET (b) Circuit symbol

Figure 9-33 Construction and circuit symbol for a *p*-channel EMOSFET.

5-1 DC LOAD LINE AND BIAS POINT

DC Load Line

The *dc load line* for a transistor circuit is a straight line drawn on the transistor output characteristics. For a common-emitter (CE) circuit, the load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance (R_C) and a given supply voltage (V_{CC}). The load line shows all corresponding levels of I_C and V_{CE} that can exist in a particular circuit.

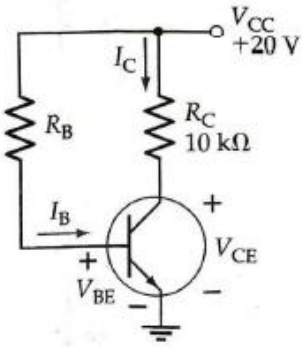


Figure 5-1 Transistor circuit with collector resistor R_C.

Consider the common-emitter circuit in Fig. 5-1. Note that the polarities of the transistor terminal voltages are such that the base-emitter junction is forward-biased and the collector-base junction is reverse-biased. These are the normal bias polarities for the transistor junctions. The dc load line for the circuit in Fig. 5-1 is drawn on the device common-emitter characteristics in Fig. 5-2.

From Fig. 5-1, the collector-emitter voltage is

$$V_{CE} = (\text{supply voltage}) - (\text{voltage drop across } R_C)$$

or

$$V_{CE} = V_{CC} - I_C R_C \qquad (5\text{-}1)$$

If the base-emitter voltage (V_{BE}) is zero, the transistor is not conducting and $I_C = 0$. Substituting the V_{CC} and R_C values from Fig. 5-1 into Eq. 5-1,

$$V_{CE} = 20\ \text{V} - (0 \times 10\ \text{k}\Omega)$$
$$= 20\ \text{V}$$

Plot *point A* on the common-emitter characteristics in Fig. 5-2 at $I_C = 0$ and $V_{CE} = 20$ V. This is one point on the dc load line.

Now assume a collector current of 2 mA, and calculate the corresponding collector-emitter voltage level.

$$V_{CE} = 20\text{ V} - (2\text{ mA} \times 10\text{ k}\Omega)$$
$$= 0\text{ V}$$

Plot *point B* on Fig. 5-2 at $V_{CE} = 0$ and $I_C = 2$ mA. The straight line drawn through points A and B is the dc load line for $R_C = 10$ kΩ and $V_{CC} = 20$ V. If either of these two quantities is changed, a new load line must be drawn.

As already stated, the dc load line represents all corresponding I_C and V_{CE} levels that can exist in the circuit, as represented by Eq. 5-1. For example, a point plotted at $V_{CE} = 16$ V and $I_C = 1.5$ mA on Fig. 5-2 does not appear on the load line. This combination of voltage and current cannot exist in this particular circuit (Fig. 5-1). Knowing any one of I_B, I_C, or V_{CE}, it is easy to determine the other two from a dc load line drawn on the device characteristics.

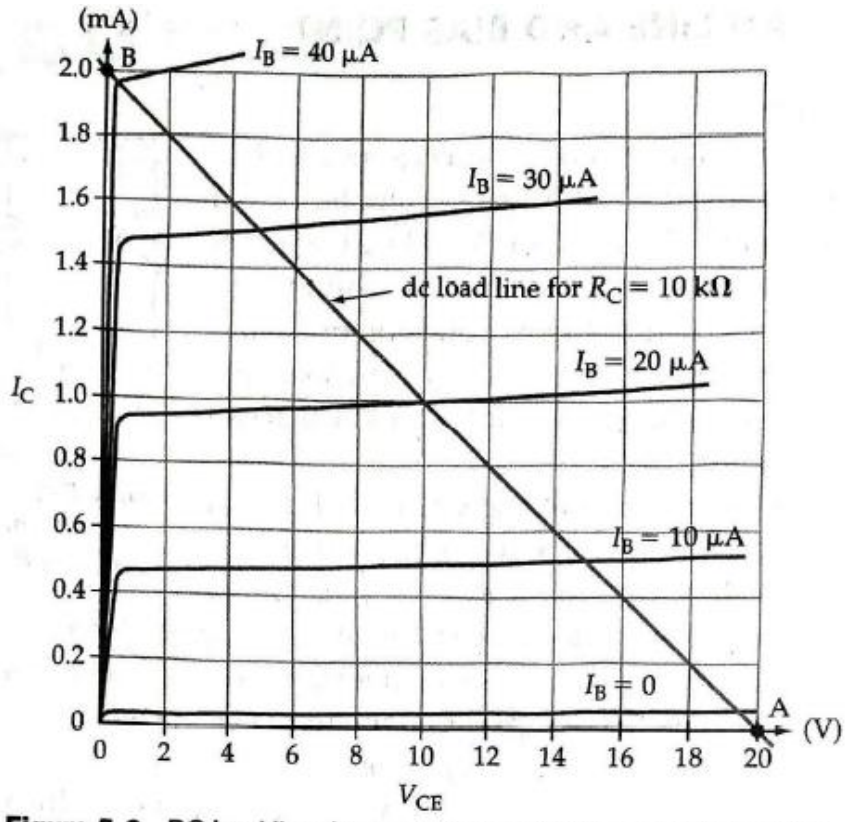


Figure 5-2 DC load line drawn upon transistor common-emitter output characteristics.

It is not always necessary to have the device characteristics in order to draw the dc load line. A simple graph of I_C versus V_{CE} can be used, as demonstrated in Ex. 5-1.

C

Common-Emitter Circuit

Figure 4-28 shows a circuit for determining BJT common-emitter characteristics. The input voltage is applied between the base and emitter terminals, and the output is taken at the collector and emitter terminals, so that the emitter terminal is common to both input and output. Resistor R_1 is included to help maintain the base current at a constant level. Voltage and current levels are measured as shown.

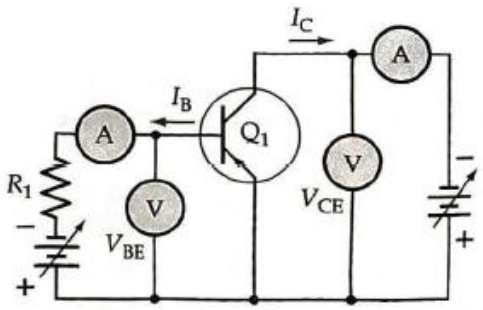


Figure 4-28 Circuit for investigating BJT common-emitter characteristics. The emitter is common to the input voltage (V_{BE}) and the output voltage (V_{CE}).

Common-Emitter Input Characteristics

To prepare a table of measured values for constructing the common-emitter input characteristics, V_{CE} is held constant, V_{BE} is set at convenient levels, and the corresponding I_B levels are recorded. I_B is then plotted versus V_{BE}, as shown in Fig. 4-29. It is seen that the common-emitter input characteristics (like the common-base input characteristics) are those of a forward-biased *pn*-junction. It should be remembered that I_B is only a small portion of the total current (I_E) that flows across the base-emitter junction.

Figure 4-29 also shows that, for a given level of V_{BE}, I_B is reduced when higher V_{CE} levels are employed. This is because the higher V_{CE} produces greater depletion region penetration into the base, reducing the distance between the collector-base and emitter-base depletion regions.

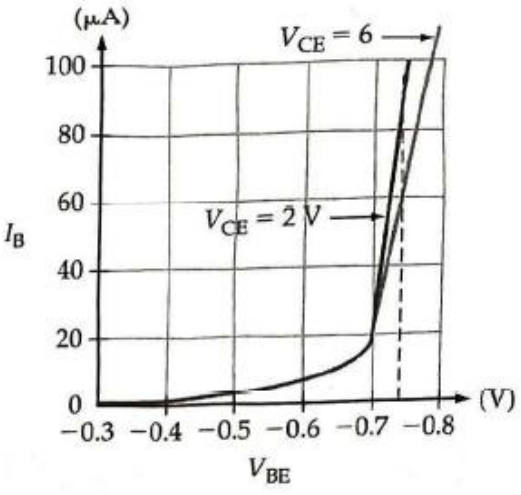


Figure 4-29 The common-emitter input characteristics for a BJT are (input) base current I_B plotted versus (input) base-emitter voltage V_{BE}. The characteristics are similar to those of a forward biased *pn*-junction.

		Module – 3			
Q.5	a.	With a neat block diagrams explain the typical op-Amp.	06	L2	CO3
	b.	Explain working of a differential amplifier.	08	L2	CO3
	c.	Explain op-Amp of an integrator circuit with an input and output waveform using square wave of input.	06	L2	CO3

1. What is an Op-Amp?

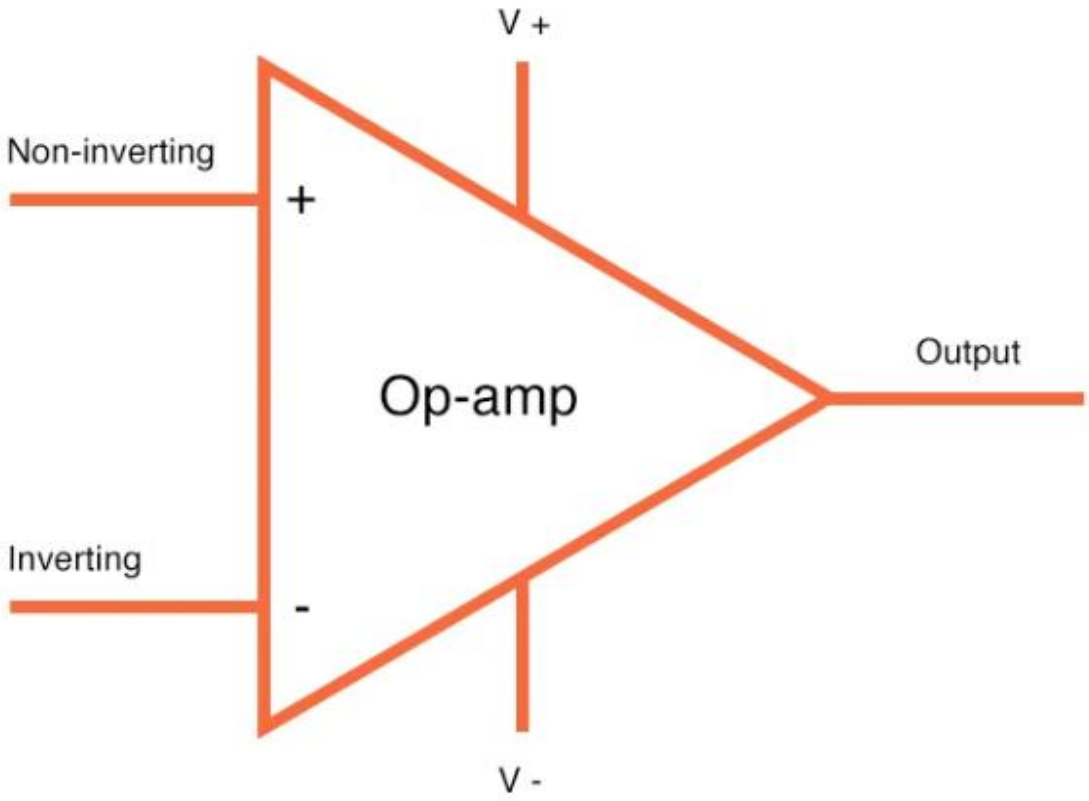
- An **operational amplifier** is a **high-gain, direct-coupled amplifier** with **differential input** and **single-ended output**.
- It was originally used to perform mathematical operations (addition, subtraction, integration, differentiation), hence the name "operational."
- Modern op-amps are used in **signal conditioning, filtering, instrumentation, oscillators, control systems, and analog computation**.

---

2. Symbol of a typical op-amp

The **standard symbol** is a triangle:

- **Two input terminals:**
  - **Inverting input (–)**
  - **Non-inverting input (+)**
- **One output terminal**
- **Power supply pins** (not always shown in basic diagrams): +Vcc and –Vee or –Vcc



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3. Typical internal structure of an op-amp

Although modern op-amps are integrated circuits with dozens of transistors, the internal structure can be conceptually divided into **three stages**:

(A) Differential amplifier input stage

- Two matched transistors form a **differential pair**.
- This stage **amplifies the difference between the two input voltages** (V+ and V–).
- Provides **high input impedance** and **low noise**.

(B) Intermediate gain stage

- Usually a **high-gain common-emitter amplifier** or a **cascaded amplifier**.
- Increases the voltage gain to a very high value (10^4 – 10^5).
- May include an **active load** or **current mirror** to improve gain.
- Often includes **frequency compensation** (using a capacitor) to maintain stability.

(C) Output stage

- Usually a **class-B or class-AB push-pull emitter follower**.
- Provides **low output impedance** to drive loads.
- Ensures the op-amp can source or sink current efficiently.

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4. Ideal vs Practical Characteristics

Ideal op-amp characteristics

- **Infinite open-loop gain (A → ∞)**
- **Infinite input impedance (Rin → ∞)** → no input current drawn
- **Zero output impedance (Rout → 0)** → can drive any load without loss
- **Infinite bandwidth** → amplifies all frequencies equally
- **Zero offset voltage** → output is exactly zero if inputs are equal
- **Infinite common-mode rejection ratio (CMRR)** → ignores any common signal at both inputs

Practical op-amp characteristics

- **Open-loop gain:** very high (10^5 to 10^6), but not infinite
- **Input impedance:** very high (10^6 to 10^{12} Ω)
- **Output impedance:** low (10 Ω to 100 Ω)
- **Bandwidth:** limited (MHz range)
- **Small input bias current** and **offset voltage** present

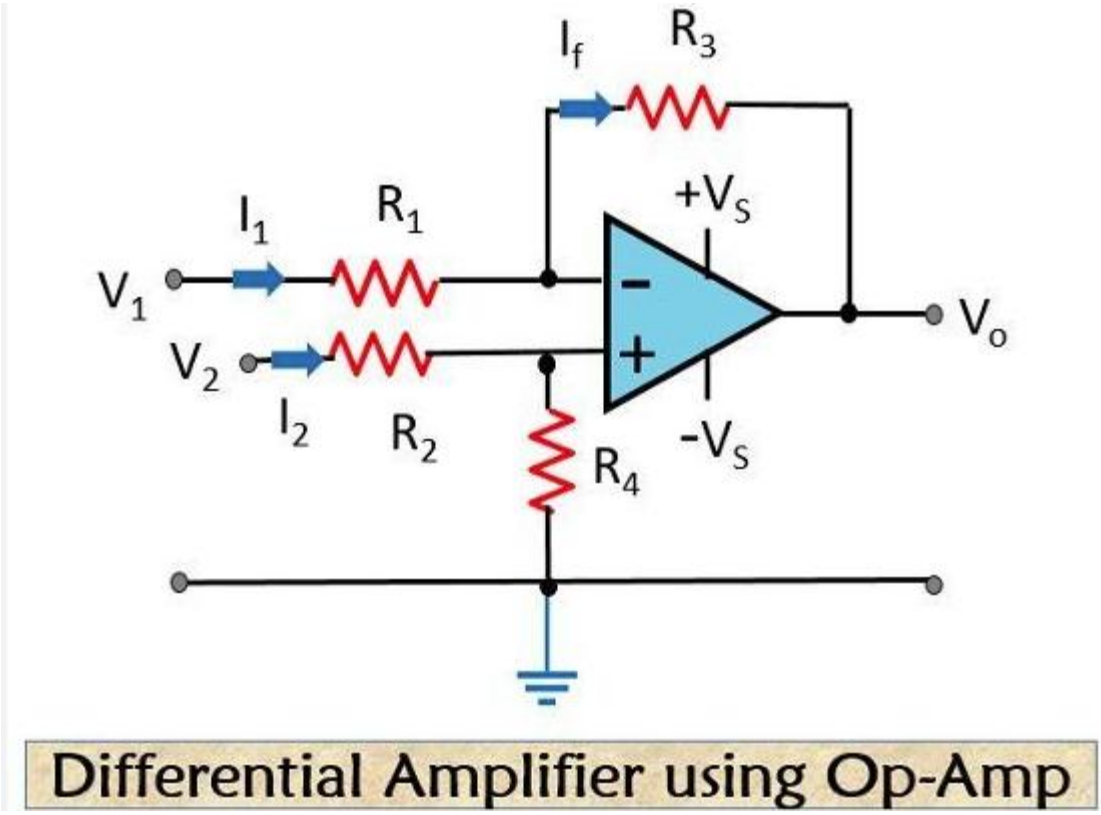
---

5. Neat diagram of a typical op-amp

A clean diagram should include:

1. **Block stages:** differential input → gain stage → output stage
2. **Input and output terminals clearly labeled** (+, –, Vout)
3. **Power supply rails** (+Vcc, –Vcc)
4. **Arrows showing signal flow** from input to output

B


I_f
R_3
$+V_S$
I_1
R_1
V_1
V_2
I_2
R_2
R_4
$-V_S$
V_o
Differential Amplifier using Op-Amp

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

Summing point $V_a = V_b$

and $V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$

If $V_2 = 0$, then: $V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$

If $V_1 = 0$, then: $V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

Differential Amplifier Equation

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

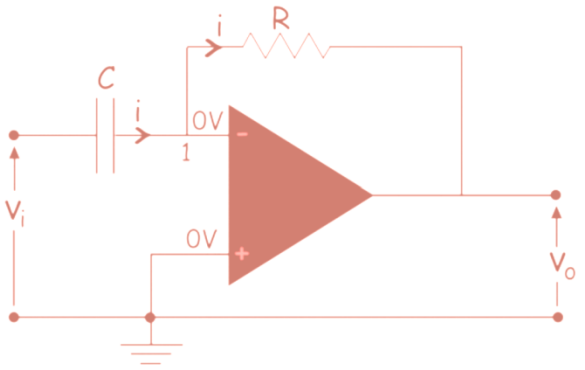
If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = $V_2 - V_1$.

Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive.

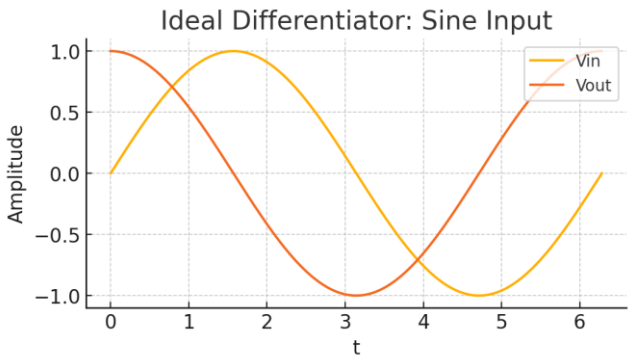
The **Differential Amplifier** circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors R1 and R3, the resultant circuit can be made to either "Add" or "Subtract" the voltages applied to their respective inputs. One of the most common ways of doing this is to connect a "Resistive Bridge" commonly called a *Wheatstone Bridge* to the input of the amplifier as shown below.

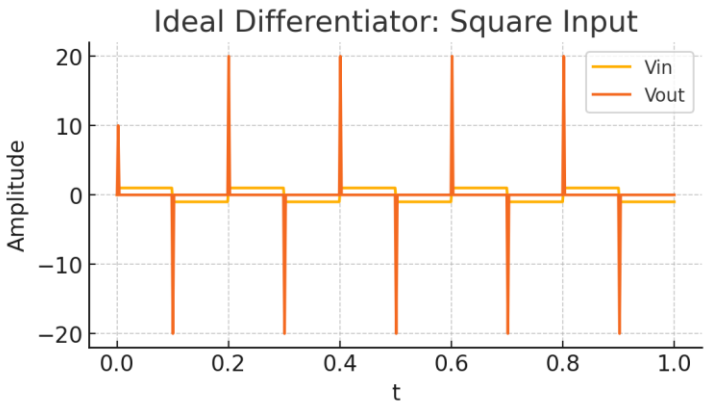
Q6 (a) Explain Differentiator with waveform and circuit.

An op-amp differentiator produces an output proportional to the time-derivative of the input. For the ideal inverting differentiator, the input capacitor C and feedback resistor Rf give Vout(t) = −Rf · C · dVin(t)/dt. Practical versions add a small Rin in series with C and a capacitor Cf in parallel with Rf to limit high-frequency noise and stabilize the circuit.



Typical waveforms:





Q6 **(b) Define Op-amp parameters: Gain, CMRR, Slew rate, Input resistance.**

• Open-loop Gain (A_OL): Ratio of output voltage to the differential input voltage with no feedback. Very large (10^5–10^6). Closed-loop gain is set by external resistors.

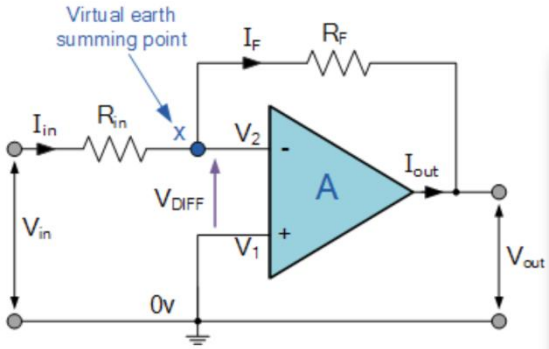
• CMRR (Common-Mode Rejection Ratio): The ability to reject signals common to both inputs. CMRR = Ad/Ac; usually expressed in dB as 20·log10(CMRR). Higher is better.

• Slew Rate (SR): Maximum rate of change of the output, SR = dVout/dt (V/µs). Limits large-signal speed.

• Input Resistance (Rin): Equivalent resistance seen at each input; ideally infinite. High Rin means very small input current (bias current).

Q6 (c) Explain Inverting Amplifier.

In the inverting amplifier, Vin is applied through Rin to the inverting input; the non-inverting input is grounded. Negative feedback via Rf forces the inverting node to a virtual ground (V−≈ 0). The ideal gain is Av = Vout/Vin = −Rf/Rin; input resistance = Rin; output is 180° out of phase with input.



Q7 **(a) Express F = A + BC as a sum of minterms.**

We convert F = A + BC into canonical SOP (sum of minterms) using a truth table and indexing.

Step 1 — Truth Table

A	B	C	BC	F = A + BC	Index (ABC)
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	2
0	1	1	1	1	3
1	0	0	0	1	4
1	0	1	0	1	5
1	1	0	0	1	6
1	1	1	1	1	7

Step 2 — Rows where F=1
Indices: 3, 4, 5, 6, 7.

Step 3 — Corresponding Minterms
Index 3 (A,B,C=0,1,1): m3 = A' B C

Index 4 (1,0,0): m4 = A B' C'

Index 5 (1,0,1): m5 = A B' C

Index 6 (1,1,0): m6 = A B C'

Index 7 (1,1,1): m7 = A B C

Step 4 — Canonical SOP (Sum of Minterms)
F(A,B,C) = Σ m(3,4,5,6,7)

= A'BC + AB'C' + AB'C + ABC' + ABC

Q7 (b) How NAND and NOR are universal gates.

NAND universality:

NOT X = X NAND X;

AND = (X NAND Y) NAND (X NAND Y);

OR = (X NAND X) NAND (Y NAND Y).

Similarly for NOR: NOT X = X NOR X;

OR = (X NOR Y) NOR (X NOR Y);

AND = (X NOR X) NOR (Y NOR Y).

Since NOT, AND, OR form a functionally complete set, NAND and NOR alone can realize any Boolean function.

Q7 (c) Axiomatic definition of Boolean Algebra.

A Boolean algebra is a set B with two binary operations (+,·), a unary complement (′), and two distinguished elements 0 and 1, such that for all x,y,z ∈ B:

(1) Closure under + and ·.

(2) Commutativity: x+y=y+x, x·y=y·x.

(3) Associativity: x+(y+z)=(x+y)+z, x·(y·z)=(x·y)·z.

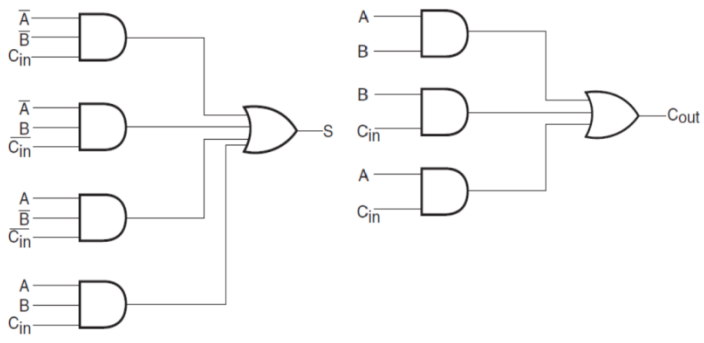
(4) Distributivity: x·(y+z)=x·y+x·z and x+(y·z)=(x+y)·(x+z).

(5) Identities: x+0=x, x·1=x.

(6) Complements: x+x′=1, x·x′=0. From these, other theorems (idempotence, De Morgan's laws, etc.) follow.

Q8 (a) Working of a Full Adder using basic gates.

A full adder adds A, B, and Cin. Sum S = A ⊕ B ⊕ Cin. Carry-out Cout = AB + BCin + ACin. Implementation: two half adders (HA1 forms S1 and C1 from A,B; HA2 forms final S from S1 and Cin) and an OR combining C1 and HA2 carry.



Q8(b) SOP vs POS — Definitions and Examples

1) Key Ideas:

- Minterm (canonical product term): AND of all variables (each in true or complemented form). It is 1 for exactly one row of the truth table. For variables (X,Y,Z), index a minterm by the binary row XYZ: m5 (binary 101) = X Y' Z.
- Maxterm (canonical sum term): OR of all variables (each in true or complemented form). It is 0 for exactly one row. For row (101): M5 = X' + Y + Z'.

Mapping rule: For mintermm_i: bit 1 → variable uncomplemented, bit 0 → complemented. For maxterm M_i: bit 1 → complemented, bit 0 → uncomplemented (opposite of minterms).

2) SOP (Sum of Products): OR of product terms. Canonical SOP: sum of all minterms for which F=1.

Example: For F=1 at rows 001, 011, 101, 111 → indices 1,3,5,7:

F(X,Y,Z) = Σ m(1,3,5,7) = X'Y'Z + X'YZ + XY'Z + XYZ.

3) POS (Product of Sums): AND of sum terms. Canonical POS: product of all maxterms for which F=0.

Example: Zeros at indices 0,2,4,6:

F = Π M(0,2,4,6) = (X+Y+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y+Z').

Tip: Σ m(ones) ↔ Π M(zeros), where the sets are complements in the index range.

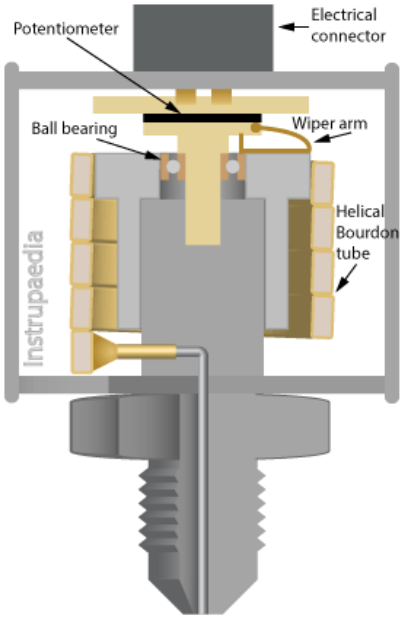
Q8(c) Converting F = XY + $\bar{X}$Z to Product of Maxterms

Method 1 — From truth table:

Truth table:

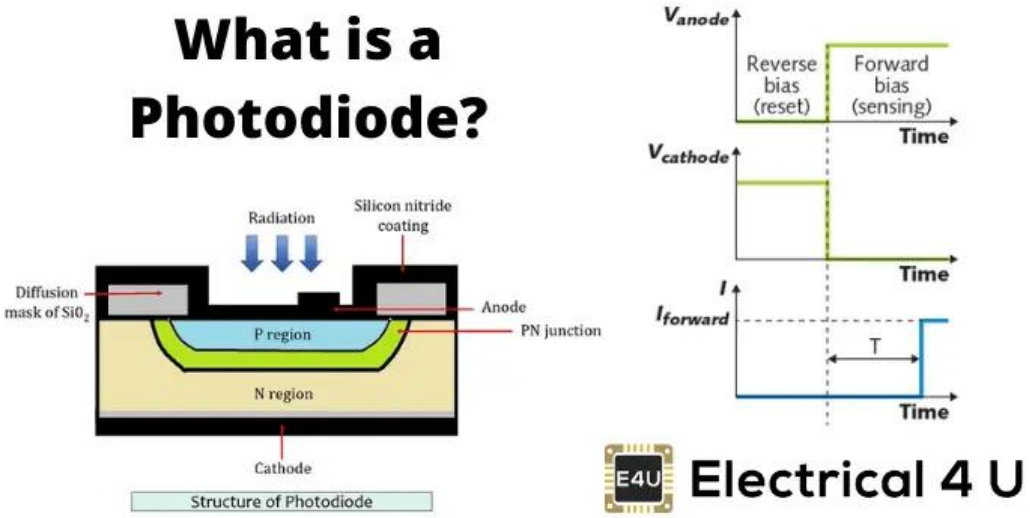
X	**Y**	**Z**	**Index**	**F = XY + $\bar{X}$Z**
0	0	0	0	0
0	0	1	1	1
0	1	0	2	0
0	1	1	3	1
1	0	0	4	0
1	0	1	5	0
1	1	0	6	1
1	1	1	7	1

Zeros at indices 0,2,4,5 → Maxterms:
M0 (000): (X+Y+Z)
M2 (010): (X+Y'+Z)
M4 (100): (X'+Y+Z)
M5 (101): (X'+Y+Z')
Canonical POS: F = Π M(0,2,4,5) = (X+Y+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y+Z').
Method 2 — Algebraic factoring:
XY + X'Z = (X+Z)(X'+Y) [consensus identity].
Convert each to canonical form:
(X+Z) = (X+Y+Z)(X+Y'+Z)
(X'+Y) = (X'+Y+Z)(X'+Y+Z')
Multiply: (X+Y+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y+Z') — same as Method 1.
Simplified POS (non-canonical): (X+Z)(X'+Y).
Q9 (a) Working of a Potentiometer-type Transducer.



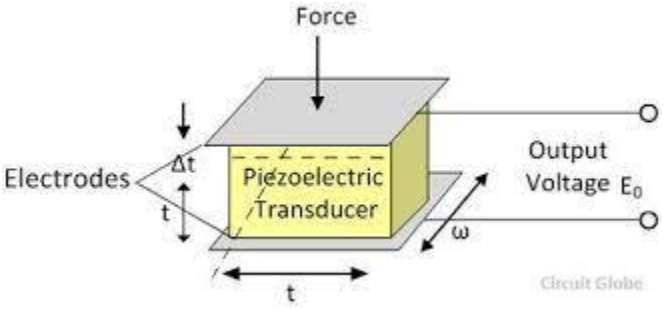
A resistive track of length L is excited by Vs. A wiper linked to displacement x taps a fraction of the voltage: Vout = (x/L)·Vs (linear pot) or proportional to angle (rotary pot). It is simple, low-cost, and suitable for static and dynamic displacement. Errors arise from wear, noise at the wiper, and loading (finite input resistance of the measuring circuit). Resolution depends on track granularity.

Q9 (b) Note on Photodiodes.



A photodiode is a PN/PIN/Avalanche junction operated under reverse bias; incident photons create electron–hole pairs, producing a photocurrent nearly proportional to optical power. Key relations: I = Idark + RP (A/W×W). PIN structure gives fast response; APD provides internal gain. Used in optical receivers, light meters, encoders.

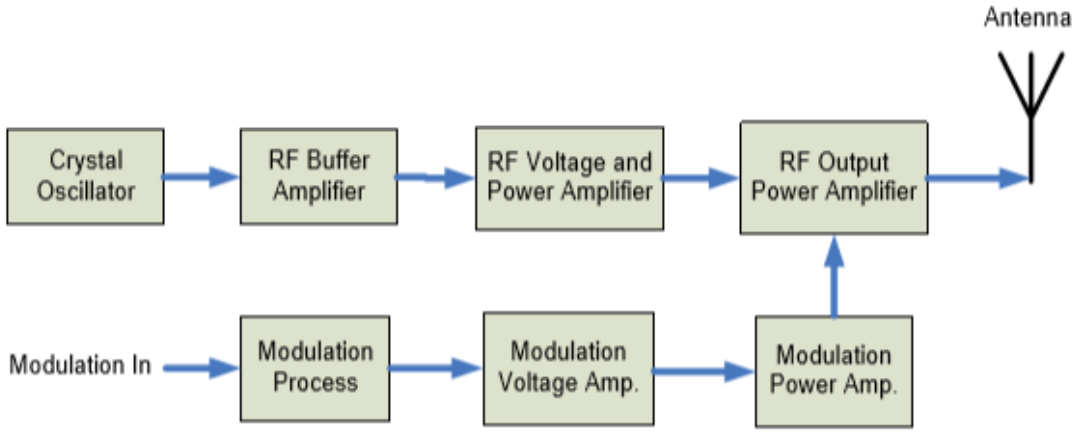
Q9 (c) Piezoelectric Transducer



Certain crystals (quartz, PZT) generate charge when stressed: Q = d·F, where d is the piezoelectric coefficient. The output voltage is V = Q/C. Equivalent circuit is a charge source in parallel with capacitance and large resistance; hence unsuitable for true DC/static measurement but excellent for dynamic pressure/acceleration/ultrasound. Needs high-impedance amplifier/charge amplifier.

Q10 (a) Typical Radio Transmitter.

Blocks: Audio/Baseband source → Audio processing/AF amplifier → Modulator (AM/FM/PM) driven by RF carrier oscillator → RF chain (buffer/driver/power amplifier) → Matching network/antenna. For superheterodyne-style upconversion, an IF stage and mixer may be inserted before the PA.



Q10 (b) What is modulation? Need for modulation.

Modulation is the process of varying a high-frequency carrier by the baseband signal (amplitude, frequency, or phase). Need: (1) Practical antenna size ($\lambda/4$ at carrier) (2) Long-distance propagation and multiplexing (sharing spectrum) (3) Improved noise/interference immunity and selectivity (4) Frequency translation of baseband to assigned RF channel (5) Power efficiency and manageable radiation.

Q10 (c) Working of LVDT.

An AC-excited primary couples to two identical secondary coils connected in opposition. With the core centered (null), V1≈V2 so Vo≈0. Displacing the ferromagnetic core increases coupling to one secondary and decreases the other; the differential output Vo = V2 − V1 is proportional to displacement and its phase indicates direction. Highly linear over a central range; frictionless; requires AC excitation and demodulation.

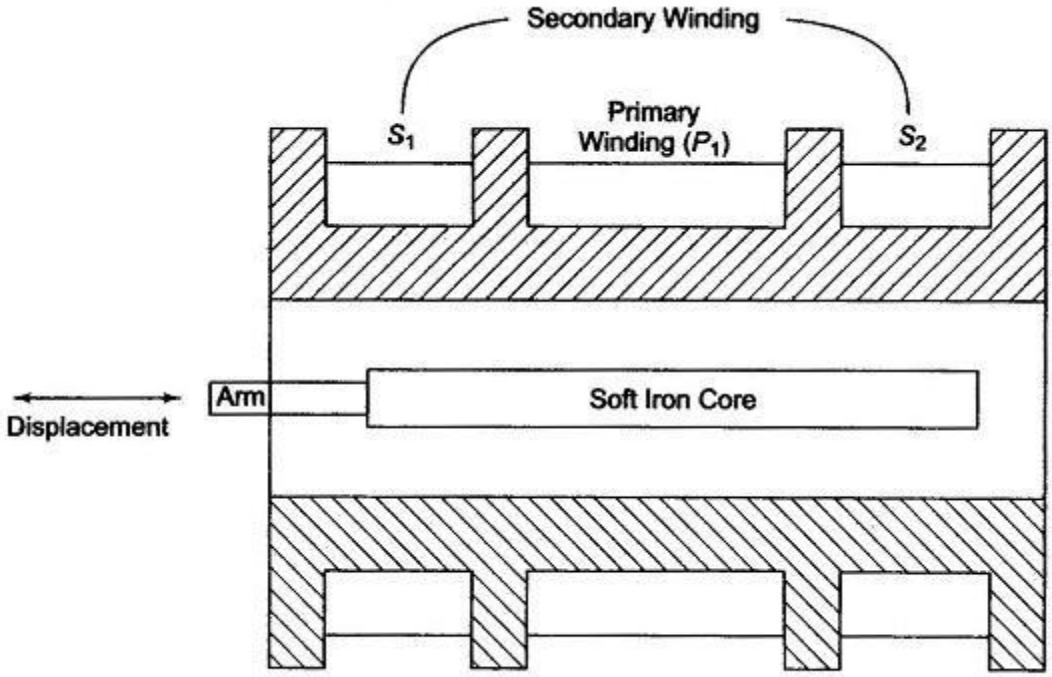


Fig. 13.19 Construction of a Linear Variable Differential Transducer (LVDT)