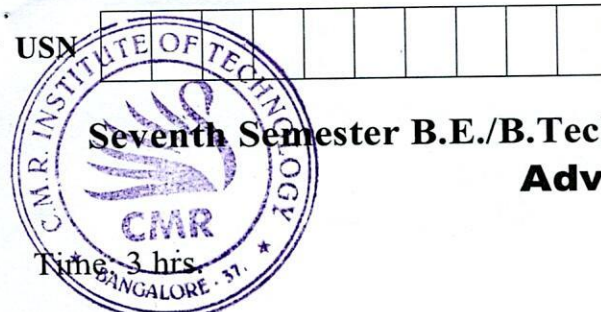




Seventh Semester B.E./B.Tech. Degree Examination, June/July 2025 Advanced VLSI

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat flow diagram, explain the steps involved in ASIC design. (10 Marks)
- b. With neat diagram, explain the following :
 - i) Programmable logic devices
 - ii) Structured gate arrays. (10 Marks)

OR

- 2 a. With relevant diagram and equations, explain the conventional ripple carry adder. Mention its limitations. (10 Marks)
- b. Explain the following:
 - i) I/O cells
 - ii) Cell compilers. (10 Marks)

Module-2

- 3 a. Explain the measurement of delay in floor planning. (10 Marks)
- b. Briefly explain the following:
 - i) Goals and objectives of placement
 - ii) Timing driven placement method. (10 Marks)

OR

- 4 a. Explain physical design flow with respect to placement. (10 Marks)
- b. Explain global routing between blocks. (10 Marks)

Module-3

- 5 a. Explain the verification process with an example. (10 Marks)
- b. Discuss direct testing method and its limitations in system verilog. (10 Marks)

OR

- 6 a. Describe fixed size arrays with an example. (08 Marks)
- b. Explain dynamic arrays with sample code. (06 Marks)
- c. Explain array reduction methods and array locator methods. (06 Marks)

Module-4

- 7 a. Explain tasks, functions and void functions in system verilog. (10 Marks)
- b. Explain time values in system verilog. (10 Marks)

OR

- 8 a. List the interface tradeoffs in system verilog. (08 Marks)
- b. Explain system verilog assertions. (12 Marks)

Module-5

- 9 a. What is Randomization? Explain all design inputs in detail for randomization. (10 Marks)
- b. Explain in detail about iterative and array constraints. (10 Marks)

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- 10 a. Describe various functional coverage strategies in detail. (10 Marks)
- b. Discuss various carriage options with an example. (10 Marks)

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