CBCS SCHEME

USN | | | | | | | | | | 18EC72

Seventh Semester B.E./B.Tech. Degree Examination, June/July 2025
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain DC transfer characteristics of CMOS inverter high lighting the regions of operation. Comment on the current flowing through the inverter. **(10 Marks)**

b. Derive an expression for drain current of enhancement mode nMOS transistor operating in linear and saturation regions. **(10 Marks)**

OR

2 a. Explain in detail non ideal I-V effects :
i) Mobility degradation
ii) Velocity saturation
iii) Channel length modulation. **(06 Marks)**

b. Explain the operation of MOS capacitor. **(06 Marks)**

c. Explain the operation of nMOS enhancement mode transistor for different values of V_{gs} and V_{ds}. Explain the VI characteristics. **(08 Marks)**

Module-2

3 a. Describe in detail step by step procedure involved in the fabrication of CMOS inverter using n-well process. **(12 Marks)**

b. Compare the two technology scaling methods. Show analytically by using equations how power dissipation and power density are affected in terms of scaling factor S. **(08 Marks)**

OR

4 a. Explain the following :
i) Photolithography
ii) Water formation with neat diagrams. **(08 Marks)**

b. Explain different methods of oxidation. **(06 Marks)**

c. Draw the circuit and stick diagram for $Y = \overline{(A+B+C)} \cdot D$. **(06 Marks)**

Module-3

5 a. Estimate the minimum delay of the path from A to B in Fig.Q5(a) and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and output load is equivalent to 45 λ of transistor width. Find x, y.

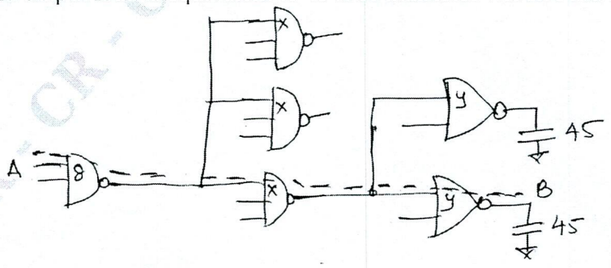

Fig.Q5(a) **(10 Marks)**

b. Explain layout dependence of capacitance. **(04 Marks)**

c. Explain with neat diagrams : i) Pseudo nMOS logic ii) CVSL. **(06 Marks)**

OR

6 a. Estimate tpdf and tpdr for a 3-i/p NAND gate if the output is loaded with h identical NAND gates. Transistor widths are chosen to achieve effective rise and fall resistance equal to that of a unit inverter. Consider the worst –case rising output transition. **(08 Marks)**

b. What do you mean by skewed gates? Compute the average logical effort to Hi-skewed and low-skewed inverter and 2-input NAND gate. **(12 Marks)**

Module-4

7 a. Derive the expressions for fall time during logic '0' transfer and time during logic '1' transfer when an nMOS pass transistor drives the gate of another nMOS transistor. Calculate the fall time of soft node voltage. **(10 Marks)**

b. Explain dynamic passtransistor circuits :
i) Depletion load nMOS dynamic shift register circuit
ii) CMOS transmission gate dynamic shift register. **(10 Marks)**

OR

8 a. Explain the operation of conventional CMOS latches and flip-flops. Discuss about their advantages and limitations. **(10 Marks)**

b. Explain the principle and operation of dynamic CMOS logic. What are its advantages and limitations. **(10 Marks)**

Module-5

9 a. Explain different types of refresh operations in DRAM. **(06 Marks)**

b. Write a note on testing and testability. **(08 Marks)**

c. Define observability, controllability and fault coverage. **(06 Marks)**

OR

10 a. Explain full CMOS SRAM cell with data read and write operations. **(08 Marks)**

b. Explain different kinds of physical faults that can occur on a CMOS chip and relate them to typical circuit failures. **(08 Marks)**

c. Explain the components of current that contribute to leakage currents in DRAM. **(04 Marks)**

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