CBCS SCHEME

USN

BEC602

Sixth Semester B.E/B.Tech. Degree Examination, June/July 2025
VLSI Design and Testing

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Compare CMOS and NMOS logic.	5	L3	CO1
	b.	With neat diagram, explain the physical representation of transmission gate.	5	L2	CO1
	c.	Design CMOS compound gate for the functions : i) $Y = \overline{A(B+C)+DE}$ ii) $Y = \overline{A}B + A\overline{B}$.	10	L3	CO1
		OR			
2	a.	Design D-flip-flop using transmission gates and explain its operation with necessary conditions on LD input.	7	L3	CO1
	b.	Illustrate different alternate circuit representations used in digital circuit designs with an example for each.	6	L2	CO1
	c.	With a neat diagram, explain the physical representation of CMOS inverter.	7	L2	CO1
		Module – 2			
3	a.	With neat diagram, explain the working of nMOS enhancement mode transistor under various voltage conditions.	6	L2	CO2
	b.	How does body effect influences threshold voltage? What are the design strategies to minimize body effect?	6	L2	CO2
	c.	For an nMOSFET, derive the equation for drain current in linear and saturation region.	8	L3	CO2
		OR			
4	a.	Explain the working of pseudo nMOS inverter. Find the output voltage equation for pseudo nMOS inverter.	6	L3	CO2
	b.	Find the expression for V_{out} in region C of CMOS inverter transfer characteristics.	8	L3	CO2
	c.	Illustrate with suitable sketch, latup phenomenon in CMOS circuits and also explain its prevention.	6	L2	CO2
		Module – 3			
5	a.	Illustrate with neat diagram wafer processing and selective diffusion.	6	L2	CO3
	b.	Derive the equation for rise time, fall time and delay time.	8	L3	CO3
	c.	Explain with neat diagram, the process flow of fabricating inverter (CMOS) using Twin-tub process.	6	L2	CO3

		OR			
6	a.	What is sheet resistance? Estimate the sheet resistance for a given layer having length 'L' and width 'W'.	7	L4	CO3
	b.	Explain the various capacitances in MOS transistor.	6	L2	CO3
	c.	Estimate the total capacitance for the structure as shown in below Fig.Q6(c).	7	L4	CO3

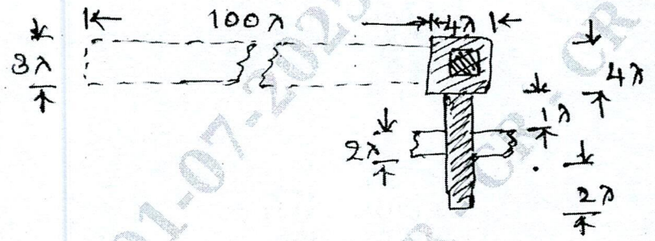

Fig.Q6(c)

		Module – 4			
7	a.	Differentiate static and dynamic CMOS circuit with relevant diagrams.	7	L3	CO4
	b.	Explain the percharge and evaluate phase in dynamic logic.	6	L2	CO4
	c.	Design a CVSL (Cascade Voltage Switch Logic) based XOR gate.	7	L3	CO4
		OR			
8	a.	Design a 2 : 1 multiplexer using pass transistor logic.	7	L3	CO4
	b.	Draw and explain the layout diagram of a 2 input NAND gate.	6	L2	CO4
	c.	Design a schematic and layout for $Z = \overline{(A+B+CD)}$ using Euler's graph.	7	L3	CO4
		Module – 5			
9	a.	With appropriate neat diagram of two inverter bistable element, explain in detail the voltage transfer characteristics (VTC) and potential energy analogy.	7	L2	CO5
	b.	Explain the operation of SR latch using CMOS NAND2 gates and switch level diagram.	6	L2	CO5
	c.	With neat appropriate diagrams, explain the clocked JK – Latch using NOR2 gates.	7	L2	CO5
		OR			
10	a.	What is structured design strategy? Explain the factors modularity, regularity and locality.	7	L2	CO5
	b.	Distinguish self-test and built-in test with examples.	6	L3	CO5
	c.	Explain with neat diagram, Gate Array Design flow.	7	L2	CO5

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