CBCS SCHEME

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18EC56

Fifth Semester B.E. Degree Examination, June/July 2025
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain design hierarchy using 4 bit ripple carry counter. **(10 Marks)**
b. Explain different levels of abstractions used in programming in verilog. **(06 Marks)**
c. Explain trends in HDL language. **(04 Marks)**

OR

2 a. Explain typical design flow for designing VLSI IC circuits with neat block diagram. **(08 Marks)**
b. Explain following components in simulation.
i) Design block
ii) Stimulus block **(06 Marks)**
c. Explain topdown and bottom up design methodology with suitable example. **(06 Marks)**

Module-2

3 a. Explain port connecting rules. **(08 Marks)**
b. What are operators? Classify and explain with an example. **(08 Marks)**
c. Explain any two compiler directives in VHDL **(04 Marks)**

OR

4 a. With neat block diagram explain components of verilog module. **(08 Marks)**
b. What are data types in verilog? Explain following data types with example.
i) Nets ii) Parameters iii) array iv) memory **(08 Marks)**
c. List all lexical. Conventions used in verilog and explain with examples. **(04 Marks)**

Module-3

5 a. Describe rise, full and turnoff delays in gate level description and also explain min/max. and typical delay of each type. **(08 Marks)**
b. Construct XOR modules using AND/NOT/OR gates. Write stimulus that exercises all four combination. **(08 Marks)**
c. Explain following primitives used in verilog HDL with truth table.
i) buf if
ii) notif **(04Marks)**

OR

6 a. Explain assignment delay, implicit assignment delay and net declaration delay for continuous assignment statements with an example. **(08 Marks)**
b. Create your own two input verilog gates called my –or, my-and and my-not form two input nand gates. (but) functionality of these gates with stimulus module. **(06 Marks)**
c. Full substractor has three one bit inputs. x, y and z (previous borrow) and two one bit output. "D" (difference and BC barrow). The logic equation for 'D' and 'B' are given below.
Write verilog code for full substractor module including I/O ports.
$D=\bar{x}\,\bar{y}z+\bar{x}\,y\,\bar{z}+x\,\bar{y}\,\bar{z}+xyz$
$B=\bar{x}y+\bar{x}\,z+yz$ **(06 Marks)**

Module-4

7 a. What is difference between functions and task. **(06 Marks)**
b. Write a programme for 2:4 priority encoder using casex. **(06 Marks)**
c. Explain blocking and non blocking assignment statements with suitable examples. **(08 Marks)**

OR

8 a. Explain sequential and parallel blocks with suitable examples. **(08 Marks)**
b. Explain different types of event based timing control in verilog **(06 Marks)**
c. Write a programme for 4:1 mux using if else structure. **(06 Marks)**

Module-5

9 a. Explain conditional compilation and Execution. **(06 Marks)**
b. Using assign and deassign statements design a positive edge triggered D – Flip Flop with asynchronous clear and preset. **(08 Marks)**
c. Write a note on over riding of parameters. **(06 Marks)**

OR

10 a. Explain impact of logic synthesis as verilog. **(06 Marks)**
b. With neat diagram explain synthesis design flow. **(08 Marks)**
c. Explain verilog HDL synthesis process. **(06 Marks)**

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