CBCS SCHEME

USN | | | | | | | | | | 18EC42

Fourth Semester B.E./B.Tech. Degree Examination, June/July 2025
Analog Circuits

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the design constraints of a classical discrete – circuit biasing arrangement with circuit and relevant equations. How does R_E provide a negative feedback action to stabilize the bias current? **(10 Marks)**

b. Design biasing using a collector to base feedback resistor to obtain a DC current of 1mA at the collector. Assume $V_{CC} = 10V$, $V_{CE} = 2.3V$ and $\beta = 100$. **(07 Marks)**

c. Mention any three the advantages of MOSFET compared to BJT. **(03 Marks)**

OR

2 a. Explain the following biasing scheme of MOS circuits :
i) Biasing by fixing V_{GS}
ii) Biasing by fixing V_G and connecting a resistance at the source. **(10 Marks)**

b. For the circuit shown in Fig.Q2(b), find the value of V_{GS} to establish a DC bias current of $I_D = 0.5mA$. Device parameters are $V_t = 1V$, $K_n' \frac{W}{L} = 1mA/V^2$ and $\lambda = 0$. What is the % change in I_D obtained when the transistor is replaced with another having $V_t = 1.5V$.

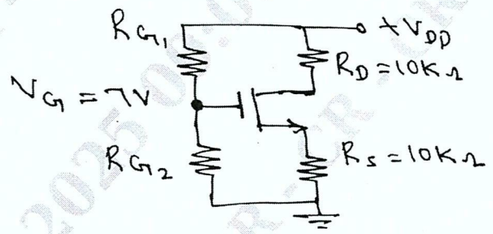

Fig.Q2(b) **(10 Marks)**

Module-2

3 a. What are the basic configurations for connecting the MOSFET as an amplifier and explain them. **(08 Marks)**

b. With the help of AC equivalent circuit, derive the expressions for R_{in}, Av_0, R_0 and G_v for a common source amplifier without R_S. **(12 Marks)**

OR

4 a. Explain the various internal capacitances in the MOSFET with necessary equations. **(08 Marks)**

b. Design a self biased phase shift oscillator using FET having $g_m = 500\ \mu s$, $r_d = 40\ K\Omega$ and a feedback network value of R = 10 KΩ. What should be the value of 'C' for sustained oscillation at 5 KHz and R_D for A > 29? **(08 Marks)**

c. Mention the features of source follower. **(04 Marks)**

Module-3

5 a. With mathematical analysis, show how gain can be desensitized and bandwidth is increased with negative feedback. **(07 Marks)**

b. For the block diagram shown in Fig.Q5(b), a signal of 1V from the source results in a difference signal of 10 MV being provided to the amplifying element (A) and 10V applied to the load. For this arrangement, identify the value of A and B that apply.

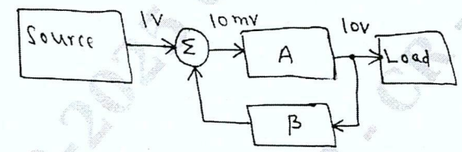

Fig.Q5(b) **(08 Marks)**

c. Draw the block diagram of series shunt feedback amplifier and also mention the effect of R_{if}, R_{of}. **(05 Marks)**

OR

6 a. Explain the classification of output stage based on the Q-point. **(08 Marks)**

b. Explain the working of class – B output stage. Prove that maximum conversion efficiency is 78.5%. **(08 Marks)**

c. Mention the advantages of class – C output stage. **(04 Marks)**

Module-4

7 a. Derive the expressions of Exact voltage gain, input resistance with feedback and output resistance with feedback of non-inverting amplifiers. **(12 Marks)**

b. For the inverting amplifier $R_1 = 470\ \Omega$ and $R_F = 4.7K\Omega$. Assume A = 200000, $R_i = 2\ M\Omega$, $R_0 = 75\ \Omega$ and $f_0 = 5$ Hz. Calculate A_F, R_{iF}, R_{0F} and f_F. **(08 Marks)**

OR

8 a. Explain the working of instrumentation amplifier using transducer bridge and also derive the expression of output voltage. **(12 Marks)**

b. Explain the working of a Schmitt trigger with necessary input and output waveforms. **(08 Marks)**

Module-5

9 a. Derive the output voltage expression $V_0 = -V_R \frac{R_F}{R}(b_0 + 2b_1 + 4b_2 + 8b_3)$. **(08 Marks)**

b. For the DAC using R – 2R network with R = 10 KΩ and $V_R = 5$ V.
i) Determine the size of each step if $R_F = 27\ K\Omega$
ii) Calculate the output voltage when the inputs b_0, b_1, b_2 and b_3 are at 5V. **(06 Marks)**

c. Explain the working of non–inverting type small signal half wave rectifier. **(06 Marks)**

OR

10 a. What are the advantages of active filters? **(04 Marks)**

b. Explain the working of a First Order Active High Pass Filter with necessary circuit and waveforms. **(08 Marks)**

c. In the Astable Multivibrator using 555 Timer $R_A = 2.2\ K\Omega$, $R_B = 3.9K\Omega$ and $C = 0.1\ \mu F$. Determine : i) t_c ii) t_d iii) free running frequency iv) Duty cycle. **(08 Marks)**

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