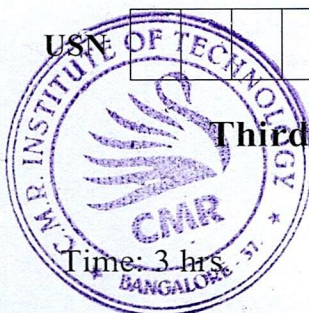




Third Semester B.E. Degree Examination, June/July 2025
Digital System Design

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Define combinational logic. What are SOP and POS expressions? Explain with an example. (08 Marks)
- b. Convert the following incomplete canonical form of expressions into canonical form of expressions :
 - (i) $P = f(a, b, c) = \bar{b}c + a\bar{b}$
 - (ii) $Q = f(x, y, z) = (x + \bar{y}).(\bar{x} + \bar{z})$ (06 Marks)
- c. Simplify the equation, $y = \bar{a}bcd + a\bar{b}cd + abcd + abcd + a\bar{b}cd + a\bar{b}cd + abcd$ using K-map method. (06 Marks)

OR

- 2 a. Simplify $P = f(a, b, c, d) = \sum(0, 1, 4, 5, 6, 8, 9, 12) + dm(2, 10, 14, 15)$ using K-map method and draw the logic diagram for obtained expression. (10 Marks)
- b. Simplify $A = f(w, x, y, z) = \prod M(2, 5, 7, 10, 13, 14) + dm(0, 1, 4, 6, 9, 15)$ using K-map method and draw the logic circuit for obtained expression using NOR Gates. (10 Marks)

Module-2

- 3 a. Realize multiple O/P four variable function using 4 to 16 decoder with active low outputs.
 $S = f(a, b, c, d) = \sum(0, 2, 7, 14)$
 $T = f(a, b, c, d) = \sum m(1, 5, 12, 15)$ (10 Marks)
- b. Draw a PLA structure to implement the following functions :
 $f_1 = \bar{a}bd + a\bar{b}c + \bar{b}c$
 $f_2 = c + \bar{a}b\bar{d}$
 $f_3 = bc + \bar{a}b\bar{d}$ (10 Marks)

OR

- 4 a. Realize the function $T = f(w, x, y, z) = \sum m(0, 2, 3, 5, 8, 11, 14, 15)$ using 8 : 1 Mux. (10 Marks)
- b. Explain 4-bit carry look ahead adder with necessary diagrams and relevant expressions. (10 Marks)

Module-3

- 5 a. Explain the operation of JK-FF (Flip-flop) with the help of functional table and logic diagram. (10 Marks)
- b. What is race around condition and how it is over come? Explain with logic diagram. (10 Marks)

OR

- 6 a. Obtain the characteristic table and characteristic equation for SR-Flip-flop. (06 Marks)
- b. Explain 3-bit ripple up counter with the help of logic diagram and timing diagram. (10 Marks)
- c. Write the difference between combinational and sequential logic. (04 Marks)

Module-4

- 7 a. Design 2-bit synchronous up counter. (10 Marks)
- b. Explain state machine notations with an example. (10 Marks)

OR

- 8 a. Design MOD-6 synchronous counter using T-flip flops. (10 Marks)
- b. List the difference between Mealy and Moore model with necessary diagrams. (10 Marks)

Module-5

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- 9 a. Design a Mealy type sequence detector to detect the sequence of 101 in the given sequence of 0011011001010100 (10 Marks)
- b. Explain the operation of serial adder with the help of necessary diagrams. (10 Marks)

OR

- 10 a. Design a sequential circuit to convert BCD to Excess-3 code with state table, state graph and transition table. (12 Marks)
- b. Give CPLD implementation of a shift Register and Parallel adder with accumulator. (08 Marks)
