CBCS SCHEME

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BEC306C

Third Semester B.E/B.Tech. Degree Examination, June/July 2025
Computer Organization and Architecture

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	With a neat diagram, explain the basic operational concept of a computer.	10	L2	CO1
	b.	Explain the single bus structure of computers.	4	L2	CO1
	c.	What is an operating system? Explain the user program and OS routine sharing the processor.	6	L2	CO1
		OR			
2	a.	Define byte addressability, Big-endian and Little-endian assignments.	8	L2	CO1
	b.	With examples, explain : i) Three address ii) Two address iii) One address iv) Zero address instructions.	8	L2	CO1
	c.	Represent 85.125 in IEEE floating point single precision.	4	L2	CO1
		Module – 2			
3	a.	What do you mean by addressing mode? Explain : i) Indirect ii) Index iii) Base with index iv) Autoincrement addressing modes.	10	L2	CO2
	b.	Consider a database of marks scored by students in 3 tests, stored in memory starting at address LIST. Each student record consists of student ID followed by marks in 3 tests. Assume each of these to be 4 bytes in size. There are 50 students in the class and this value is stored at location NUM. i) Sketch the memory map showing all the details ii) Develop an ALP using indexed addressing mode to compute the sum of scores by all the students in Test-2 and store the result in location SUM. Write appropriate comments.	5	L3	CO2
	c.	Consider a register R1 to size 16-bit with initial data 5867d. With neat sketches, depict the output in each case, after performing the following operations. i) LShiftL #2, R1 ii) RotateR #1, R1.	5	L2	CO2

		OR			
4	a.	Explain shift and rotate instructions with examples.	**7**	**L2**	**CO2**
	b.	Consider a set of numbers (each 4 bytes in size) stored in memory starting at address TABLE. Total numbers are N and this value is stored at location LOCN. i) Sketch memory map showing all details ii) Develop an ALP using auto-increment addressing mode, to compute the sum of all numbers and store the result at memory address RESULT. Write appropriate comments.	**8**	**L3**	**CO2**
	c.	Explain any five assembler directives used in assembly language programming.	**5**	**L2**	**CO2**
		Module – 3			
5	a.	Showing the register details of the keyboard and display, write an ALP to demonstrate program – controlled I/O to read a line from the keyboard, store it in memory, and also echo it back to the display.	**10**	**L2**	**CO3**
	b.	What is an interrupt? With neat diagrams explain interrupt priority schemes.	**10**	**L2**	**CO3**
		OR			
6	a.	Using registers involved in a DMA interface, illustrate the operation of DMA.	**10**	**L2**	**CO3**
	b.	Define interrupts. Point out and explain various ways to enable and disable the interrupts.	**6**	**L2**	**CO3**
	c.	Explain the concept of vectored interrupts.	**4**	**L2**	**CO3**
		Module – 4			
7	a.	With a neat diagram, explain virtual memory organization.	**10**	**L2**	**CO4**
	b.	Explain any five non-volatile memory concepts.	**10**	**L2**	**CO4**
		OR			
8	a.	With diagram explain the internal organization of 2M × 8 dynamic memory chip.	**10**	**L2**	**CO4**
	b.	Explain the construction and working of a secondary storage device.	**10**	**L2**	**CO4**
		Module – 5			
9	a.	Explain the process of fetching a data word from memory using designated registers of the processor.	**10**	**L2**	**CO5**
	b.	Explain the following : i) Grating signal ii) Control word iii) Micro – routine iv) Control store.	**4**	**L2**	**CO5**
	c.	Give the actions required to execute the complete instruction ADD(R3), R1 using single bus organization.	**6**	**L2**	**CO5**
		OR			
10	a.	Explain the three-bus organization of a processor and its advantages.	**8**	**L2**	**CO5**
	b.	With a block diagram, explain the organization of a micro programmed control unit.	**8**	**L2**	**CO5**
	c.	Give the actions required to execute the complete instruction ADD R4, R5, R6 using three bus organization.	**4**	**L2**	**CO5**

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