Internal Assessment Test 2 –January 2025
SOLUTION

Sub:	Digital Design and Computer Organization					Sub Code:	BCS302	Branch:	CSE	
Date:		Duration:	90 minutes	Max Marks:	50	Sem / Sec:	III / A, B, C		OBE	

	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	a) Write a program that can evaluate the expression (A-B) + (C*D) using One, Two and Three address instruction?	[5]	3	L3

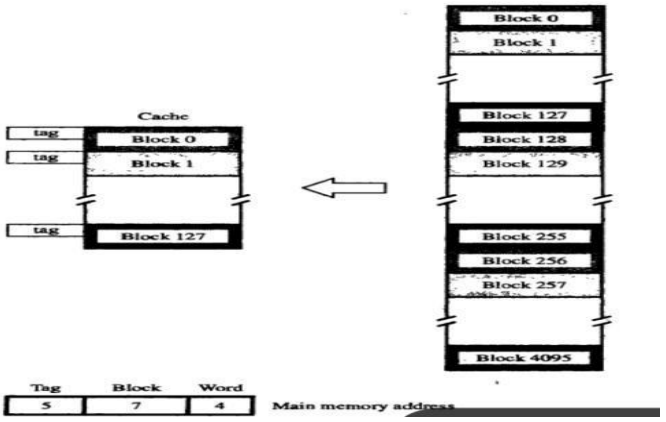
One address	Two address	Three address
LOAD A	MOV A, R1	SUB A, B, R1
SUB B	SUB B, R1	MUL C, D, R2
STORE T	MOV C, R2	ADD R1, R2, X
LOAD C	MUL D, R2	
MUL D	ADD R2, R1	
ADD T	MOV R1, X	
STORE X		

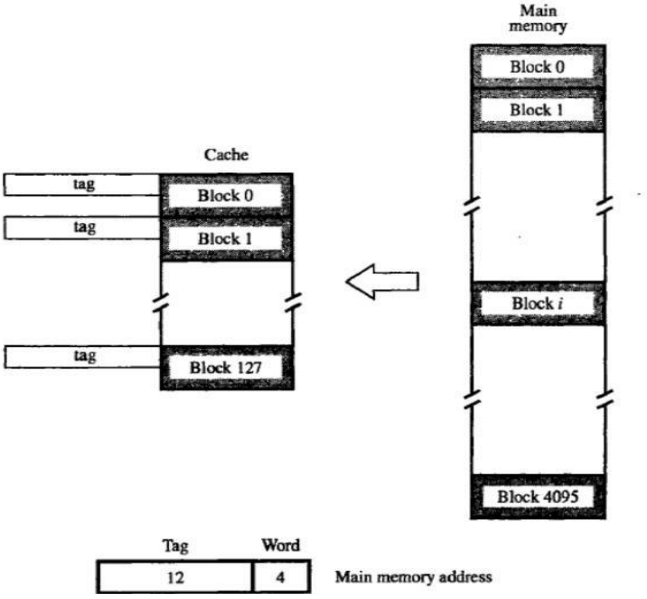
		[5]	3	L1

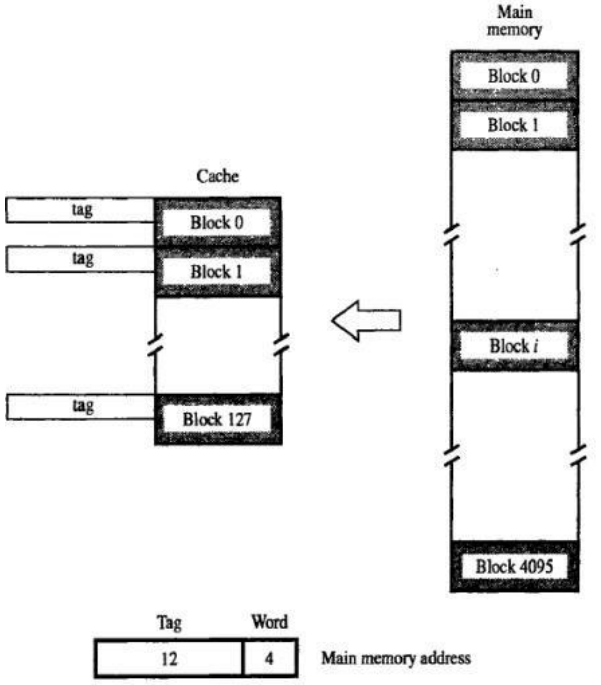
Name	Assembler syntax	Addressing function
Immediate	#Value	Operand = Value
Register	Ri	EA = Ri
Absolute (Direct)	LOC	EA = LOC
Indirect	(Ri) (LOC)	EA = [Ri] EA = [LOC]
Index	X(Ri)	EA = [Ri] + X
Base with index	(Ri,Rj)	EA = [Ri] + [Rj]
Base with index and offset	X(Ri,Rj)	EA = [Ri] + [Rj] + X
Relative	X(PC)	EA = [PC] + X
Autoincrement	(Ri)+	EA = [Ri]; Increment Ri
Autodecrement	−(Ri)	Decrement Ri; EA = [Ri]

EA = effective address
Value = a signed number

2	a) Explain different types of cache mapping functions with neat diagram? There are 3 techniques to map main memory blocks into cache memory – 1. Direct mapped cache 2. Associative Mapping 3. Set-Associative Mapping	[5]	4	L1


Cache
tag
Block 0
tag
Block 1
tag
Block 127
Block 0
Block 1
Block 127
Block 128
Block 129
Block 255
Block 256
Block 257
Block 4095
Tag
Block
Word
5
7
4
Main memory address


Main memory
Cache
tag
Block 0
tag
Block 1
tag
Block 127
Block 0
Block 1
Block i
Block 4095
Tag
Word
12
4
Main memory address


Main memory
Cache
tag
Block 0
tag
Block 1
tag
Block 127
Block 0
Block 1
Block i
Block 4095
Tag
Word
12
4
Main memory address

	b) Draw the memory hierarchy and explain in terms of size, speed and cost per bit?	[5]	4	L2

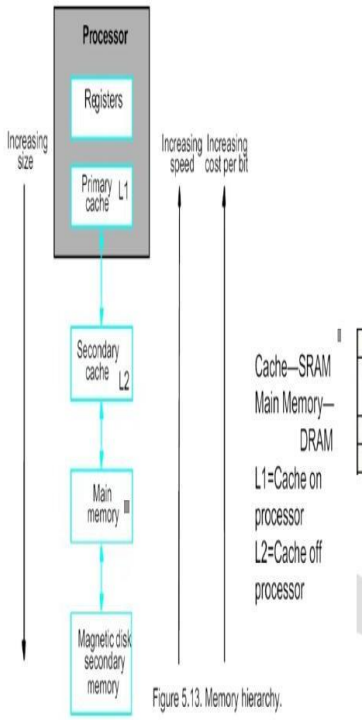


Figure 5.13. Memory hierarchy.

Cache–SRAM
Main Memory–DRAM
L1=Cache on processor
L2=Cache off processor

Characteristics	SRAM	DRAM	Magnetis Disk
Speed	Very Fast	Slower	Much slower than DRAM
Size	Large	Small	Small
Cost	Expensive	Less Expensive	Low price

Memory	Speed	Size
Registers	Very high	Lower
Primary cache	High	Lower
Secondary cache	Low	Low
Main memory	Lower than Seconadry cache	High
Secondary Memory	Very low	Very High

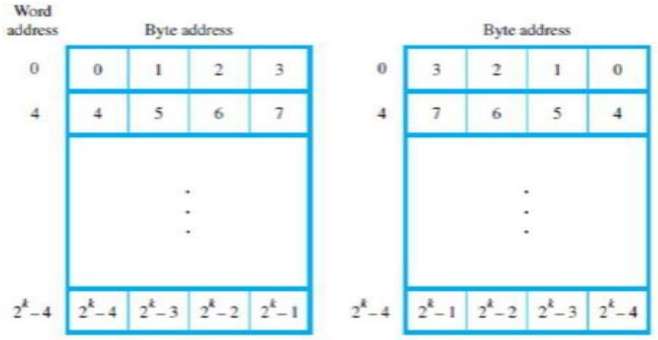
3	(a)Explain the following (a) byte addressability (b) Big-endian assignment(c) Little –endian assignment.	[5]	3	L1

BYTE-ADDRESSABILITY:

- We have three basic information quantities to deal with: **bit, byte, and word.**
- A byte is always 8 bits, but the word length typically ranges from 16 to 64 bits.
- It is impractical to assign distinct addresses to individual bit locations in the memory.
- The most practical assignment is to have successive addresses refer to successive byte locations in the memory.
- This is the assignment used in most modern computers.
- The term byte-addressable memory is used for this assignment.
- Byte locations have addresses 0, 1, 2,.... Thus, if the word length of the machine is 32 bits, successive words are located at addresses 0, 4, 8,..., with each word consisting of four bytes.

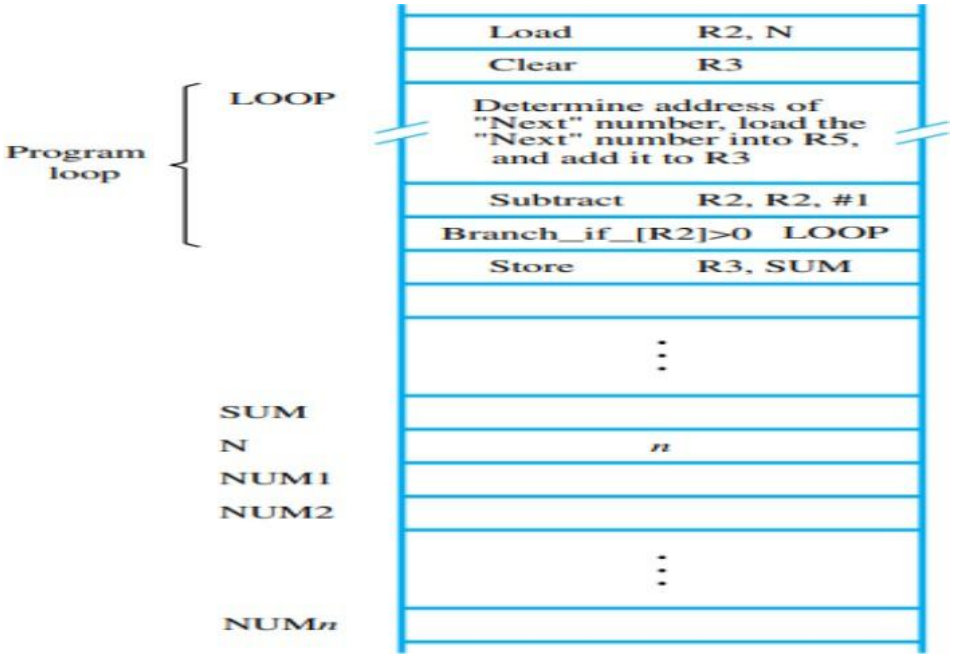
BIG-ENDIAN & LITTLE-ENDIAN ASSIGNMENTS

- There are two ways in which byte-addresses are arranged (Figure 2.3).
  1) **Big-Endian:** Lower byte-addresses are used for the more significant bytes of the word.
  2) **Little-Endian:** Lower byte-addresses are used for the less significant bytes of the word
- In both cases, byte-addresses 0, 4, 8. . . . . are taken as the addresses of successive words in the memory.



(a) Big-endian assignment (b) Little-endian assignment

(b)Explain the concept of Branch Instruction? [5] 3 L1



4 Explain the concept of (a) Register Transfer Notation (b) Fetching word from memory? [5+5] 5 L1

REGISTER TRANSFER NOTATION (RTN)

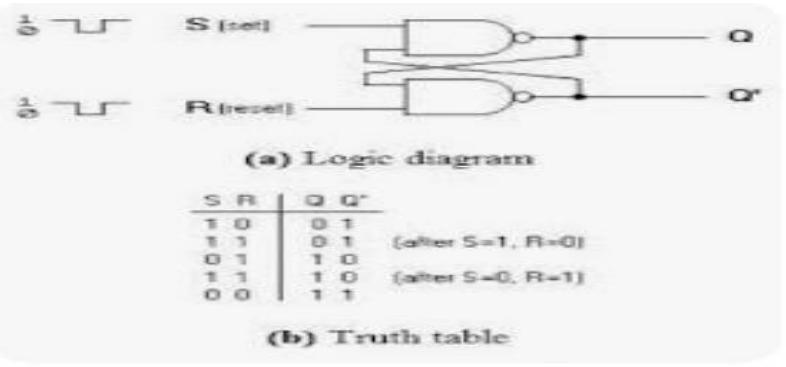
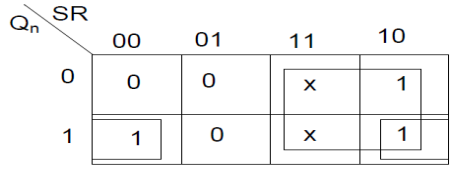
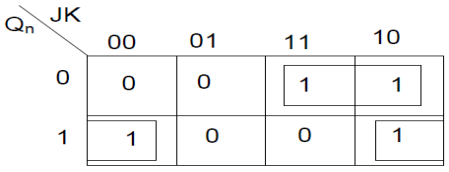
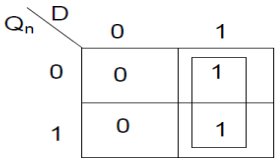
- The possible locations in which transfer of information occurs are: 1) Memory-location 2) Processor register & 3) Registers in I/O device.

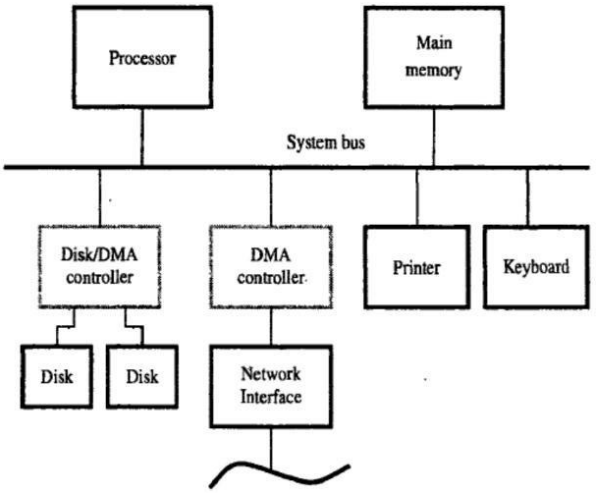
Location	Hardware Binary Address	Example	Description
Memory	LOC, PLACE, NUM	R1 ← [LOC]	Contents of memory-location LOC are transferred into register R1.
Processor	R0, R1 ,R2	[R3] ← [R1]+[R2]	Add the contents of register R1 &R2 and places their sum into R3.
I/O Registers	DATAIN, DATAOUT	R1 ← DATAIN	Contents of I/O register DATAIN are transferred into register R1.

ASSEMBLY LANGUAGE NOTATION

- To represent machine instructions and programs, assembly language format is used.

Assembly Language Format	Description
Move LOC, R1	Transfer data from memory-location LOC to register R1. The contents of LOC are unchanged by the execution of this instruction, but the old contents of register R1 are overwritten.
Add R1, R2, R3	Add the contents of registers R1 and R2, and places their sum into register R3.

5	a) Explain S-R latch using NAND Gate with a neat diagram and truth table? Positive edges occur at t_0,t_1,t_2,t_3 and t_4. At t_0, S=0 and R=0, hence no change in the output and Q=0. At t_1, S=1 and R=0, hence the output is set and Q=1. At t_2, S=0 and R=1, hence the output is reset and Q=0. At t_3, S=1 and R=0, hence the output is set and Q=1 At t_4, S=0 and R=0, hence no change in the output and Q=1.  (a) Logic diagram S R | Q Q' 1 0 | 0 1 1 1 | 0 1 (after S=1, R=0) 0 1 | 1 0 1 1 | 1 0 (after S=0, R=1) 0 0 | 1 1 (b) Truth table	[5]	2	L1
	b) Derive the characteristic equation of SR, JK and D flip flops?  Characteristic Equation for SR flip flop is $Q_{n+1}=S+\overline{R}Q_n$  Characteristic Equation for JK flip flop is $Q_{n+1}=J\overline{Q}_n+\overline{K}Q_n$  Characteristic Equation for D flip flop is $Q_{n+1}=D$	[5]	2	L3
6	a) Explain DMA with a neat diagram. The DMA controller connects two external devices namely disk 1 and disk 2 to system bus asshown in the above fig. ¯ The DMA controller also interconnects high speed network devices to system bus as shownin the above fig. ¯ Let us consider direct data transfer operation by means of DMA controller without the involvement of CPU in between main memory and disk 1 as indicated by dotted lines (in the fig.). ¯ To establish direct data transfer operation between main memory and disk 1. DMA controller request the processor to obtain 3 parameters namely: 1) Starting address of the memory block. 2) No of words to be transferred. 3) Type of operation (Read or Write).	[5+5]	4 4	L1



b) Explain vector interrupt and simultaneous interrupt requests

• A device requesting an interrupt identifies itself by sending a special-code to processor over bus. • Then, the processor starts executing the ISR.

• The special-code indicates starting-address of ISR.

• The special-code length ranges from 4 to 8 bits.

• The location pointed to by the interrupting-device is used to store the staring address to ISR.

• The staring address to ISR is called the interrupt vector.

• Processor → loads interrupt-vector into PC & → executes appropriate ISR.

• When processor is ready to receive interrupt-vector code, it activates INTA line.

• Then, I/O-device responds by sending its interrupt-vector code & turning off the INTR signal.

• The interrupt vector also includes a new value for the Processor Status Register

INTERRUPT NESTING • A multiple-priority scheme is implemented by using separate INTR & INTA lines for each device

• Each INTR line is assigned a different priority-level as shown in Figure. Device

• Each device has a separate interrupt-request and interrupt-acknowledge line.

• Each interrupt-request line is assigned a different priority level.

• Interrupt requests received over these lines are sent to a priority arbitration circuit in the processor.

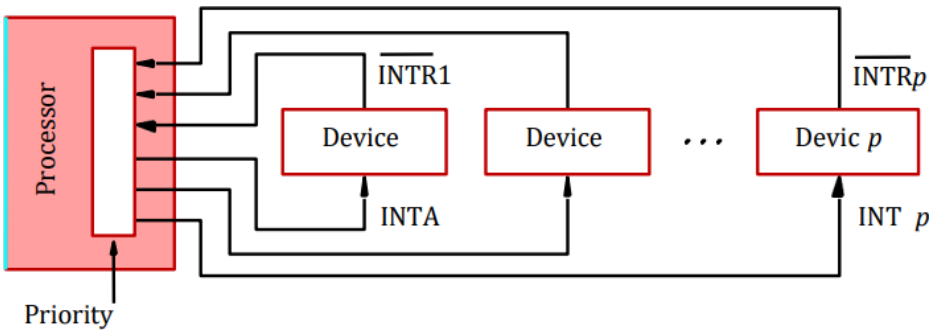
• If the interrupt request has a higher priority level than the priority of the processor, then the request is accepted.

• Priority-level of processor is the priority of program that is currently being executed.

• Processor accepts interrupts only from devices that have higher-priority than its own.

• At the time of execution of ISR for some device, priority of processor is raised to that of the device.

• Thus, interrupts from devices at the same level of priority or lower are disabled.


Processor
INTR1
INTRp
Device
Device
Devic p
INTA
INT p
Priority

CI CCI HoD