CMR INSTITUTE OF TECHNOLOGY

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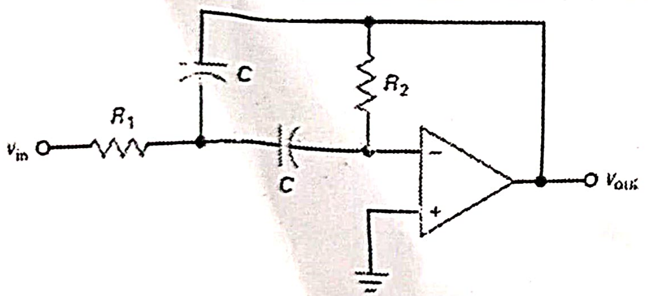
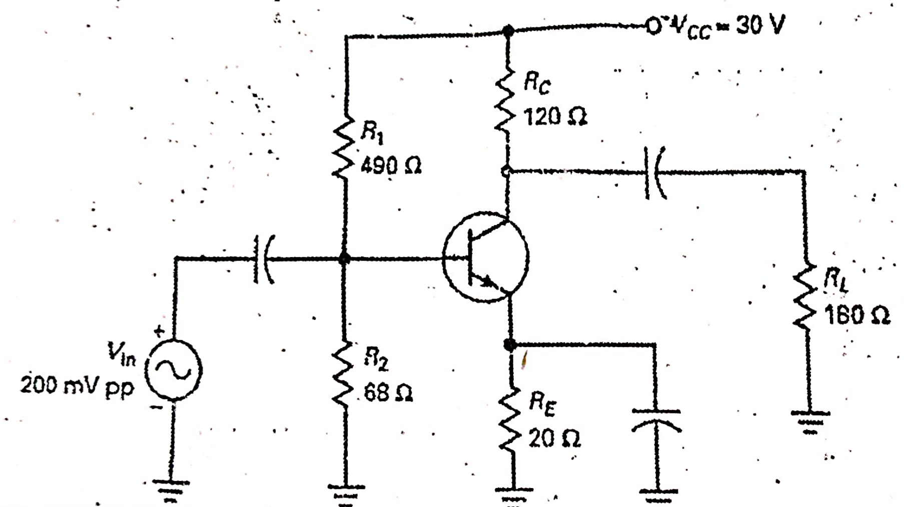
Internal Assesment Test - I

Sub:	Electronic Principles and Circuits						Code:	BEC303
Date:	07/01/2026	Duration:	90 mins	Max Marks:	50	Sem: 3rd	Branch:	ECE

Answer Any FIVE FULL Questions

		Marks	OBE CO	OBE RBT
1.	(a) Explain the working of Astable multivibrator using 555 timer with internal diagram. (b) Develop an expression for transconductance in terms of drain current and overdrive voltage.	[7+3]	CO3	L1
2.	 Explain wideband and narrowband filters. In Fig., R1 =2 kΩ, R2 =56 kΩ, and C =270 pF. determine the voltage gain, Q, and center frequency?	[10]	CO4	L2
3.	Differentiate class A, class B, and class C power amplifier.	[10]	CO5	L1
4.	Draw T-equivalent model of (i) CS Amplifier (ii) CD MOSFET Amplifier	[5+5]	CO3	L3

P.T.O

5.	Explain the different configurations of negative feedback circuits with necessary diagrams and equations.	[10]	CO4	L2
6.	For a peak-to-peak output voltage of 18 V, and input impedance of the base is 100 ohm, find the power gain, power dissipation, and power efficiency. 	[10]	CO5	L3
7.	(a) Draw two-transistor model of SCR. Explain SCR phase control with necessary waveforms. (b) Explain the design of IGBT.	[7+3]	CO5	L1

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1.	(a) Explain the working of Astable multivibrator using 555 timer with internal diagram.	[7+3]	CO3	L1

Astable Operation of the 555 timer

* Generating time delays from microseconds to h... is useful in many applications.
The 555 timer can also be used as an astabl... (or) free-running multivibrator.
* In this mode, it requires two external resi... and one capacitor to set the frequency oscillations.
* The trip points are same as for monostable operation.

$\boxed{UTP = \frac{2V_{CC}}{3}}$ $\boxed{LTP = \frac{V_{CC}}{3}}$

* When Q is low, the transistor is cut off and the capacitor is charging through a total resistance of:

$\boxed{R = R_1 + R_2}$.

* The charging time constant is $(R_1+R_2)C$. As the capacitor charges, the threshold voltage (pin 6) increases.
* When the threshold voltage exceeds $+\frac{2V_{CC}}{3}$. then, the upper comparator sets the flip-flop.

* With Q high, the transistor saturates and grounds pin 7. The capacitor now discharges through R_2. Therefore, the discharging time constant is R_2C.
* When the capacitor voltage drops to slightly less than $\frac{V_{cc}}{3}$, the lower comparator resets the flip flop.

flip-flop.

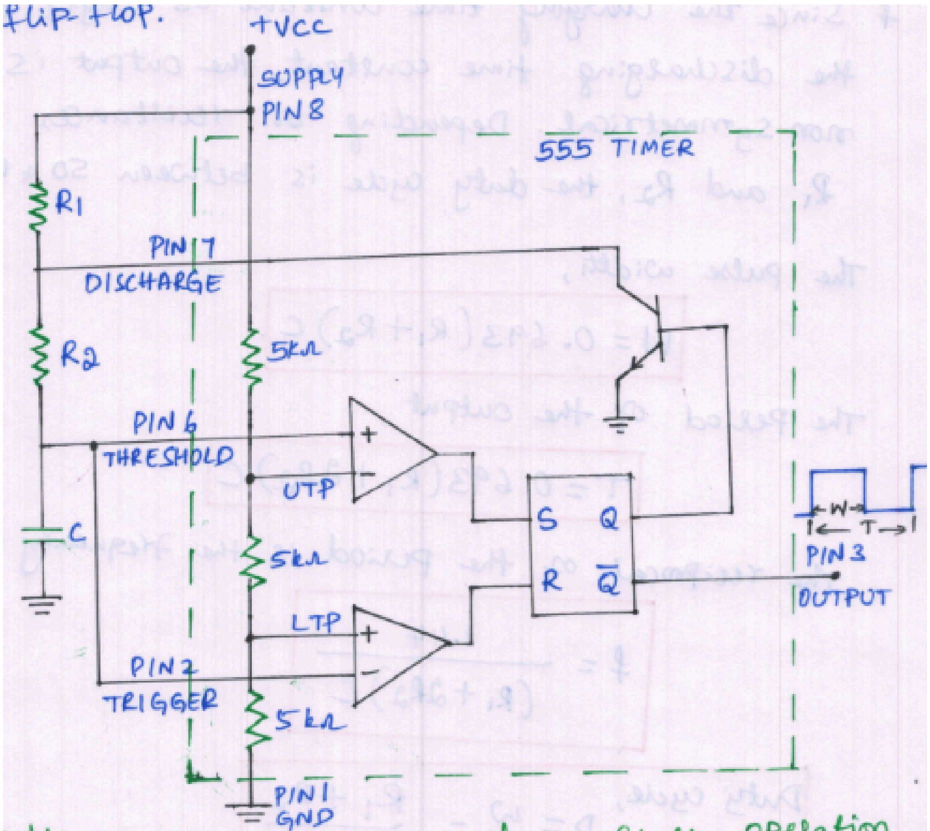


Fig 1:- 555 timer connected for astable operation

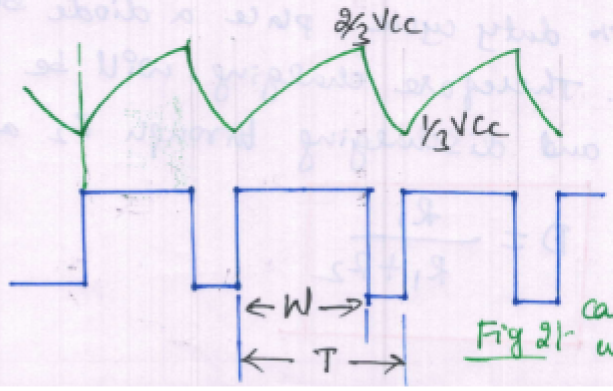


Fig 2:- capacitor & output waveforms

* Fig 2 Shows the waveforms. The timing Capacitor has exponentially rising and falling Voltages between UTP and LTP. The output is a rectangular wave that Swings between 0 and Vcc.

* Since the charging time constant is longer than the discharging time constant, the output is non symmetrical. Depending on resistances R_1 and R_2, the duty cycle is between 50 & 100%.

The pulse width,

$$\boxed{W = 0.693(R_1 + R_2)C}$$

The Period of the output,

$$\boxed{T = 0.693(R_1 + 2R_2)C}$$

The reciprocal of the period is the frequency:

$$\boxed{f = \frac{1.44}{(R_1 + 2R_2)C}}$$

$$\boxed{\text{Duty cycle, } D = \frac{W}{T} = \frac{R_1 + R_2}{R_1 + 2R_2}}$$

* To get 50% duty cycle, place a diode between pins 7 & 6. Therefore charging will be through R_1 alone and discharging through R_2 alone.

$$\boxed{D = \frac{R_1}{R_1 + R_2}}$$

(b) Develop an expression for transconductance in terms of drain current and overdrive voltage.

Define Transconductance:-

From (3).

$$i_d = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_t)\,v_{gs} \longrightarrow (4).$$

This equation relates i_d (output ac) and v_{gs} (input ac).

From (4).

$$\boxed{g_m = \frac{i_d}{v_{gs}} = \mu_n C_{ox}\left(\frac{W}{L}\right)(\underbrace{V_{GS}-V_t}_{DC}).} \longrightarrow (5)$$

Typically, $g_m = 1\ mA/V$.

$$g_m = \frac{i_d \xrightarrow{} \text{ac output}}{v_{gs} \xrightarrow{} \text{ac input}} \quad \text{(or)} \quad i_d = g_m \cdot v_{gs}.$$

Alternatively, eqn (5) can be obtained by partially diff. eqn (1) w.r.t. V_{GS}.

i.e.,
$$g_m = \frac{\partial i_D}{\partial V_{GS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_t) \longrightarrow (6).$$

But, w.k.t. $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$.

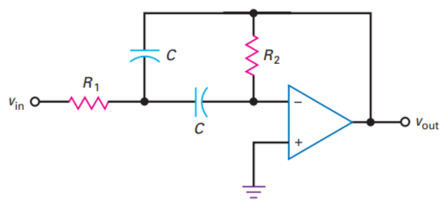
(or)
$$\frac{\sqrt{I_D}}{\sqrt{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)}} = (V_{GS}-V_t) \longrightarrow (7).$$

Substituting (7) in (6).

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)\frac{\sqrt{I_D}}{\sqrt{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)}}.$$

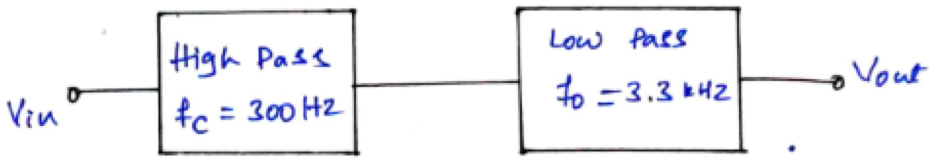
$$= \left(\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)}\right)^{\cancel{2}} \frac{\sqrt{2 I_D}}{\cancel{\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)}}}$$

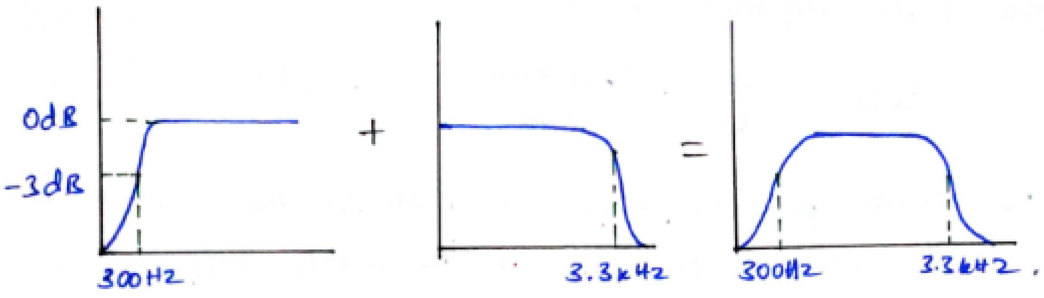
i_D. $\therefore \boxed{g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}} \longrightarrow (8).$

2.		[10]	CO4	L2

Explain wideband and narrowband filters. In Fig., R1 =2 kΩ, R2 =56 kΩ, and C =270 pF. determine the voltage gain, Q, and center frequency?

Wideband filter uses cascade of low-pass and high-pass stages.





→ Above fig shows a wideband filter with $f_1 = 300$ HZ and $f_2 = 3.3$ kHZ.

→ In this case center frequency is.

$$f_0 = \sqrt{f_1 f_2} = \sqrt{(300\,\text{Hz})(3.3\,\text{kHz})} = 995\,\text{HZ}.$$

→ Bandwidth is.

$$BW = f_2 - f_1 = 3.3\,\text{kHZ} - 300\,\text{HZ} = 3\,\text{kHZ}.$$

→ Q is

$$Q = \frac{f_0}{BW} = \frac{995\,Hz}{3kHz} = 0.332$$

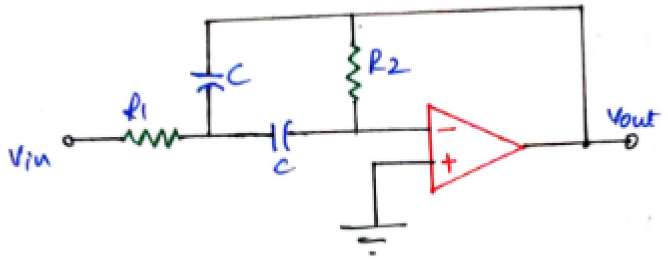
→ Since $Q<1$, low pass and high pass stages can be cascaded.

→ HPF has cutoff frequency = 300Hz and LPF has cutoff frequency = 3.3 kHz.

→ When two responses are added we get a BP response.

Narrow band filters.

* when $Q>1$, we use multiple feedback filter as below.



$$A_V = \frac{-R_2}{2R_1}$$

$$Q = 0.5\sqrt{\frac{R_2}{R_1}}$$

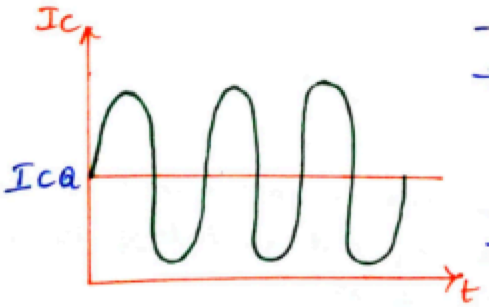
$$f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}}$$

→ Input signal is applied to inverting terminal and circuit has 2 feedback paths, one through a capacitor and another through a resistor.

→ At low frequency, capacitor is open and Vin cannot reach OP-amp and $V_{out} = 0$.

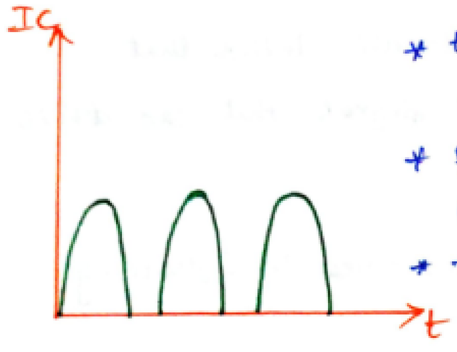
→ At high frequency, capacitor is short. In this case, $A_V = 0$ because $X_C = 0$ and hence $V_{out} = 0$.

→ Between low and high extremes, there is a band of frequencies where circuit acts like an inverting amplifier.

	→ The voltage gain at fc is $\boxed{A_V = \frac{-R_2}{2R_1}}$ → Quality factor is $\boxed{Q = 0.5\sqrt{\frac{R_2}{R_1}}}$ which is equivalent to: $\boxed{Q = 0.707\sqrt{-A_V}}$ → center frequency is given by, $\boxed{f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}}$ Since $C_1 = C_2$ . . $\boxed{f_0 = \frac{1}{2\pi C\sqrt{R_1 R_2}}}$			
3.	Differentiate class A, class B, and class C power amplifier. 1. Classes of operation. 1) class A operation :- Here transistor operates in the active region at all times. i.e., Collector current (I_C) flows for 360° of the ac cycle as shown below.  → ICQ → DC component of IC. → In class 'A' operation, the Q-point is usually at the middle of the load line. → Thus, the signal swing over the maximum possible range without saturating or cutting of the transistors which would distorted the signal.	[10]	CO5	L1

2) class B operation :-

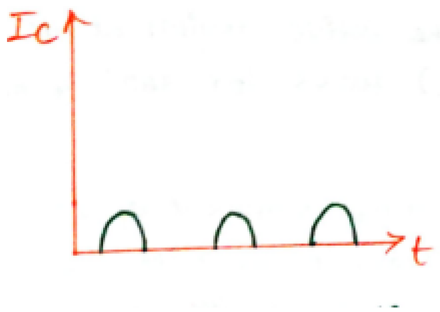
Here Collector current (I_c) flows only half the cycle (180°), as shown below.



* Here Q-point is located at cutoff.
* Positive half a ac base voltage can produce collector current (I_c).
* This reduces the wasted heat in power transistors.

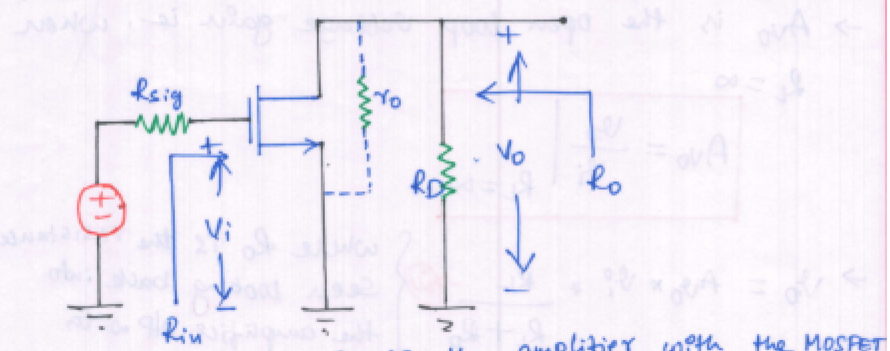
3) Class C operation :-

* Here the collector current flows less than 180° of the ac cycle.
* only part of the positive half cycle of AC base voltage produces collector current.

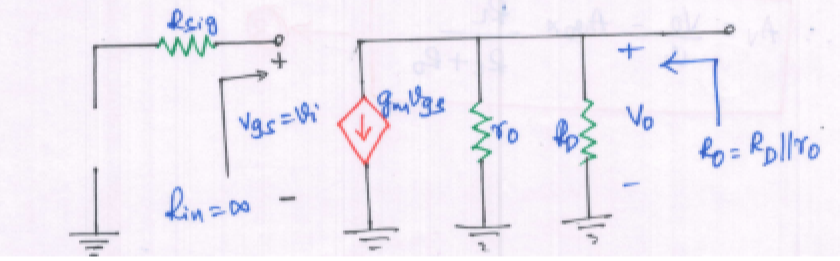


4.	Draw T-equivalent model of (i) CS Amplifier (ii) CD MOSFET Amplifier	[5+5]	CO3	L3

The Common Source (CS) Amplifier without Source Resistance



The below circuit shows the amplifier with the MOSFET replaced with its hybrid-π model.



→ Let us now, find the characteristic parameters of the amplifier.

1) R_{in},

$$\boxed{R_{in} = \infty}$$

2) A_{vo} from the circuit,

$$v_o = -(g_m v_{gs})(R_D || r_o)$$

Since $v_{gs} = v_i$, $A_{vo} = \frac{v_o}{v_i} = -(g_m \times (R_D || r_o))$

$$\boxed{A_{vo} \cong -g_m R_D} \Big|_{\text{for } r_o \gg R_D}.$$

3) R_o :

$$R_o = R_D || r_o$$

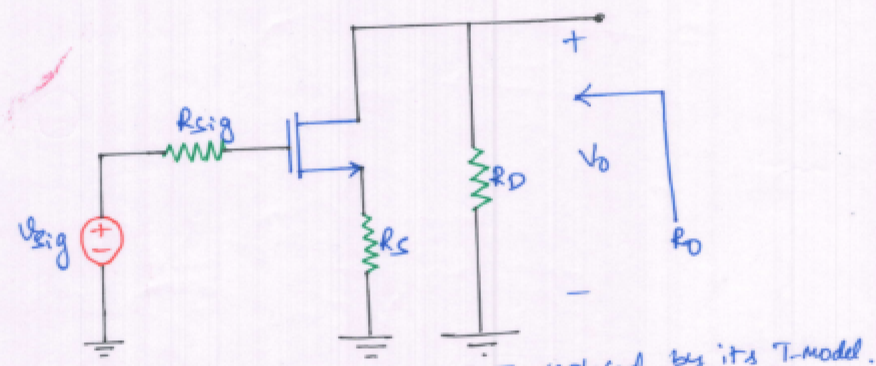
for $r_o \gg R_D$ $\boxed{R_o \cong R_D}$

Overall vg gain G_v : To determine the overall voltage gain G_v, by considering R_L.

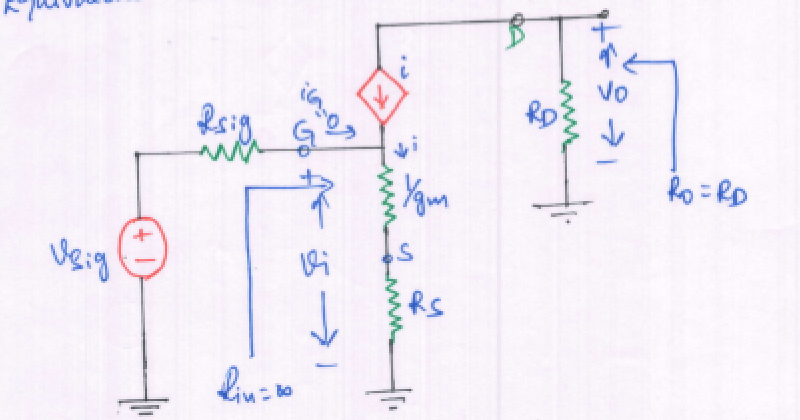
Then, $\boxed{G_v = -g_m (R_D || R_L || r_o)}$

Common Source Amplifier with a Source Resistance.

[Note: whenever a resistance is connected in the Source lead, the T model is preferred.
r_o is not included in the analysis. As its value is very high which has least effect in amplifier parameter But addition of r_o would unnecessarily complicate the analysis].



Equivalent circuit with MOSFET replaced by its T-model.



From the circuit,

$$v_{gs} = v_i \times \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_s} = \frac{v_i}{1 + g_m R_s}.$$

$$v_o = -i R_D.$$

where, $$i = \frac{v_i}{\frac{1}{g_m} + R_s} = \left(\frac{g_m}{1 + g_m R_s}\right) v_i$$

$$\therefore v_o = -\frac{g_m}{(1 + g_m R_s)} \times v_i \times R_D.$$

$$\boxed{A_{vo} = \frac{v_o}{v_i} = \frac{-g_m}{1 + g_m R_s} \times R_D}$$

The equation of A_{vo} indicates that including R_S reduces the voltage gain by the factor $(1 + g_m R_s)$.

Common Drain Amplifier

(or)

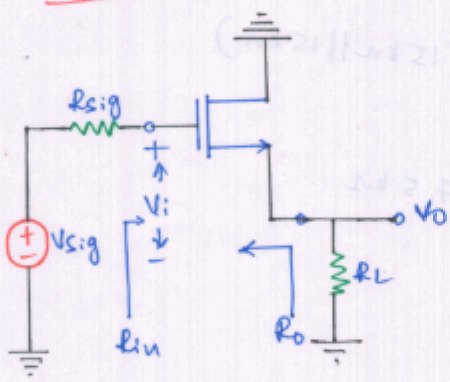
Source Follower.

→ In this configuration, Drain is grounded.

→ The Voltage at the O/P terminal (source) will follow that at the i/P. Hence, the name Source follower.

→ It is used as a buffer.

Circuit :-



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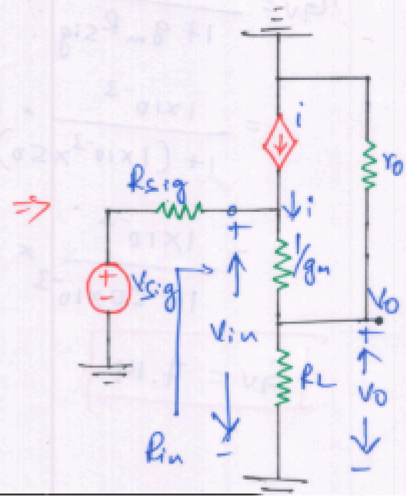

Characteristics parameters

Rin :

$$\boxed{R_{in} = \infty} \rightarrow (1)$$

Av : from the circuit,

$$v_o = v_i \times \frac{R_L}{R_L + 1/g_m}$$

$$\therefore \boxed{A_V = \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m}} \rightarrow (2)$$

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A_{vo} : (Setting $R_L = \infty$)
from (2)
$\boxed{A_{vo} = 1}$ $\Rightarrow$ ∴ $V_o = V_i$, Hence the name Voltage follower.

R_o :
The o/p resistance R_o is found by Setting $V_i = 0$
Now looking back into the o/p terminal, excluding R_L, R_o we see as $\frac{1}{g_m}$.
∴ $\boxed{R_o = \frac{1}{g_m}}$

$G_V = \frac{R_{in}}{R_{in} + R_{sig}} \times A_{vo} \times \frac{R_L}{R_L + R_o}$.
$= \underbrace{1}_{(R_{in}=\infty)} \times 1 \times \frac{R_L}{R_L + R_o}$. {since $A_{vo} = 1$ & $R_{in} = \infty$}

$\boxed{G_V = \frac{R_L}{R_L + \frac{1}{g_m}}}$ ∴ G_V will be lower than unity
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Explain the different configurations of negative feedback circuits with necessary diagrams and equations.

Four Types of Negative Feedback:-

The negative feedback amplifier is an electronic amplifier in which the feedback energy (Voltage (or) Current) is out of phase with input signal and thus opposes it. Negative feedback reduces gain. It also reduces distortion, noise and instability. This feedback increases bandwidth and improves input and output impedance.

The input to a negative feedback amplifier can be either a voltage (or) current, also, the output signal can be either a voltage (or) a current, this implies that four types of negative feedback exists.
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<td>[10]</td>
<td>CO4</td>
<td>L1</td>
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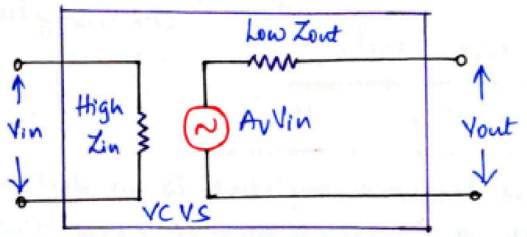
Ideal Negative Feedback.

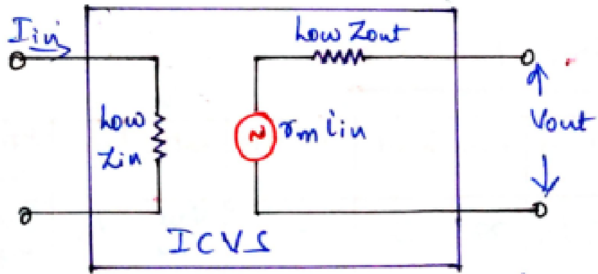
Input	Output	Circuit	Zin	Zout	Converts	Ratio	Symbol	Type of Amplifier
V	V	VCVS	∞	0	—	$\frac{V_{out}}{V_{in}}$	A_V	Voltage amplifier.
I	V	ICVS	0	0	i to V	$\frac{V_{out}}{i_{in}}$	r_m	Transresistance Ampr.
V	I	VCIS	∞	∞	V to i	$\frac{i_{out}}{V_{in}}$	g_m	Transconductance ampr.
I	I	ICIS	0	∞	—	$\frac{i_{out}}{i_{in}}$	A_i	Current Amplifier

1. Voltage Controlled Voltage Source (VCVS).



* It is ideal voltage amplifier because it has a stabilized voltage gain, infinite input impedance and zero output impedance.
* Voltage gain is symbolized as 'Av'.
* Input impedance is '∞'.
* output impedance is '0'.
* also known as 'voltage amplifier'.

2. Current Controlled Voltage Source (ICVS).



* An input current controls an output voltage, an ICVS is something called a transresistance amplifier.
* Transresistance amplifier (Current to Voltage converter)
* Input impedance is low.
* output impedance is also low.
* Symbolized as 'rm' and expressed in ohms.

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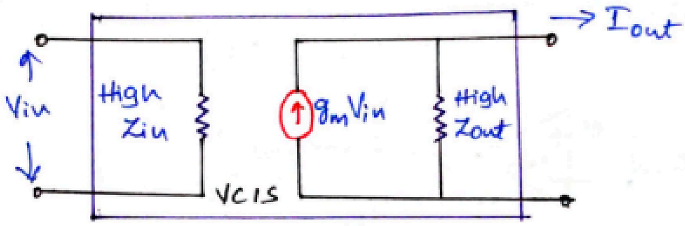
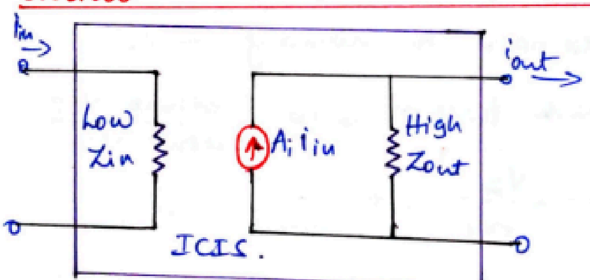
3. Voltage Controlled Current Source (VCIS).



* Input voltage controls an output current.
* Also known as 'transconductance amplifier'.
* High input impedance.
* High output impedance.
* Conversion factor of VCIS is called transconductance and symbolized 'g_m' and expressed in 'Siemens' (mho).

4. Current Controlled Current Source (ICIS).



* An input current is amplified to get a larger output current.
* It is ideal current amplifier because it has a stabilized current gain, zero input impedance, and infinite output impedance.
* Low input impedance.
* High output impedance.
* also known as 'current amplifier'.
* Current gain is symbolized as 'A_i'.

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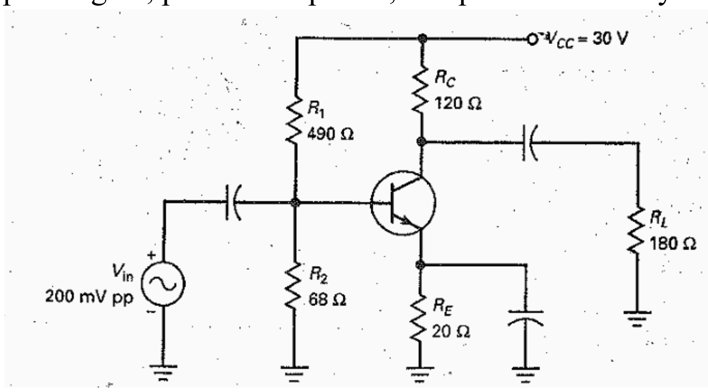
For a peak-to-peak output voltage of 18 V, and input impedance of the base is 100 ohm, find the power gain, power dissipation, and power efficiency.



</td>
<td>[10]</td>
<td>CO5</td>
<td>L3</td>
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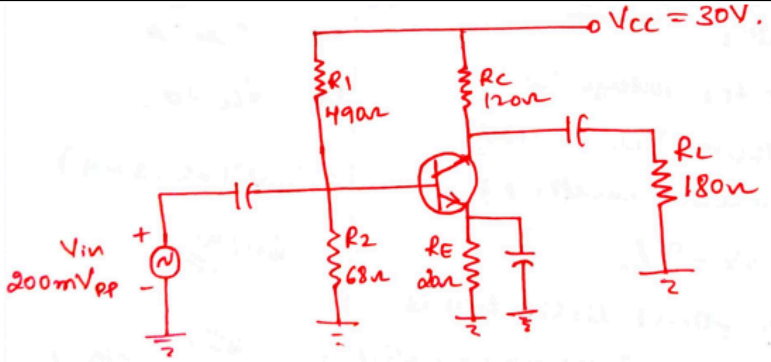
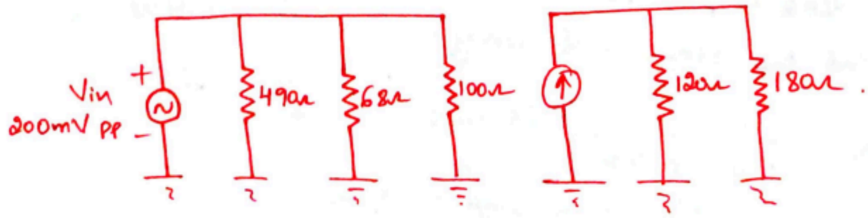




Sol^n: As shown in fig (b).

$$Z_{in(stage)} = 490\Omega \,||\, 68\Omega \,||\, 100\Omega = 37.4\Omega.$$

The ac input power is:

$$P_{in} = \frac{(200mV)^2}{8(37.4)} = 133.7\,\mu W.$$

The ac output power is:

$$P_{out} = \frac{(18V)^2}{8(180\Omega)} = 225mW.$$

The power gain is:

$$A_p = \frac{225mW}{133.7\,\mu W} = 1683.$$

Sol^n

The dc emitter current is:

$$I_E = \frac{V_E}{R_E} = \frac{3V}{20\Omega} = 150mA.$$

The dc collector voltage is:

$$V_C = 30V - (150mA)(120\Omega) = 12V.$$

and the dc collector-emitter v/g is

$$V_{CEQ} = 12V - 3V = 9V.$$

The transistor power dissipation is:

$$P_{DQ} = V_{CEQ} I_{CQ} = (9V)(150mA) = 1.35W.$$

To find the stage efficiency:

$$I_{bias} = \frac{30V}{490\Omega + 68\Omega} = 53.8mA.$$

$$I_{dc} = I_{bias} + I_{CQ} = 53.8mA + 150mA = 203.8mA.$$

The dc input power to the stage is

$$P_{dc} = V_{CC} I_{dc} = (30V)(203.8mA) = 6.11W.$$

$$\eta = \frac{225mW}{6.11W} \times 100\%.$$

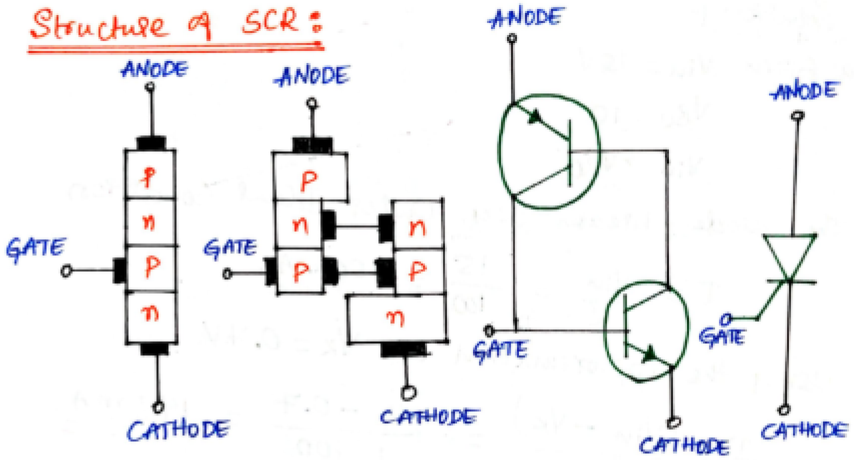
$$\boxed{\eta = 3.68\%}$$

7.	(a) Draw two-transistor model of SCR. Explain SCR phase control with necessary waveforms.	[7+3]	CO5	L1

Silicon Controlled Rectifier (SCR).

The SCR is the most widely used Thyristor. It can switch very large currents ON and OFF.
Because of this, it is used to control motors, ovens, air conditioners, and induction heaters.

Structure of SCR:



Silicon Controlled Rectifier.

Figure above shows the structure of the SCR. The input is called gate, the top is anode, the bottom is cathode. The SCR is more useful than four layer diode because gate triggering is easier than breakover triggering.

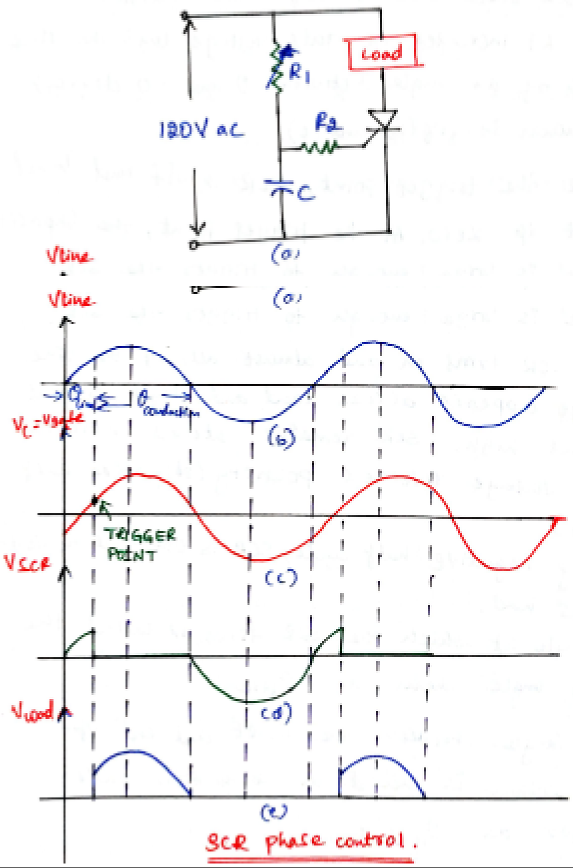
Triggering the SCR (turning ON)

By adding an input terminal to the base of Q2 and by applying a trigger (sharp pulse) to the base of Q2, the SCR can be turned ON. Therefore, the SCR is equivalent to a latch with a trigger input. Since the gate of an SCR is connected to the base of an internal transistor, it takes at least 0.7V to trigger an SCR.

The trigger momentarily increases the base current of Q2. This starts the positive feedback, which drives both transistors into saturation and voltage across the device is ideally zero.

SCR Phase Control.

Phase control of SCR means having control on the phase relationship between the start of current through the SCR and source voltage. These are used as rectifiers to generate controlled DC voltage from the ac input.



SCR phase control.

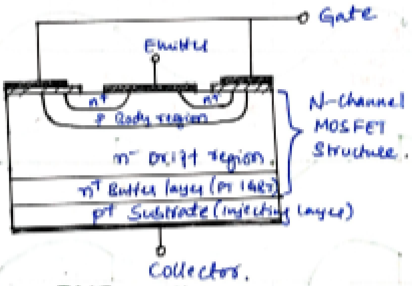
Operation:-

* Fig(a) shows ac line voltage being applied to an SCR circuit that controls the current through a heavy load. In this circuit, variable resistor R1 and capacitor shift the phase angle of the gate signal. When R1 is 0, the gate voltage is in phase with the line voltage and SCR acts like a half wave rectifier.
  When R1 increases, ac gate voltage lags the line voltage by an angle between 0 and 90 degrees as shown in fig(b) and (c).
* Before the trigger point, SCR is off and load current is zero. At the trigger point, the capacitor voltage is large enough to trigger the SCR.
* The SCR turns on and almost all of the line voltage appears across load and load current becomes high. SCR remains latched until the line voltage reverses polarity (Negative half cycle).
* During negative half cycle, SCR is off and no voltage across load.
* The angle at which the SCR fires is called the firing angle shown as θ_{fire}.
* The angle between the start and end of conduction is called as conduction angle shown as $\theta_{conduction}$.

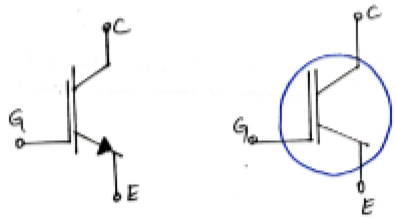
(b) Explain the design of IGBT.

The IGBT is the combination of BJT and MOSFET. It is a four-layer PNPN voltage controlled high speed switching device capable of handling large currents. It has three PN junctions and three terminals Gate (G), Collector (C) and Emitter (E). Gate terminal as it is the input part, taken from MOSFET while the collector and emitter as they are the output, taken from the BJT.

Basic construction



Basic IGBT structure.



	IGBT is made of four layers of semiconductor to form a PNPN structure. The collector (C) electrode is attached to P layer while the Emitter (E) is attached between the P and N layers. A P+ substrate is used for the construction of IGBT. * AN N-layer is placed on top of it to form PN junction J1. Two P regions are fabricated on top of N-layer to form PN junction J2. The P region is designed in such a way to leave a path in the middle for the gate (G) electrode. N+ regions are diffused over the P region as shown in the figure. * The emitter and gate are metal electrodes. The emitter is directly attached to the N+ region while the gate is insulated using a silicon dioxide layer. The base P+ layer inject holes into N-layer that is why it is called injector layer. while the N-layer is called the drift region. * The N-layer is designed to have a path for current flow between the emitter and collector through the junction using the channel that is created under the influence of the voltage at the gate electrode.			

CI ***CCI*** ***HOD***