Modified

CBCS SCHEME

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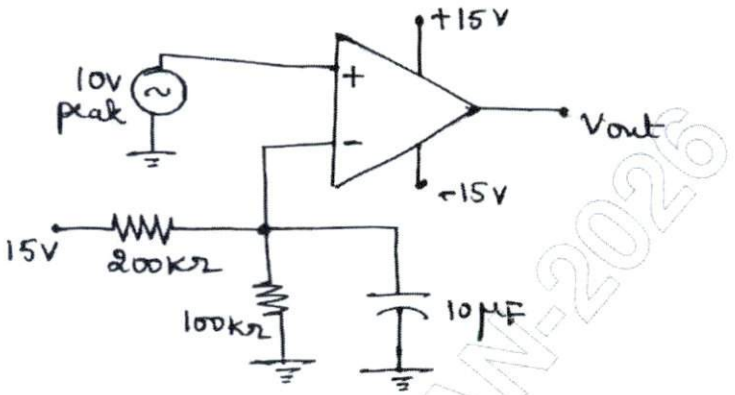
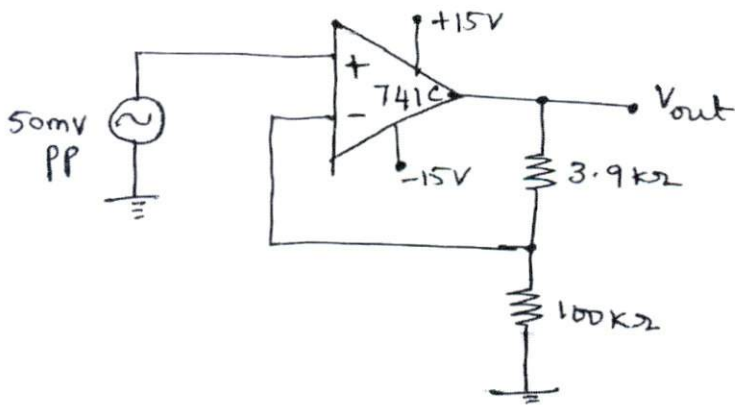
BEC303

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Electronic Principles and Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Develop an expression for the operating point I_C and V_{CE} for the voltage divider bias circuit using approximate analysis. Hence calculate the operating point for the VDB circuit given : $V_{CC} = 10V$, $R1 = 10K\Omega$, $R2 = 2.2\ K\Omega$, $R_C = 3.6K\Omega$, $R_E = 1\ K\Omega$.	10	L3	CO1
	b.	For the voltage divider biased amplifier, derive the expression for the voltage gain from i) π –Model ii) T –Model.	10	L2	CO1
		OR			
Q.2	a.	Develop an expression for voltage gain and input impedance for an emitter follower with neat circuit diagram.	10	L2	CO1
	b.	Determine the operating point for two supply emitter bias circuit given : $V_{CC} = 10V$, $R_C = 3.6\ K\Omega$, $R_B = 2.1\ K\Omega$, $R_E = 1\ K\Omega$ and $-V_{EE} = -2V$.	5	L2	CO1
	c.	Develop an expression for the operating point I_C and V_{CE} for collector feedback bias circuit.	5	L2	CO1
		Module – 2			
Q.3	a.	With neat circuit diagrams, explain biasing of MOSFET by fixing the gate voltage.	10	L2	CO2
	b.	With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common source amplifier with source resistance.	10	L2	CO2
		OR			
Q.4	a.	With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common gate amplifier.	10	L2	CO2
	b.	Define transconductance and hence develop any three expressions for transconductance.	10	L2	CO4

		Module – 3			
Q.5	**a.**	With neat circuit diagram, explain the operation of R-2R digital to analog converter.	**6**	**L2**	**CO4**
	b.	For the circuit shown in Fig.Q5(b) the input voltage is a sine wave with peak value of 10V. What is the trip point of the circuit? Determine the cut off frequency of bypass capacitor. Also draw the input output waveform.  Fig.Q5(b)	**6**	**L3**	**CO4**
	c.	Explain the operation of inverting Schmitt-trigger with neat circuit diagram and waveform.	**8**	**L2**	**CO4**
		OR			
Q.6	**a.**	Make use of the concept of lead-lag circuit to explain the operation of Wein bridge oscillator.	**10**	**L2**	**CO4**
	b.	Explain the operation of Astable Multi-Vibrator using 555 timer with internal block diagram and waveforms.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With neat block diagram, explain four types of negative feedback circuit.	**8**	**L2**	**CO3**
	b.	For the circuit shown in Fig.Q7(b), calculate the feedback fraction, the ideal closed loop voltage gain, the percent error and the exact closed loop voltage gain, use the open loop gain of 741C as 100,000.  Fig.Q7(b)	**6**	**L2**	**CO3**
	c.	With neat circuit diagram and equations, explain the operation of a current amplifier.	**6**	**L2**	**CO3**

		OR			
Q.8	**a.**	Classify filters and explain each filter with its ideal frequency response.	**10**	**L2**	**CO3**
	b.	What is First Order Filters? Explain the various implementation of first order low pass and high pass active filters with expressions.	**10**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Explain the operation of class–B push pull emitter follower amplifier with its advantages and disadvantages.	**10**	**L2**	**CO5**
	b.	Discuss the concepts of DC and AC load line taking voltage divider bias amplifier as an example.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain the working of SCR phase control with the help of circuit and waveform.	**10**	**L2**	**CO5**
	b.	Explain the construction, control and advantages of Insulated-Gate Bipolar Transistor (IGBT).	**10**	**L2**	**CO5**

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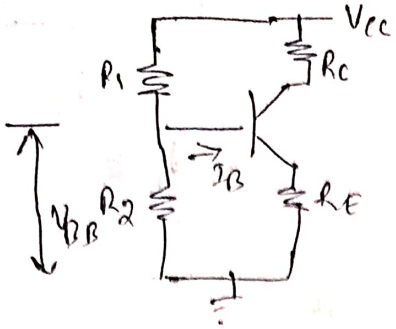
VTU EPC Solutions 2026 (BEC303)

1. (a)



we have $V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}$

Applying KVL at the o/p mode,

$V_{cc} - I_c R_c - V_c = 0$

where, $V_c = V_{cc} - I_c R_c$

$\therefore V_{CE} = V_c - V_E = V_{cc} - I_c R_c - I_c R_E = V_{cc} - I_c (R_c + R_E)$

$\Rightarrow \boxed{V_{CE} = V_{cc} - I_c (R_c + R_E)}$

Applying KVL at the i/p mode,

$V_{BB} - V_{BE} - V_E = 0$, $I_E = I_c = \frac{V_E}{R_E}$

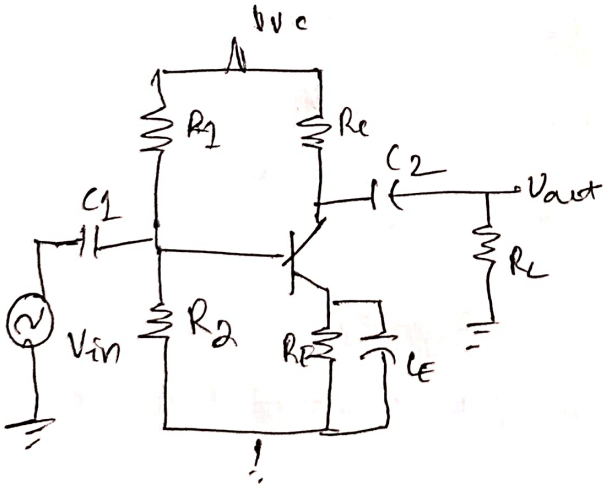
To find the operating point,

1. $V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2} = 1.8\,V$. 2. $V_E = V_{BB} - V_{BE} = 1.1\,V$.

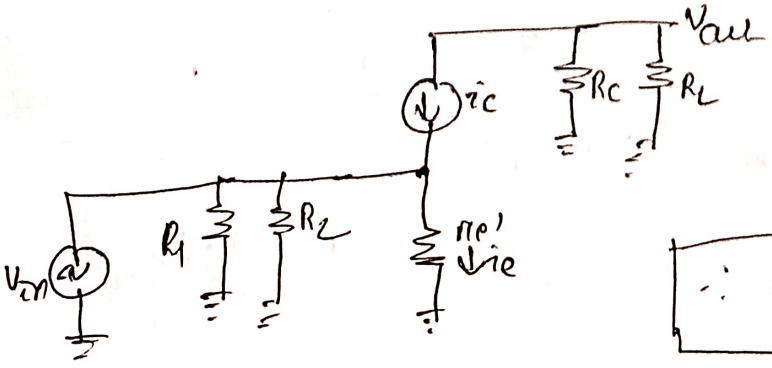
3. $I_E = \frac{V_E}{R_E} = 1.1\,mA$ (4) $V_{CB} = V_{CC} - I_C R_C = 6.04\,V$

(5) $V_{CE} = V_C - V_E = 4.94\,V$.

(b) voltage divider ckt :-



T- model



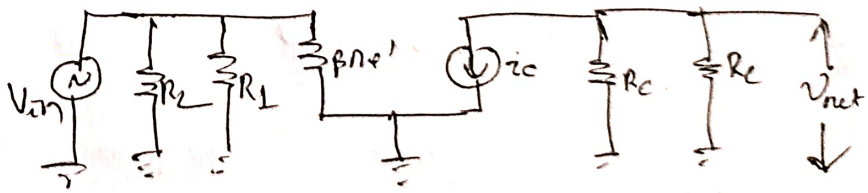
$V_{in} = i_e r_e'$

$V_{out} = i_c (R_c \| R_L)$

$\therefore A_V = \frac{V_{out}}{V_{in}} = \frac{i_c (R_c \| R_L)}{i_e r_e'} = \frac{R_c \| R_L}{r_e'} = \frac{r_e}{r_e'}$

where $r_e = R_c \| R_L$

π- model

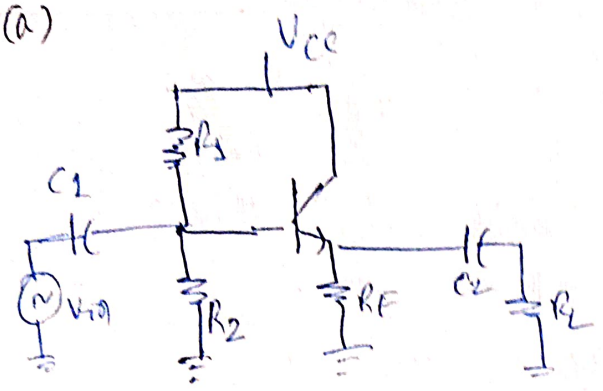


$V_{in} = i_B \beta r_e'$

$V_{out} = i_c (R_c \| R_L)$

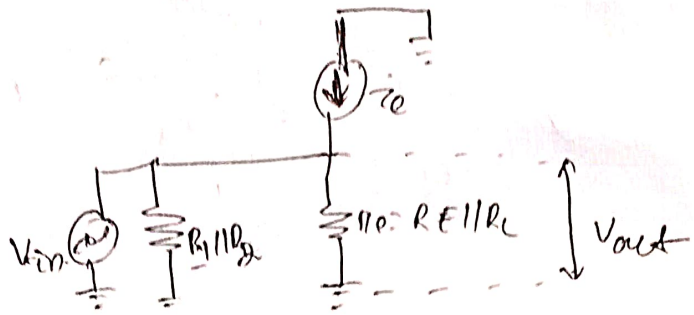
$\therefore A_V = \frac{V_{out}}{V_{in}} = \frac{\beta i_b (R_c \| R_L)}{i_b \beta r_e'} = \frac{R_c \| R_L}{r_e'}$

(2) (a) Ckt. of Emitter Follower :-



$\Rightarrow$

T-model :



Expressions for the voltage gain :-

$V_{out} = i_e (r_e \| r_e')$

$V_{in} = i_e (r_e + r_e')$

$\therefore \frac{V_{out}}{V_{in}} = A_v = \frac{r_e \| r_e'}{i_e (r_e + r_e')} = \frac{r_e}{r_e + r_e'}$

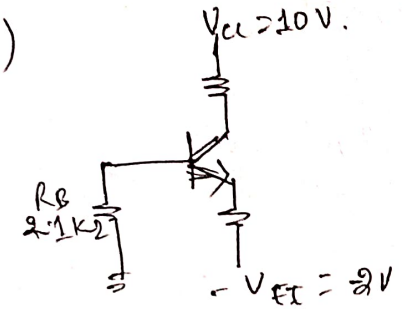
As $r_e \gg r_e' \Rightarrow$ $\boxed{A_v = \frac{r_e}{r_e} \simeq 1}$

i/p impedance :-

$Z_{in} = \frac{V_{in}}{i_b} = \frac{\beta i_b (r_e + r_e')}{i_b} = \beta (r_e + r_e') = Z_{in(base)}$

$\boxed{Z_{in(stage)} = R_1 \| R_2 \| \beta (r_e + r_e')}$

(b)

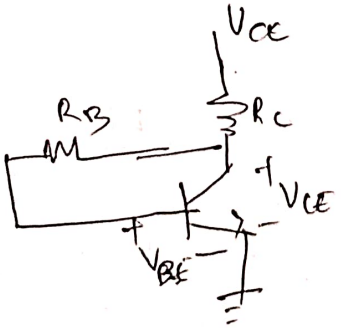


$I_E = \frac{V_{EE} - V_{BE}}{R_E} = 1.3$ mA

$V_C = V_{CC} - I_C R_C = 5.32$ V.

$V_{CE} = V_C + V_{BE} = 6.02$ V.

(c)



$\therefore$ Applying KVL to the base,

$V_{cc} - (I_c + I_B) R_c - I_B R_B - V_{BE} = 0$

$\because I_c + I_B \simeq I_c$

$\Rightarrow V_{cc} - I_c R_c - I_B R_c - V_{BE} = 0$

$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{\beta R_E + R_B}}$

Applying KVL at the o/p,

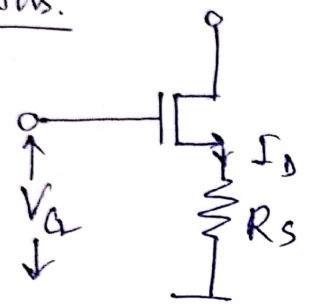
$V_{cc} - (I_c + I_B) R_c - V_{CE} = 0$

$\boxed{V_{CE} = V_{cc} - I_c R_c}$

$\boxed{I_c = \beta I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta}}$

3a.) With neat circuit diagrams, explain biasing of MOSFET by fixing the gate voltage. → 10 M

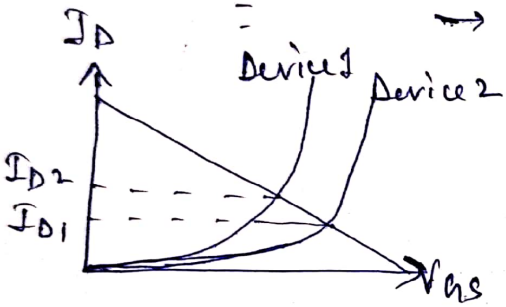
Ans:



$V_G = V_{GS} + I_D R_S$

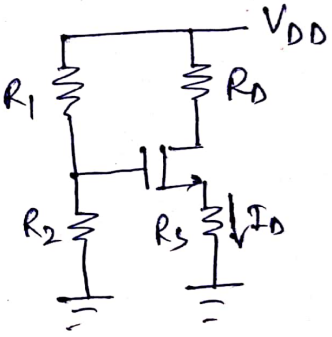
→ If I_D increase, since V_G is constant V_{GS} must decrease which inturn decrease I_D

→ Variation of I_D is small compared to V_{GS}



Implementation 1

Using voltage divider, ~~Implem~~ + explaination

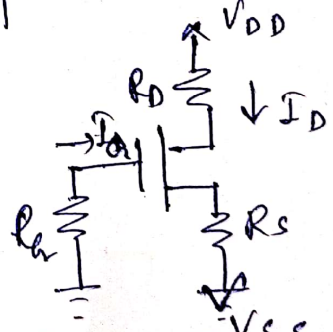


→ R_D is large to obtain high gain and small to allow the desired signal swing.

Implementation 2 with circuit + explaination

$$V_{SS} = V_{GS} + I_D R_S$$

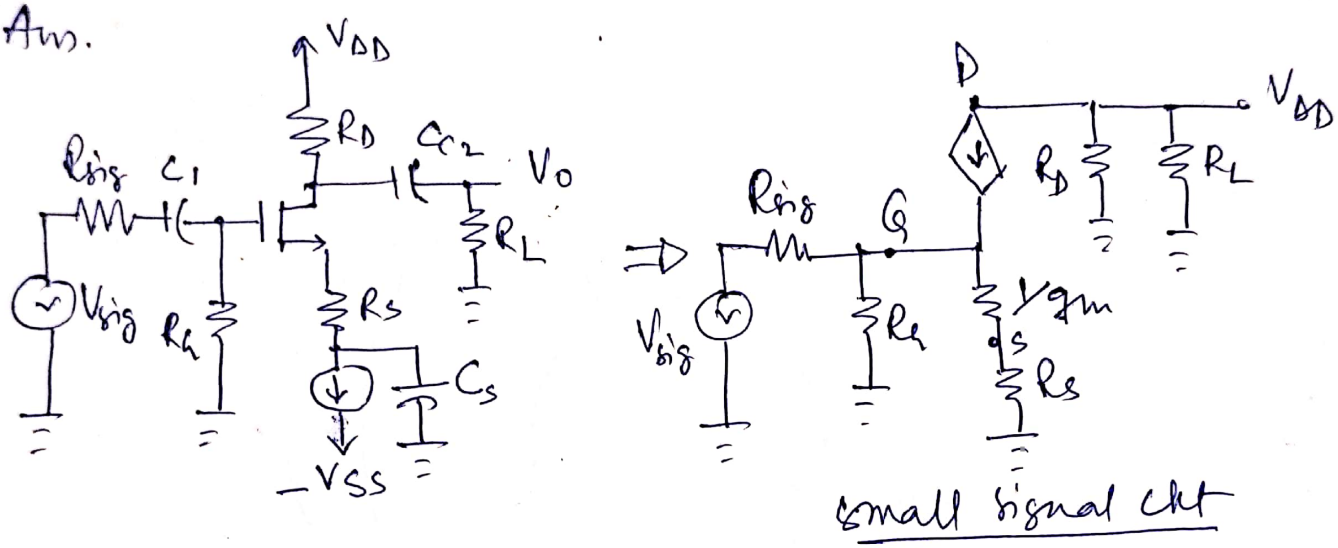
$$I_D = \frac{V_{SS} - V_{GS}}{R_S}$$



If I_D increase, since V_{SS} is const, V_{GS} decrease which decrease I_D

3b) With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common source amplifier with source resistance.

Ans.



Input Impedance: $R_{in} = R_i = R_g$

To find v_i & V_{gs}, $\longrightarrow$

$$v_i = \frac{V_{sig} R_g}{R_g + R_{sig}}, \quad V_{gs} = \frac{v_i \cdot \frac{1}{g_m}}{\frac{1}{g_m} + R_s} = \frac{v_i}{1 + g_m R_s}$$

To find voltage gain and R_o $\longrightarrow$

$$i_d = g_m V_{gs} = \frac{g_m v_i}{1 + g_m R_s}, \quad V_o = -i_d (R_D \| R_L) = \frac{-g_m (R_D \| R_L) v_i}{1 + g_m R_s}$$

$$\therefore \frac{V_o}{v_i} = A_v = \frac{-g_m (R_D \| R_L)}{1 + g_m R_s}$$

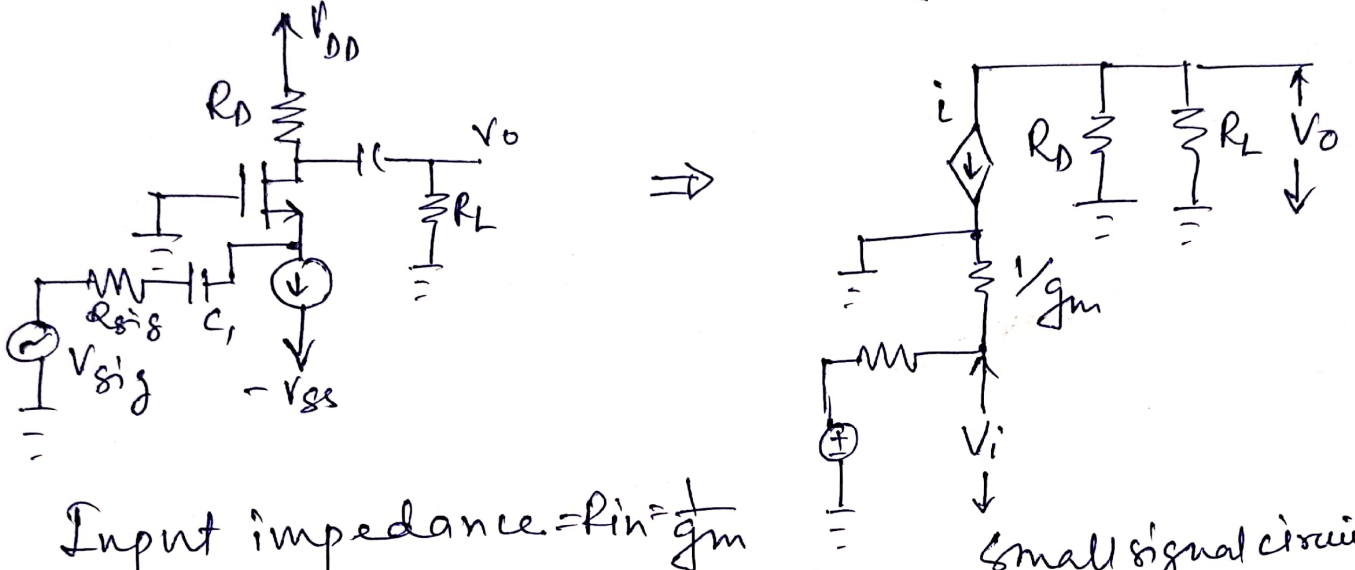
$$\Rightarrow A_{Vo} = -\frac{g_m R_D}{1 + g_m R_s}$$

$$A_v = \frac{V_o}{V_{sig}} = \frac{-g_m (R_D \| R_L)}{1 + g_m R_s} \cdot \frac{R_g}{R_g + R_{sig}}$$

$$R_{out} = R_D$$

4a) With neat circuit diagram, develope an expression for voltage gain, input impedance and output impedance for common gate amplifier.

Ans: Ckt diagram of common gate amplifier →



Small signal circuit

Input impedance $= R_{in} = \frac{1}{g_m}$

To obtain input vtg & drain current,

$$V_i = \frac{V_{sig} \cdot R_{in}}{R_{in} + R_{sig}} \; ; \; R_{in} = \frac{1}{g_m} \Rightarrow V_i = \frac{V_{sig}}{1 + g_m R_{sig}}$$

$$i_i = \frac{V_i}{R_{in}} = g_m V_i \Rightarrow i_d = i = -i_i = -g_m V_i$$

To obtain o/p vtg and gain, & R_o →

$$V_o = -i_d (R_D \| R_L) \Rightarrow \frac{V_o}{V_i} = A_v = g_m (R_D \| R_L)$$

$$A_{vo} = g_m R_D, \quad G_v = \frac{V_o}{V_{sig}} = g_m (R_D \| R_L) \frac{1}{1 + g_m R_{sig}}$$

The o/p Resistance $= Z_o = R_D$.

4b). Define transconductance and hence develop any three expressions for transconductance.

Ans: Definition of $g_m \longrightarrow$

$$g_m = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L} (V_{GS} - V_t)$$

Defⁿ 1: $v_{GS} = V_{GS} + v_{gs}$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

$$= \frac{1}{2} k_n' (W/L) (V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2} k_n' \frac{W}{L} \{ (V_{GS} - V_t)^2 + v_{gs}^2 + 2 (V_{GS} - V_t) \}$$

The signal component is, $i_d = k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t) v_{gs}$

$$\therefore \frac{i_d}{v_{gs}} = g_m = k_n' \left(\frac{W}{L}\right) (V_{GS} - V_T)$$

Defⁿ 2: $g_m = k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)$

But, $I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$

$$\therefore V_{GS} - V_t = \sqrt{\frac{2 I_D}{k_n'}} \cdot \frac{1}{\sqrt{W/L}}$$

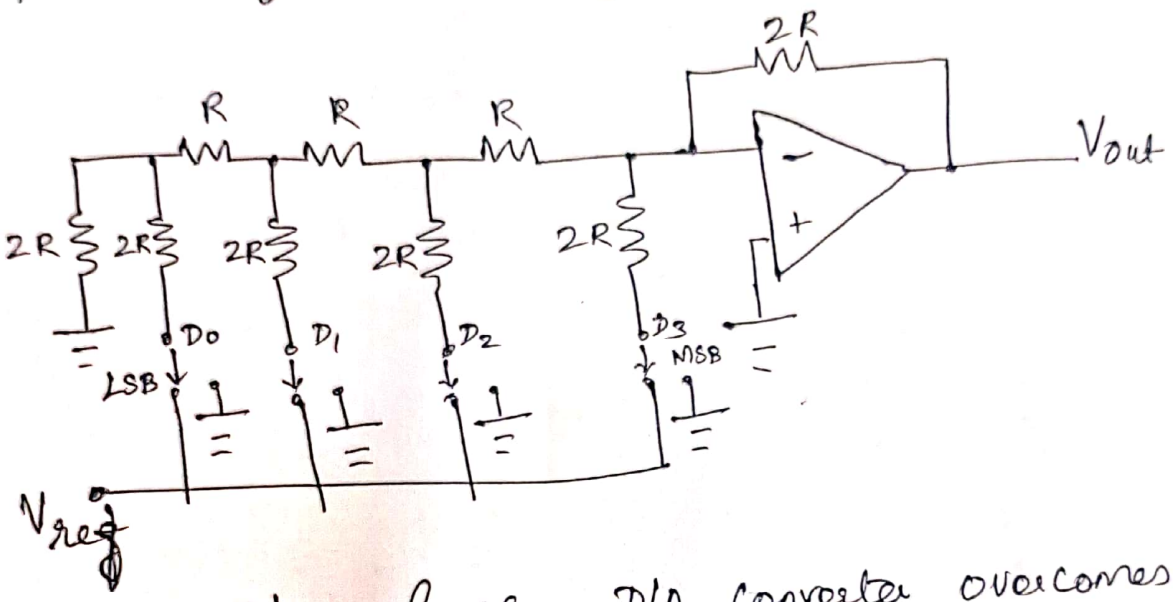
$$\therefore g_m = \sqrt{2 I_D k_n' (W/L)}$$

Defⁿ 3: $g_m = k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)$

But $k_n' \left(\frac{W}{L}\right) = \frac{2 I_D}{(V_{GS} - V_t)^2}$

$$\therefore g_m = \frac{2 I_D}{(V_{GS} - V_t)}$$

Q5 a) With neat circuit diagram, explain the operation of R-2R digital to analog converter.



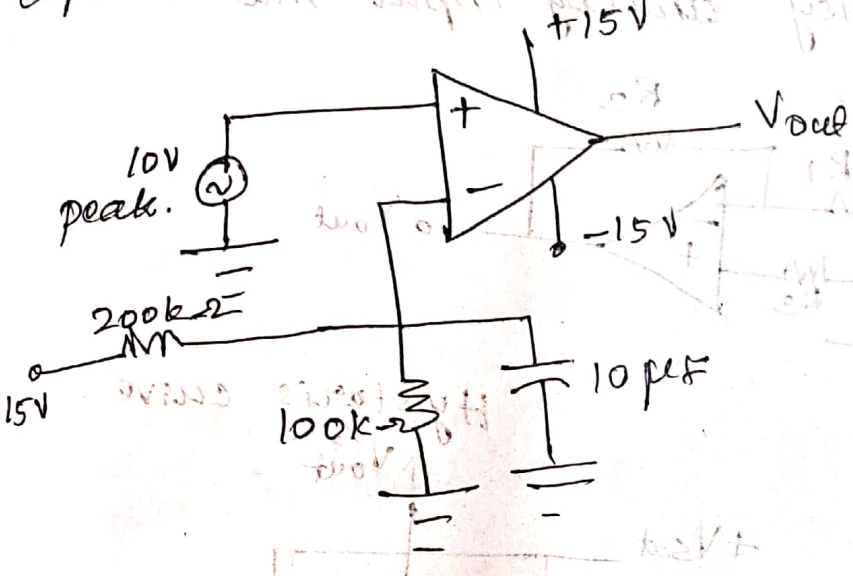
R/2R ladder D/A converter overcomes the limitations of binary weighted D/A converter. and it is widely used in integrated circuit D/A converters.

- only 2 resistors values are required (R, 2R)
- provides higher degree of accuracy.
- D_0 is considered to be the LSB & D_3 is considered to be the MSB.
- To determine the DAC output voltage, the binary input value is charged to its decimal value B_{IN}.

$$B_{IN} = D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + \dots + D_{(N-1)} \times 2^{(N-1)}$$

$$\boxed{V_{out} = -\frac{B_{IN}}{2^N} \times 2 V_{ref}}; \quad N \rightarrow \text{no. of inputs.}$$

Q5.b: For the circuit shown in Fig. Q5.b the Input voltage is a sine wave with peak value of 10V. What is the trip point of the circuit? Determine the cut off frequency of bypass capacitor. Also draw the input output waveform.



Solution:

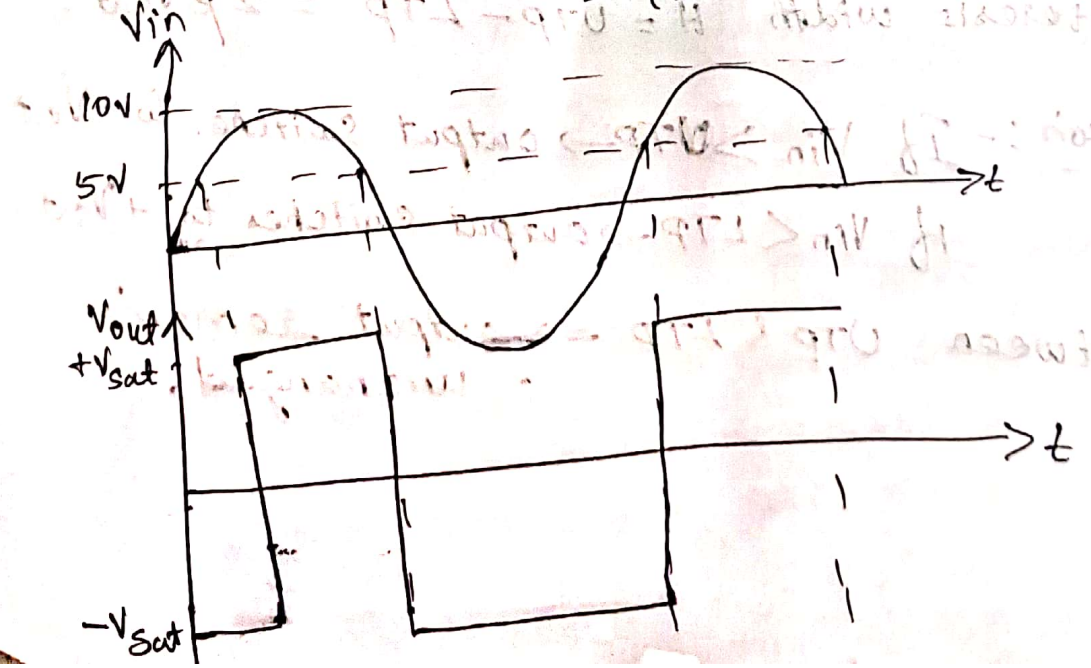
Trip point (Reference voltage) $V_{ref} = \frac{15 \times 100k}{200k + 100k}$

$= 5V$

Cutoff frequency of bypass capacitor $f_c = \frac{1}{2\pi R_{eq} C}$

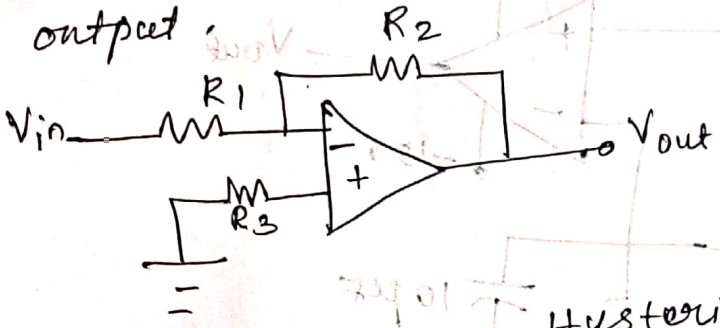
$R_{eq} = R_1 \| R_2 = 100k \| 200k = 66.67k\Omega$

$f_c = \frac{1}{2\pi (66.67 \times 10^3)(10 \times 10^{-6})} \simeq 0.24 Hz.$

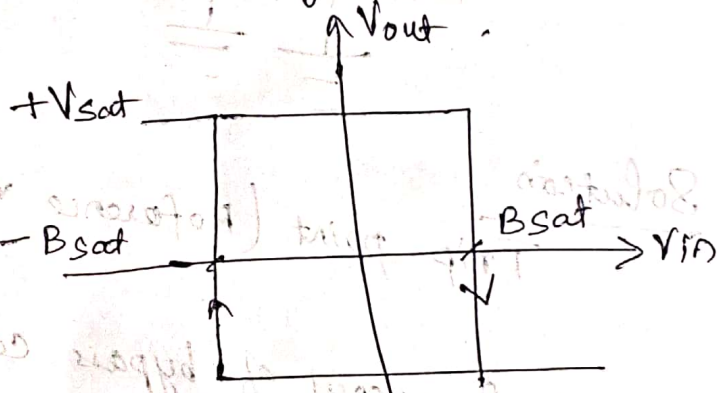


Q.5.c. Explain the operation of Inverting Schmitt-trigger with neat circuit diagram and waveform.

Schmitt trigger is a comparator with positive feedback that introduces hysteresis converting a noisy analog input into a clean digital output.



Hysteris curve.



feedback factor

$$\beta = \frac{R_1}{R_1 + R_2}$$

When output = $+V_{sat}$; $UTP = +\beta V_{sat}$.

When output = $-V_{sat}$; $LTP = -\beta V_{sat}$

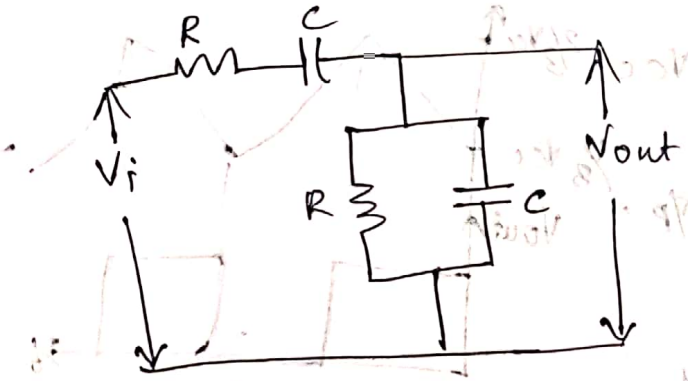
Hysteresis width $H = UTP - LTP = 2\beta V_{sat}$.

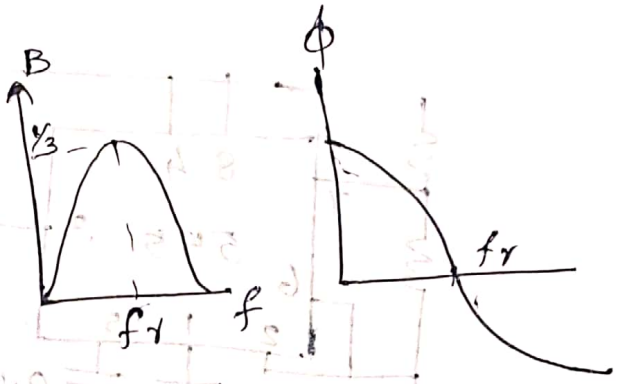
Operation :- If $V_{in} > UTP$ → output switches to $-V_{sat}$

If $V_{in} < LTP$ → output switches to $+V_{sat}$.

Between UTP & LTP → output remains unchanged.

2.b a. Make use of the concept of lead-lag circuit to explain the operation of wein bridge oscillator.





Lead lag Circuit Concept

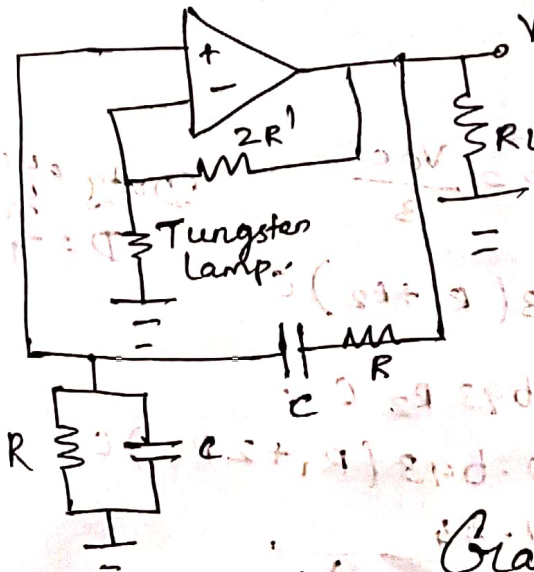
The Wien bridge uses a lead-lag RC network in the feedback path. at low frequency act as lead circuit, at high frequency act as lag circuit and at resonance, phase shift should be 0°.

at resonance $X_C = R$.

$\therefore f_o = \frac{1}{2\pi RC}$.

Barkhausen criterian $A\beta = 1$; Since $\beta = \frac{1}{3}$; $A = 3$.

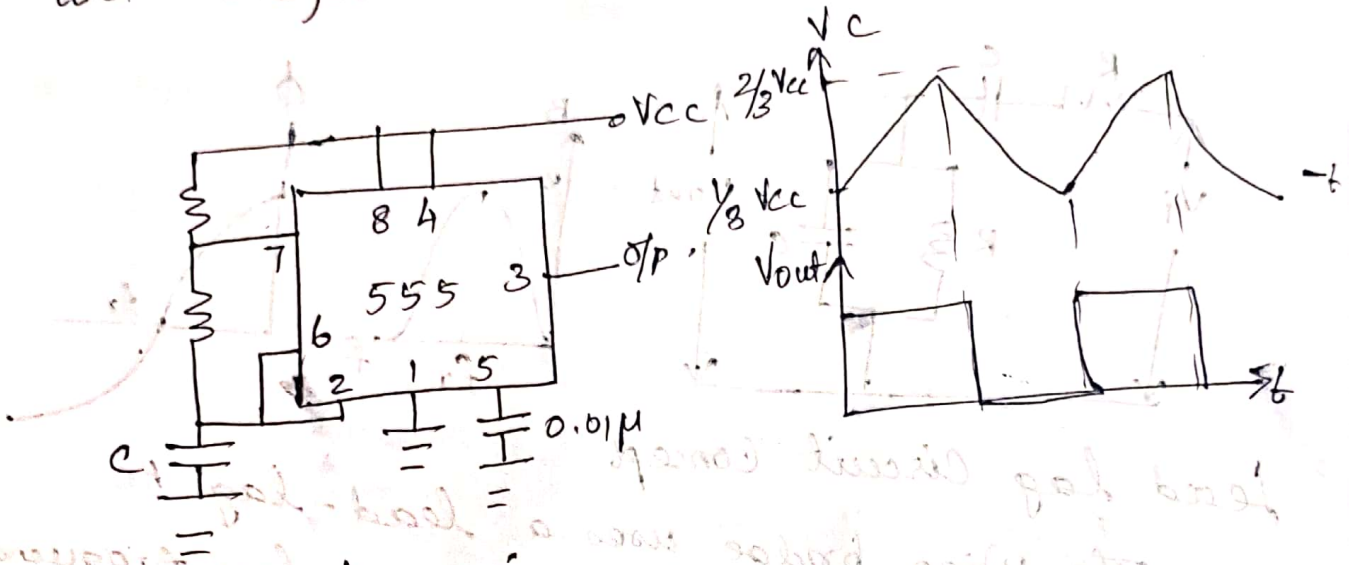
Q.6 b. Wein bridge Oscillator circuit Diagram.



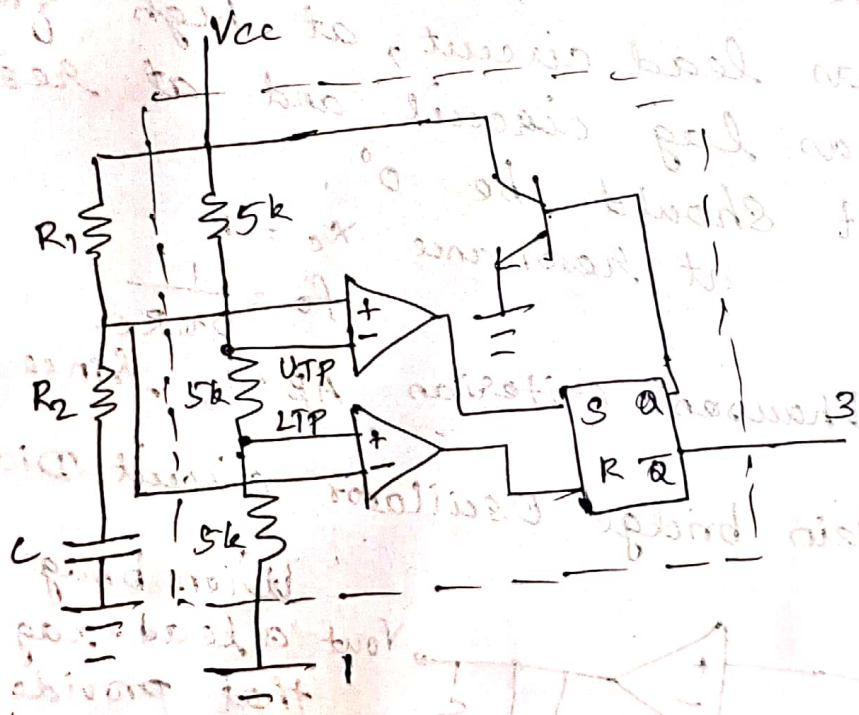
Wien bridge oscillator uses a lead-lag RC network that provides zero phase shift and $\frac{1}{3}$ feedback at $f_o = \frac{1}{2\pi RC}$. with amplifier gain set to 3, sustained Sinusoidal oscillations are produced.

$$\text{Gain} = 1 + \frac{2R'}{R} = 3 //.$$

Q.6 b) Explain the operation of Astable Multi-Vibrator using 555 timer with internal block diagram and wave forms.



Block diagram



$$UTP = \frac{+2V_{CC}}{3}, \quad LTP = \frac{V_{CC}}{3}$$

Duty cycle $D = \frac{W}{T} = \frac{R_1+R_2}{R_1+2R_2}$

Charging time, $W = 0.693(R_1+R_2)C$

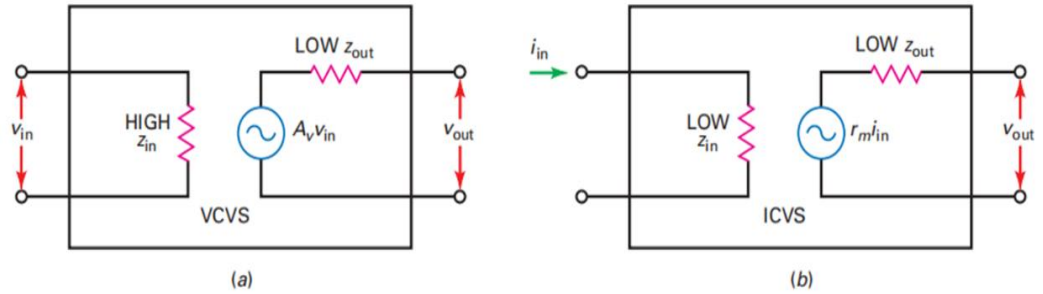
Discharging time, $d = 0.693 R_2 C$

Total time period $T = 0.693(R_1+2R_2)C$

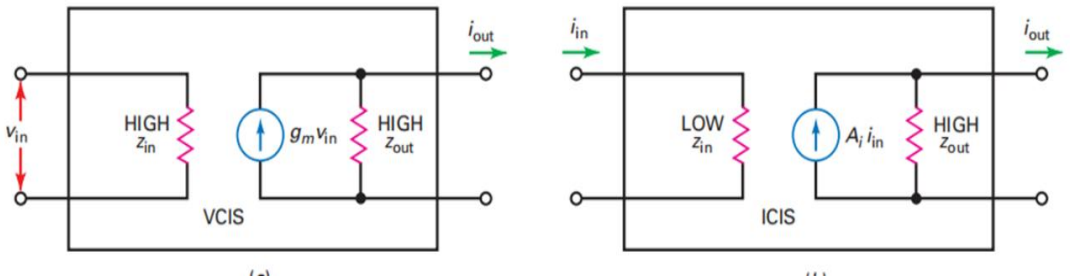
frequency, $f = \frac{1}{T} = \frac{1.44}{(R_1+2R_2)C}$

Q. 7(A)

(a) Voltage-controlled voltage source; (b) current-controlled voltage source.



(a) Voltage-controlled current source; (b) current-controlled current source.



(B)

Feedback fraction = $B = \frac{100}{100 + 3.9k} = 0.025$

Closed loop V/g gain = $\frac{1}{B} = \frac{1}{0.025} = 40$

% Error = $\frac{100\%}{1 + A_{OL}B} = \frac{100\%}{1 + 100000(0.025)} = 0.04\%$

Reduce ideal answer by 0.04%

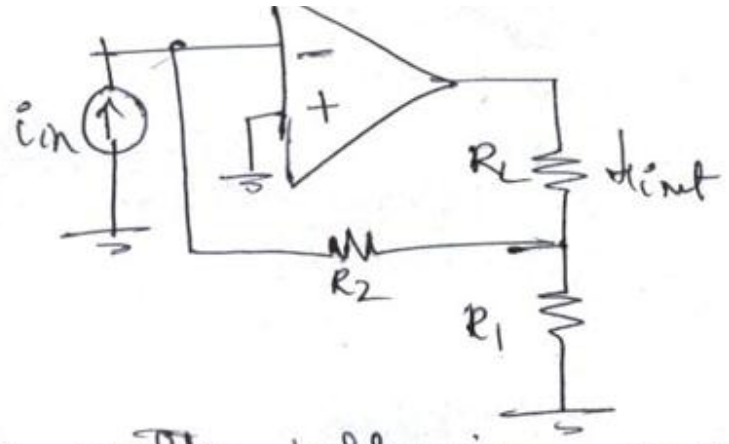
$A_V = 40 - (0.04\%)\,40 = 39.984$

With $A_V = \frac{A_{OL}}{1 + A_{OL}B} = \frac{100,000}{1 + 100000(0.025)} = 39.98$

% Error = 0.04% → obtained as before.

(C)

Circuit :



Explanation with following equations :

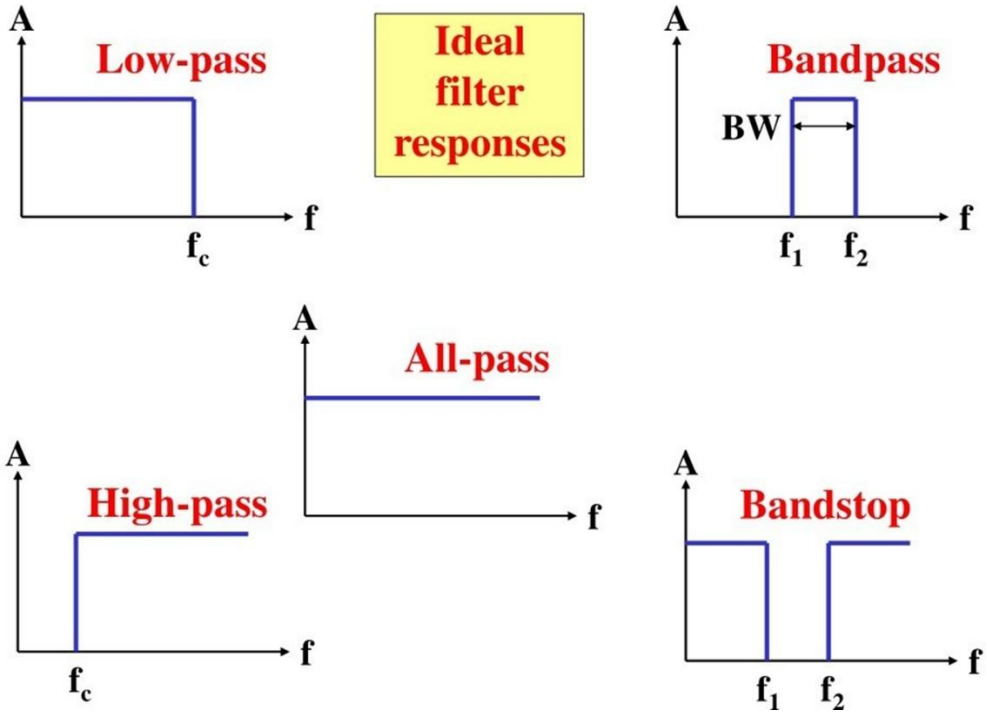
$$A_I = \frac{A_{OL}(R_1+R_2)}{R_L + A_{OL}R_1} \simeq \frac{R_2}{R_1} + 1$$

$$\text{Input impedance} = \frac{R_2}{1+A_{OL}\beta}$$

$$\beta = \frac{R_1}{R_1+R_2}$$

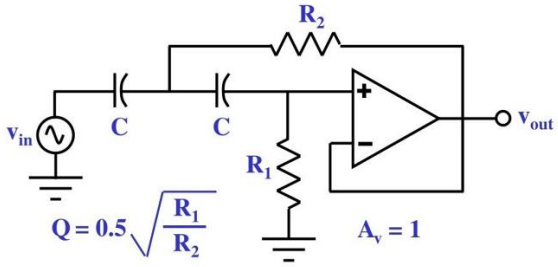
Q.8(a)

Filters in signal processing are used to selectively allow or reject specific frequency components of a signal based on their application. An ideal low-pass filter (LPF) passes all frequencies below a cutoff frequency fc and completely attenuates higher frequencies, while an ideal high-pass filter (HPF) does the opposite by blocking low frequencies and passing higher ones. A band-pass filter (BPF) allows only a specific range of frequencies between two cutoff limits f1 and f2, whereas a band-stop (notch) filter rejects frequencies within that band and passes all others. An all-pass filter permits all frequency components with equal magnitude but alters their phase response. In ideal conditions, these filters have perfectly flat passbands, zero transition width, and infinite attenuation in the stopband, resulting in a rectangular frequency response. However, such ideal filters are not physically realizable because they require non-causal, infinite impulse responses, so practical filters approximate these characteristics with finite transition bands and some ripple.



(b)

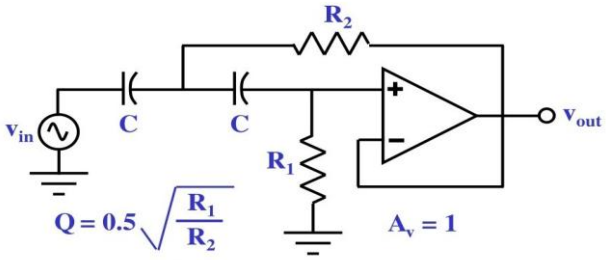
Sallen-Key second-order high-pass filter



$$Q = 0.5\sqrt{\frac{R_1}{R_2}} \qquad A_v = 1$$

$$f_p = \frac{1}{2\pi C\sqrt{R_1 R_2}}$$

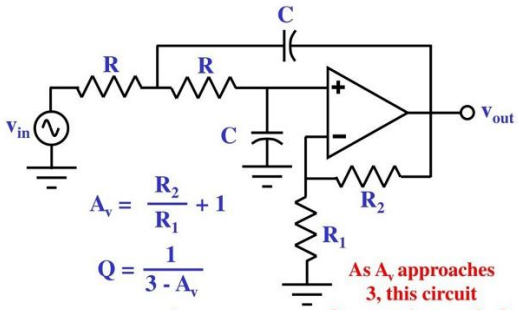
Sallen-Key second-order high-pass filter



$$Q = 0.5\sqrt{\frac{R_1}{R_2}} \qquad A_v = 1$$

$$f_p = \frac{1}{2\pi C\sqrt{R_1 R_2}}$$

Sallen-Key equal-component filter



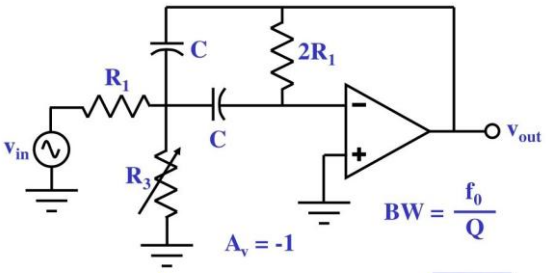
$$A_v = \frac{R_2}{R_1} + 1$$

$$Q = \frac{1}{3 - A_v}$$

$$f_p = \frac{1}{2\pi RC}$$

As A_v approaches 3, this circuit becomes impractical.

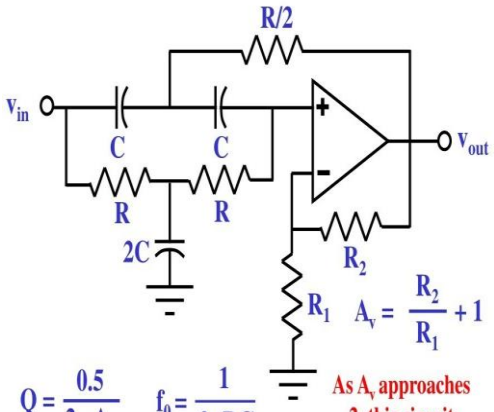
Tunable MFB bandpass filter with constant bandwidth



$$BW = \frac{f_0}{Q} \qquad A_v = -1$$

$$f_0 = \frac{1}{2\pi C\sqrt{2R_1(R_1 \| R_3)}} \qquad Q = 0.707\sqrt{\frac{R_1 + R_3}{R_3}}$$

Sallen-Key second-order notch filter

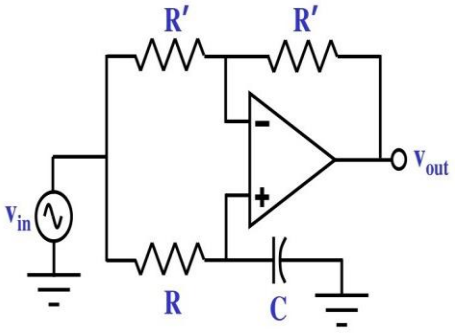


$$A_v = \frac{R_2}{R_1} + 1$$

$$Q = \frac{0.5}{2 - A_v} \qquad f_0 = \frac{1}{2\pi RC}$$

As A_v approaches 2, this circuit becomes impractical.

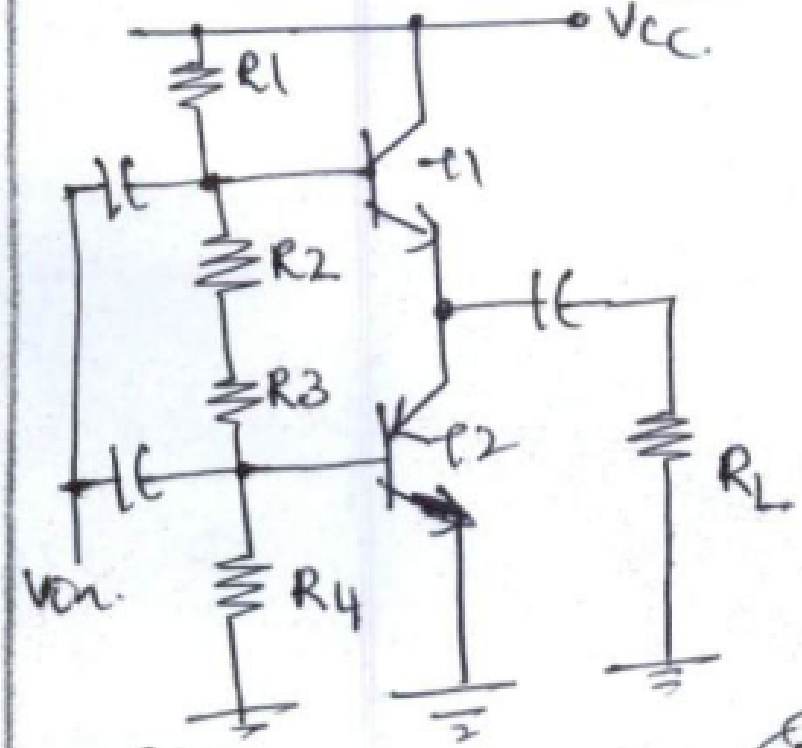
First-order all-pass lag filter



$$A_v = 1 \qquad f_0 = \frac{1}{2\pi RC} \qquad f = -2 \arctan \frac{f}{f_0}$$

9a

Circuit: → (2M.)



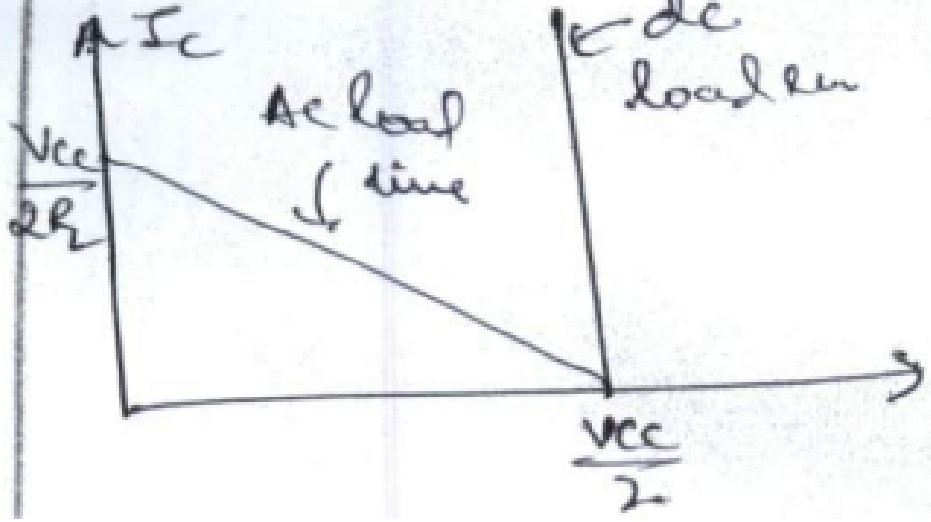
Operation: → (3M.)

→ +ve half cycle, T1 – on, T2 – off & T1 act as emitter follower

∴ % V_o = % V_i

→ -ve half cycle: T2 on; T1 – off & T2 act as emitter follower

ac & dc load line → (2M)



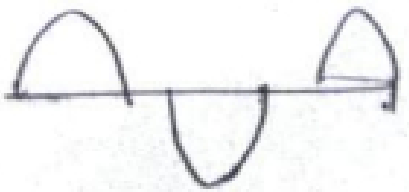
dc load line, $\frac{V_{cc}}{2}$

Adv → No transformer

Disadvantage – Crossover distortion

↓

Explain →

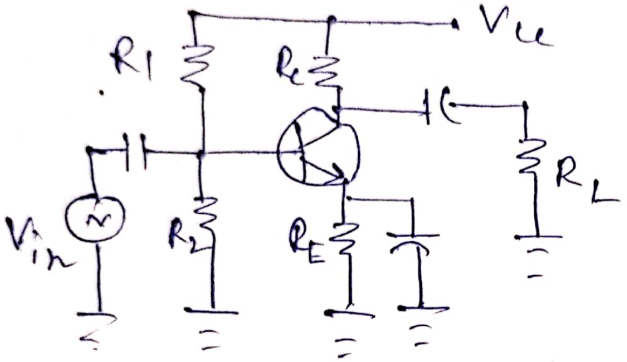


(3)

Q9.(B) (4)

(b) Explain the operation of class B push pull emitter follower amplifier with it advantages and disadvantages.

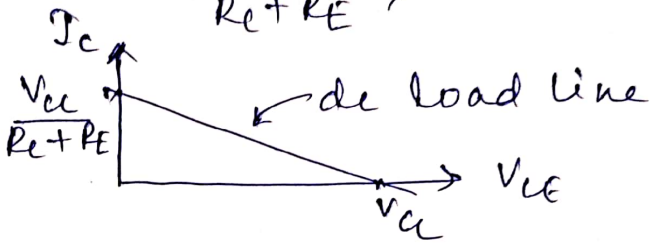
Ans: DC analysis:



Analysis + load line

$V_{cc} = I_c R_c + V_{CE} + I_E R_E$

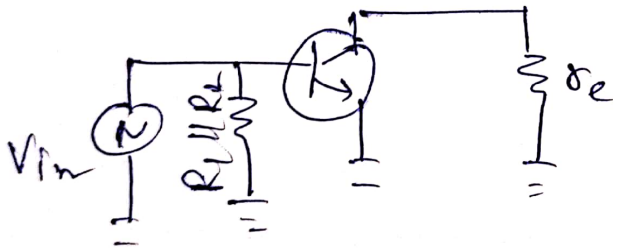
$I_c = \frac{V_{cc}}{R_c + R_E}$, $V_{CE} = V_{cc}$



AC load line:

cut + analysis

AC circuit:



$V_{ce} + i_c r_e = 0$

$i_c = -\frac{V_{ce}}{r_e}$

$i_c = \Delta I_c = I_c - I_{CQ}$

$V_{ce} = \Delta V_{CE} = V_{CE} - V_{CEQ}$

$I_c = I_{CQ} + \frac{V_{CEQ}}{r_e} - \frac{V_{CE}}{r_e}$

When Transistor is in saturation,

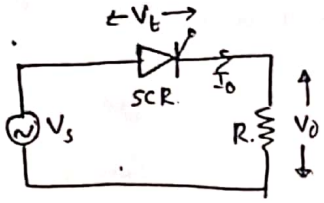
$i_{csat} = I_{CQ} + \frac{V_{CEQ}}{r_e}$

When Transistor is in cut off,

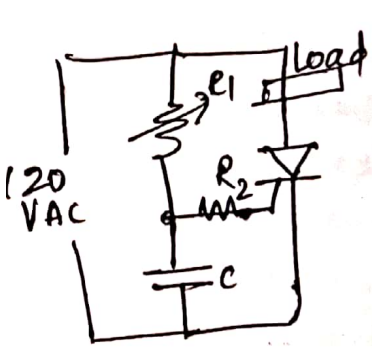
$I_c = 0 \Rightarrow V_{ce(cut\,off)} = V_{CEQ} + \Delta V_{CE}$

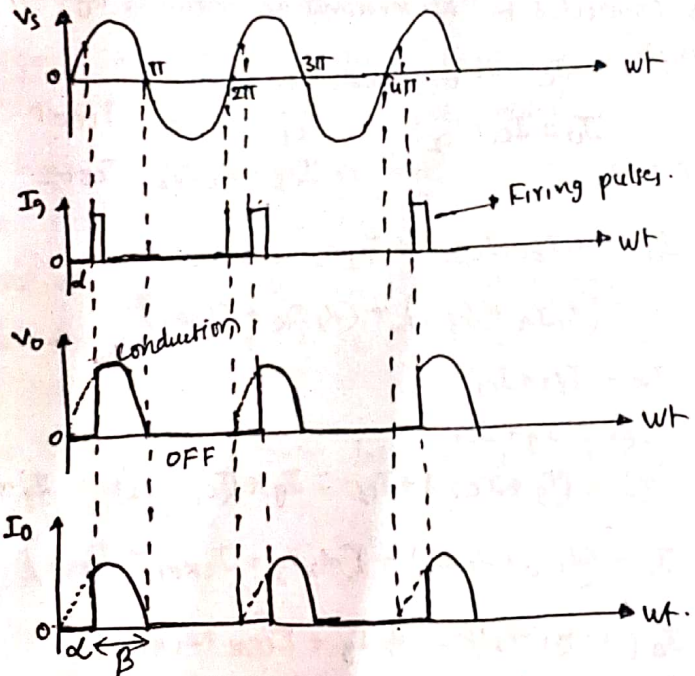
Q.10. a. Explain the working of SCR Phase control with the help of circuit and waveform.

The phase control of SCR means having control on the phase relationship between the start of the current through SCR & source voltage.



* Here the SCR is connected to the load R and a voltage source V_s. This SCR will not conduct until it is forward biased and gate signal is applied.
* The application of gate signal is called as Firing. During the positive cycle of V_s, the SCR is forward biased. If the SCR is fired it becomes ON.
* As SCR is now ON, it will start conducting. It will conduct from $\omega t = \alpha$ to π. Since load is resistive in nature, V_o and I_o will follow V_s.
* The waveforms are given by HWR





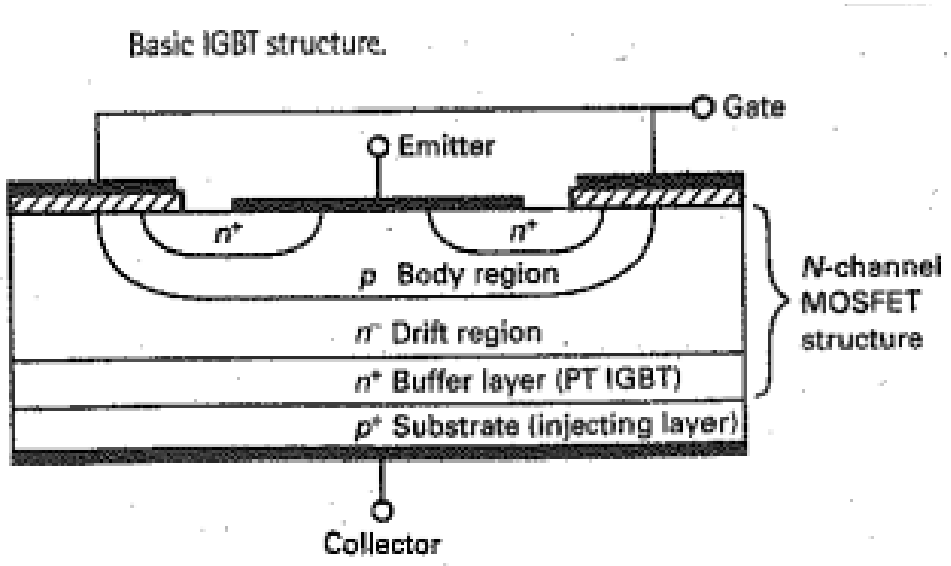
α → firing angle
β → Conduction angle.

$\alpha = \frac{t}{T} \times 180^\circ$

$\beta = (180^\circ - \alpha)$

* The SCR is getting turned ON at a phase angle of α. If α is zero then load current and source voltage will be in phase.
* If α is 90° then the load current will start when the source voltage is maximum.
* At $\omega t = 0$, SCR will get commutated as the load current becomes zero and SCR is reverse biased from π to 2π. It is called natural commutation.

Q. 10 (B)



Design:

- An Insulated Gate Bipolar Transistor (IGBT) is a semiconductor device commonly used in power electronics.
- It combines the characteristics of two types of transistors: the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and the BJT (Bipolar Junction Transistor).
- The IGBT is designed to handle high voltage and high current while offering the fast switching capabilities of MOSFETs and the low conduction loss of BJTs.

Advantages of IGBT:

- High Efficiency: Low conduction losses combined with the ability to switch at moderate speeds allow for efficient power conversion.
- Compactness: IGBTs can handle large amounts of power in a relatively small package.
- Durability: They can operate at high temperatures and handle significant electrical stresses.