



# CBCS SCHEME

21CS33

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026

## Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. Explain relaxation oscillator. (06 Marks)
- b. Explain current to voltage converter. (06 Marks)
- c. Describe the working of Schmitt trigger circuit (non inverting) with transfer characteristics. (08 Marks)

OR

- 2 a. What is Biasing? List the types of Biasing and discuss fixed bias. (06 Marks)
- b. Explain the different components of regulated power supply. (06 Marks)
- c. Explain with neat diagram, R-2R ladder type D to A converter. (08 Marks)

### Module-2

- 3 a. Reduce the following function using K-map technique and implement the expression with basic gates:  
 $f(a, b, c, d) = \sum m(0, 1, 6, 8, 9, 11) + \sum d(3, 7, 14, 15)$  (10 Marks)
- b. Find a minimum sum-of-products form using the Q-M method for given function.  
 $f(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$  (10 Marks)

OR

- 4 a. For a given function determine minimal sum using MEV technique. Use d as MEV variable.  
 $f(a, b, c, d) = \sum m(3, 4, 5, 7, 8, 11, 12, 13, 15)$ . (06 Marks)
- b. With an example, explain Petrik's method. (06 Marks)
- c. Simplify the following pos expression using K-map:  
 $f(a, b, c, d) = \prod M(0, 1, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15)$  (08 Marks)

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### Module-3

- 5 a. What is Hazard? List the types of hazard. Explain static 0 and static 1 hazard. (08 Marks)
- b. Implement the following functions using 3:8 decoder  
 $f_1(a, b, c) = \sum m(0, 4, 6, 7)$   
 $f_2(a, b, c) = \sum m(1, 4, 5)$  (06 Marks)
- c. With a neat sketch, explain the structure of PLA. (06 Marks)

OR

- 6 a. Explain the importance of three-state buffer. (06 Marks)
- b. What is programmable logic array? How does PLA differ from PAL? (06 Marks)
- c. Explain multiplexer with an example. Realize the 8:1 multiplexer using 2:1 and 4:1 MUX. (08 Marks)

### Module-4

- 7 a. Explain master-slave J-K flip flop operation. (08 Marks)
- b. Explain with a neat diagram, VHDL program structure. (06 Marks)
- c. Give VHDL code for 4:1 multiplexer using conditional assignment statement. (06 Marks)

OR

- 8 a. Derive characteristics equation for JK, T, D and SR flip flop. (08 Marks)
- b. Explain switch debouncing with an SR latch. (06 Marks)
- c. Write the VHDL code for JK flip-flop. (06 Marks)

### Module-5

- 9 a. With a neat diagram, explain n-bit parallel adder with accumulators. (10 Marks)
- b. Design Mod-8 counter using JK flip flop. (10 Marks)

OR

- 10 a. With neat diagram, explain SISO register. (10 Marks)
- b. Design a synchronous counter for the given sequence. Using JK flip flop.  
 $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$  (10 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.