



Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain Basic functional units of a computer. (10 Marks)
- b. List the rules governing addition and subtraction of n-bit signed numbers using 2's complement representation system. Perform addition and subtraction of the following:
Addition :) +7 and -3) -5 and -2
Subtraction :) +2 from -3) +1 from -7 (06 Marks)
- c. Explain Memory locations and Addresses. (04 Marks)

OR

- 2 a. Write a program for adding n numbers using straight line sequencing and branching (loop). Also explain condition codes. (10 Marks)
- b. Explain basic operational concepts. (06 Marks)
- c. Explain briefly bus structure. (04 Marks)

Module-2

- 3 a. Define Addressing Modes. Explain the following addressing modes with examples.
i) Register Mode ii) Absolute mode iii) Immediate Mode
iv) Index Mode (10 Marks)
- b. Explain the following Assembler Directives
i) EQU ii) ORIGIN iii) RESERVE iv) END (04 Marks)
- c. Develop an assembly code that packs two BCD digits (06 Marks)

OR

- 4 a. Explain Basic Input /Output operations. (10 Marks)
- b. Explain with neat diagram, stack operation. Also write a routine for safe pop and safe push operation. (06 Marks)
- c. Develop an assembly code to compute the sum of n numbers using indirect addressing mode. (04 Marks)

Module-3

- 5 a. Explain with neat diagram I/O interface for an input device. (08 Marks)
- b. Develop an assembly code that reads one line from the keyboard, stores it in memory buffer and echoes it back to the display. Also explain status and control registers in keyboard and display interfaces. (08 Marks)
- c. Explain about registers in DMA interface. (04 Marks)

OR

- 6 a. What is Interrupt? List the sequence of events involved in handling an interrupt request from a single device. (08 Marks)
- b. Explain with neat diagram, use of DMA controller in a computer system. Also explain registers in a DMA interface. (08 Marks)
- c. Explain simultaneous requests in multiple devices. (04 Marks)

Module-4

- 7 a. Explain with neat diagram, organization of bit cells it's a memory chip. (08 Marks)
- b. Define Static Memory. Explain read and write operation in a static RAM cell and a CMOS memory cell. (08 Marks)
- c. With a neat diagram explain a ROM cell. (04 Marks)

OR

- 8 a. With a neat diagram develop internal organization of a 2 M × 8 dynamic memory chip. (08 Marks)
- b. Explain organization and accessing of data on a disk. Also write in brief virtual memory organization. (08 Marks)
- c. Explain in brief about Flash Memory. (04 Marks)

Module-5

- 9 a. Explain with neat diagram, single bus organization of the data path inside a processor. (08 Marks)
- b. Explain the connection and control signals for register MDR for the instruction Move (R1), R2 with actions needed to execute the instruction. (08 Marks)
- c. Explain Microroutine for the instruction Branch < 0. (04 Marks)

OR

- 10 a. With action develop the control sequence for execution of the instruction Add (R3), R1. (08 Marks)
- b. Explain Hard-wired control unit organization with diagram and generation of the z_{in} control signal for the processor. (08 Marks)
- c. Explain control sequence for an unconditional branch instruction. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.