CBCS SCHEME

USN | | | | | | | | | |

BEC306C

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat diagram, describe the functional units of a computer.	8	L2	CO1
	b.	Explain following with an example: i) One address instruction ii) Two address instruction iii) Three address instruction	6	L2	CO1
	c.	Write a short note: i) Basic Performance equation ii) Clock rate	6	L2	CO1
		OR			
Q.2	a.	With a neat diagram, explain basic operational concept of computer.	7	L2	CO1
	b.	With help of example, explain little Endian and Big Endian byte assignment with a neat diagram.	6	L2	CO1
	c.	Explain memory operations.	7	L2	CO1
		Module – 2			
Q.3	a.	Define Assembler Directives. Explain various assembler directives used in Assembly language program.	10	L2	CO2
	b.	Define subroutine and parameter passing. Explain how to pass the parameter by value and by reference.	10	L2	CO2
		OR			
Q.4	a.	Define stack, explain PUSH and POP operations on stack with neat diagram.	10	L2	CO2
	b.	Explain shift and rotate operations with examples.	10	L2	CO2
		Module – 3			
Q.5	a.	Define Interrupt. Explain the various ways of enabling and disabling interrupts.	10	L2	CO3
	b.	Explain DMA technique and its importance.	10	L2	CO3

		OR			
Q.6	**a.**	Explain different ways of handling multiple I/O devices.	10	L2	CO3
	b.	Illustrate interrupt priority scheme with neat diagram.	10	L2	CO3
		Module – 4			
Q.7	**a.**	Explain the principle of working of magnetic disk.	10	L2	CO4
	b.	Explain the internal organization of 1K × 1 dynamic memory chip with neat diagram.	10	L2	CO4
		OR			
Q.8	**a.**	Explain the interfacing of the main memory to the processor.	10	L2	CO4
	b.	Explain virtual memory organization with a neat diagram.	10	L2	CO4
		Module – 5			
Q.9	**a.**	Explain single bus organization of the datapath inside a processor with neat diagram.	10	L2	CO5
	b.	Discuss hardwired control unit organization relevant diagram.	10	L2	CO5
		OR			
Q.10	**a.**	Explain complete processor with neat diagram.	10	L2	CO5
	b.	Develop the complete control sequence for the executing instruction Add (R_3), R_1.	10	L2 L3	CO5

* * * * *