CBCS SCHEME

USN | | | | | | | | | | 18EC56

Fifth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain typical design flow for designing VLSI IC circuit using the flow chart. **(10 Marks)**

b. Explain 4 – bit ripple carry counter. **(10 Marks)**

OR

2 a. Explain top-down and bottom –up design methodology with an example. **(10 Marks)**

b. What are the two styles of Stimulus Applications? Explain each method in brief. **(10 Marks)**

Module-2

3 a. Explain the following verilog data types with an example.
i) Net's ii) Registers iii) Integers
iv) Parameters v) Arrays. **(10 Marks)**

b. With neat block diagram, explain the components of verilog module. **(10 Marks)**

OR

4 a. What are the different ports in verilog? Explain Internal and External port connections Rules. **(08 Marks)**

b. Explain the following lexical conventions.
i) Whitespace
ii) Operators
iii) Strings
iv) Keywords **(06 Marks)**

c. With an example, explain Hierarchical names. **(06 Marks)**

Module-3

5 a. Explain different types of gate delays. **(06 Marks)**

b. Explain and , or, Not gates with respect to logic symbols, gate instantiation and truth tables. **(06 Marks)**

c. Write a verilog dataflow description for 4 – bit full adder with carry look ahead. **(08 Marks)**

OR

6 a. Explain the following:
i) Bitwise operators ii) Relational operators **(08 Marks)**

b. Write verilog code for 4:1 multiplexer using gate level modeling. **(06 Marks)**

c. Explain regular assignment delay, implicit assignment dealy and net declaration delay. **(06 Marks)**

Module-4

7 a. Explain sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog program for 4 :1 multiplexer using case statement. **(06 Marks)**

c. Write the differences between task and functions. **(06 Marks)**

OR

8 a. Explain the following with proper examples.
i) For Loop ii) Repeat iii) Forever loop iv) While loop **(08 Marks)**

b. Explain constant function and signed function. **(06 Marks)**

c. Explain Event – Based timing control with example. **(06 Marks)**

Module-5

9 a. Explain logic synthesis flow from RTL to gates. **(08 Marks)**

b. Explain any 3 useful system tasks with examples. **(06 Marks)**

c. Explain conditional compilation and execution with examples. **(06 Marks)**

OR

10 a. Explain different overriding parameters with example. **(06 Marks)**

b. Write RTL code for magnitude comparator. **(06 Marks)**

c. Explain the Basic Computer -Aided logic synthesis process. **(08 Marks)**

* * * * *