

# CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

21EC63

Sixth Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026

## VLSI Design and Testing

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Explain the working nMOS transistor and pMOS transistor with neat diagram. (10 Marks)  
b. Realize the CMOS gate for the following functions with truth table :

i)  $Y = \overline{(A,B) + (C,D)}$ .

ii)  $Y = \overline{(A + B + C).D}$ .

(10 Marks)

OR

- 2 a. Explain the implementation of  
i) CMOS positive edge triggered D flip flop  
ii) CMOS positive level sensitive Latch. (10 Marks)  
b. Draw the circuit diagram of a CMOS inverter and with the help of transfer characteristics explain various regions of operation with necessary equations. (10 Marks)

### Module-2

- 3 a. With neat diagram explain Lambda based design rules for wires, contact cuts and transistors. Also explain buried contact and butting contact with neat diagram. (10 Marks)  
b. With neat flow diagram explain the VLSI design flow. (10 Marks)

OR

- 4 a. Explain the various steps in the fabrication of simple CMOS inverter. (10 Marks)  
b. Draw the CMOS stick diagram for  $Y = \overline{A.B + C.D + E}$  (04 Marks)  
c. With equivalent R C circuit models for NMOS and PMOS transistor of width K, explain the equivalent circuit of fan – out of -1 inverter with negligible wire capacitance. (06 Marks)

### Module-3

- 5 a. Explain the operation of 4 \* 4 NOR based ROM array with neat diagram. (07 Marks)  
b. With neat diagram explain resistance load SRAM cell. (07Marks)  
c. Explain with neat diagram the organization of typical Random access memory array. (06 Marks)

OR

- 6 a. With neat diagram explain the various configurations of static RAM cell. (10 Marks)  
b. With the aid of proper diagrams explain the working three transistor DRAM cell. (10 Marks)

**Module-4**

- 7 a. Explain stuck – at faults and stuck-open faults in CMOS circuits with an example. (10 Marks)  
 b. Explain the following with respect to D – Algorithm.  
 i) Singular cover  
 ii) Propagation D cubes  
 iii) Primitive D cube of a fault. (10 Marks)

OR

- 8 a. Explain Delay fault detection. Also explain Nonrobust and robust delay tests. (10 Marks)  
 b. Explain breaks or open types of faults in CMOS circuits. (05 Marks)  
 c. What are temporary faults? Explain. (05 Marks)

**Module-5**

- 9 a. Define the terms controllability and observability with an example. (06 Marks)  
 b. Explain the various phases involved in checking experiment based on sequential structure. (06 Marks)  
 c. Explain the concept of clocked hazard free latches used in the LSSD technique, accompanied by neat logic diagram. (08 Marks)

OR

- 10 a. Explain how sequential circuits can be tested by modeling than as iterative combinational circuits. (05 Marks)  
 b. Explain any two Adhoc design rules for improving testability. (05 Marks)  
 c. Given the state table in Table 1, determine the following  
 i) The response for input sequence | 0 |  
 ii) The homing tree for the state table  
 iii) The distinguishing tree for state table.

Present state	Input	
	X = 0	X = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

(10 Marks)

\*\*\*\*\*