



CBCS SCHEME

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18EC72

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026

VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Obtain the transfer characteristics of a CMOS inverter and mark all the regions showing the status of PMOS and NMOS transistor. (10 Marks)
- b. Sketch a transistor level schematic of a CMOS 2 input XNOR gate for both true and complementary versions of the input available. (10 Marks)

OR

- 2 a. Explain the following :
 - (i) Channel length modulation
 - (ii) Mobility degradation and velocity saturation. (10 Marks)
- b. Explain the operation of MOSFET with necessary diagrams. Also derive the equation for drain current linear and saturation region of operation. (10 Marks)

Module-2

- 3 a. Draw the stick diagram, and layout for the expression, $y = A(B + C) + DE$ (10 Marks)
- b. Discuss in detail the lambda based design rules for nMOS and PMOS layers and transistors and contact cut. (10 Marks)

OR

- 4 a. Using neat diagram, describe fabrication steps of P-well CMOS process. (10 Marks)
- b. Define scaling. Explain different types of scaling and mention its advantages and disadvantages. (10 Marks)

Module-3

- 5 a. Explain Elmore delay model with suitable example. (06 Marks)
- b. Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagrams.
 - (i) 2 input NAND gate (08 Marks)
 - (ii) 3 input NOR gate. (06 Marks)
- c. Briefly discuss about input ordering delay effect. (06 Marks)

OR

- 6 a. Explain pseudo nMOS logic circuit operation. Implement three input NAND gate using pseudo nMOS logic. (06 Marks)
- b. Explain logical effort calculation in multistage logic network. (08 Marks)
- c. Write short note on :
 - (i) Cascade voltage switch logic (06 Marks)
 - (ii) Skewed gates

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Module-4

- 7 a. Explain 3 stages of a depletion load nMOS dynamic shift register driven with two phase clocking. (10 Marks)
- b. Explain basic principles of pass transistor circuit of logic '1' transfer with necessary derivations. (10 Marks)

OR

- 8 a. Explain charge storage and leakage concept with respect to pass transistor logic with necessary expressions. (10 Marks)
- b. Explain the following :
 - (i) Clocked CMOS (C²MOS)
 - (ii) Pulsed latches (10 Marks)

Module-5

- 9 a. With necessary circuit diagram, explain the operation of SRAM. (10 Marks)
- b. Explain the following :
 - (i) Logic verification
 - (ii) Debugging
 - (iii) Manufacturing test (10 Marks)

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OR

- 10 a. What is fault model? Explain stuck at fault model, short circuit and open circuit fault models with an example. (10 Marks)
- b. Explain in brief the approaches used in design for testability. (10 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.