CBCS SCHEME

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18CS34

Third Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the basic operational concepts of a computer with the help of a neat block diagram. **(08 Marks)**

b. Analyze big-endian and little-endian methods of byte addressing with proper examples. **(08 Marks)**

c. Differentiate between byte addressable and word addressable memory with examples. **(04 Marks)**

OR

2 a. What are the different types of Addressing modes in machine instructions? Explain any three with example. **(08 Marks)**

b. Analyze the call and return instructions in a subroutine with assembly language program code. **(08 Marks)**

c. Explain shift and rotate operations with example. **(04 Marks)**

Module-2

3 a. Describe the working of interrupt hardware. How does it improve the efficiency of I/O operations? **(08 Marks)**

b. Explain centralized bus arbitration with a suitable example. **(08 Marks)**

c. Analyze the 'Cycle stealing' and 'Burst mode' with respect to DMA. **(04 Marks)**

OR

4 a. With a block diagram, explain how the keyboard is connected to the processor. **(08 Marks)**

b. Explain the use of PCI bus in a computer system with neat sketch. **(08 Marks)**

c. Analyze polling with its advantages and disadvantages. **(04 Marks)**

Module-3

5 a. Explain the organization of 2M × 8 dynamic memory chip. **(08 Marks)**

b. Analyze the working of static RAM memories and asynchronous DRAMS. **(08 Marks)**

c. Explain the tree structure of USB with split bus operation. **(04 Marks)**

OR

6 a. With a neat diagram, explain direct mapped cache in mapping functions. **(08 Marks)**

b. Calculate the average access time experienced by a processor if the cache hit rate is 0.88, penalty is 0.015 ms and cache access time is 10 ms. **(08 Marks)**

c. Analyze the concept of memory interleaving. **(04 Marks)**

Module-4

7 a. Explain different types of number representation with examples and draw the addition/subtraction logic unit. **(06 Marks)**

b. Perform the following operations on 5 bit signed numbers using 2's complement representation.
(i) (–7) + (–08)
(ii) (–10) – (+4)
(iii) (–3) + (–8)
(iv) (–10) – (+5) **(08 Marks)**

c. Explain a 4-bit carry-look ahead adder with a neat diagram. **(06 Marks)**

OR

8 a. Perform division of the number 9 by 3 using the restoring division algorithm. Write the steps involved. **(06 Marks)**

b. Explain Booth Multiplication Algorithm and apply it to multiply the signed numbers – 5 and 4. **(08 Marks)**

c. Describe integer division with a neat diagram. **(06 Marks)**

Module-5

9 a. Apply the sequence of operations required to execute the following instruction:
Add(R_3), R_1 **(10 Marks)**

b. Explain the three bus organization of a data path with a neat diagram. **(10 Marks)**

OR

10 a. Compare and contrast the following :
(i) Hardwired control
(ii) Micro programmed control **(10 Marks)**

b. What is Pipelining? Explain the four-stage pipeline with instruction execution steps and hardware organization. **(10 Marks)**

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