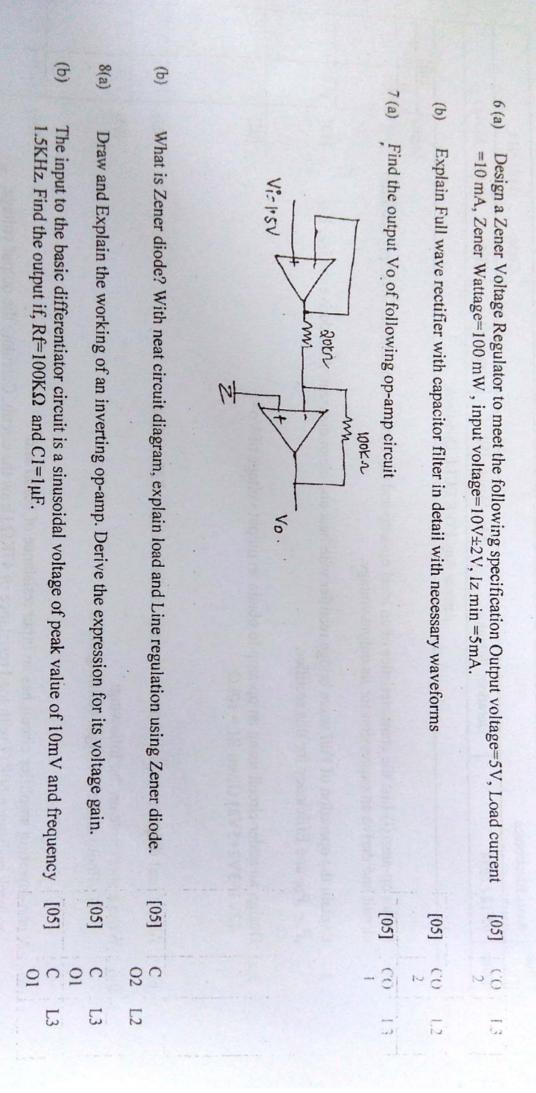
(b)	4(a)	(b)							7		
	4		3(a)	2	-		Date:	Sub		CMR INST TECH	
A non-inverting amplifier circuit has an input resistance of $10 \mathrm{K}\Omega$ and feedback resistance $60 \mathrm{K}\Omega$, with load resistance of $47 \mathrm{K}\Omega$. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is $1.5 \mathrm{V}$.	Write a short note on the following: (i) Photo diode (ii) Light emitting diode	With a neat diagram, explain how an op-amp can be used as a differentiator.	Design an adder circuit using an op-amp to obtain an output voltage of Vo=-[2V1+3V2+5V3] Given Rf = 10kΩ	Explain the operation of Full wave bridge rectifier with neat and clean diagram. Also derive the I_{DC} , I_{RMS} , P_{DC} , and Efficiency for this rectifier.	For an op-amp (i) List the characteristics of an ideal op-amp and (ii) Draw the three input inverting summer circuit and derive an expression for its output voltage.		05/12 / 2018	Basic Electronics		CMR INSTITUTE OF TECHNOLOGY	
ircuit has ar with load ro hen the inp	llowing: ght emitting	in how an o	ng an op-an Rf = 10kΩ	all wave bri	characteristi		Duration:				
input resist esistance of ut voltage is	diode	p-amp can b	np to obtain a	dge rectifier er.	ics of an idea	Answe	90 mins			USN	
ance of 10KΩ and 47KΩ.Draw the circuit. (1.5V.		e used as a differentiator.	an output voltage of Vo=	with neat and clean diagr	al op-amp and (ii) Draw t	Answer Any FIVE FULL Questions	Max Marks: 50		Internal Assesment Test - II	C	
Calculate the out				am. Also derive	he three input inv	ons	Sem: I				
out voltage,				the I _{DC} , I _{RMS}	erting summ		SEC:	Code:			
[53]	[05]	[05]	[05]	[10]	Marks ner [10]		I,J,K,L,M,N,O	18ELN14			
COI	(0)	(0)	COI	C'02	88		N,0			SA SA	_
ప		1.2	5.5	[2]	OBE RBT L3					NSTITUTE OF	(20)

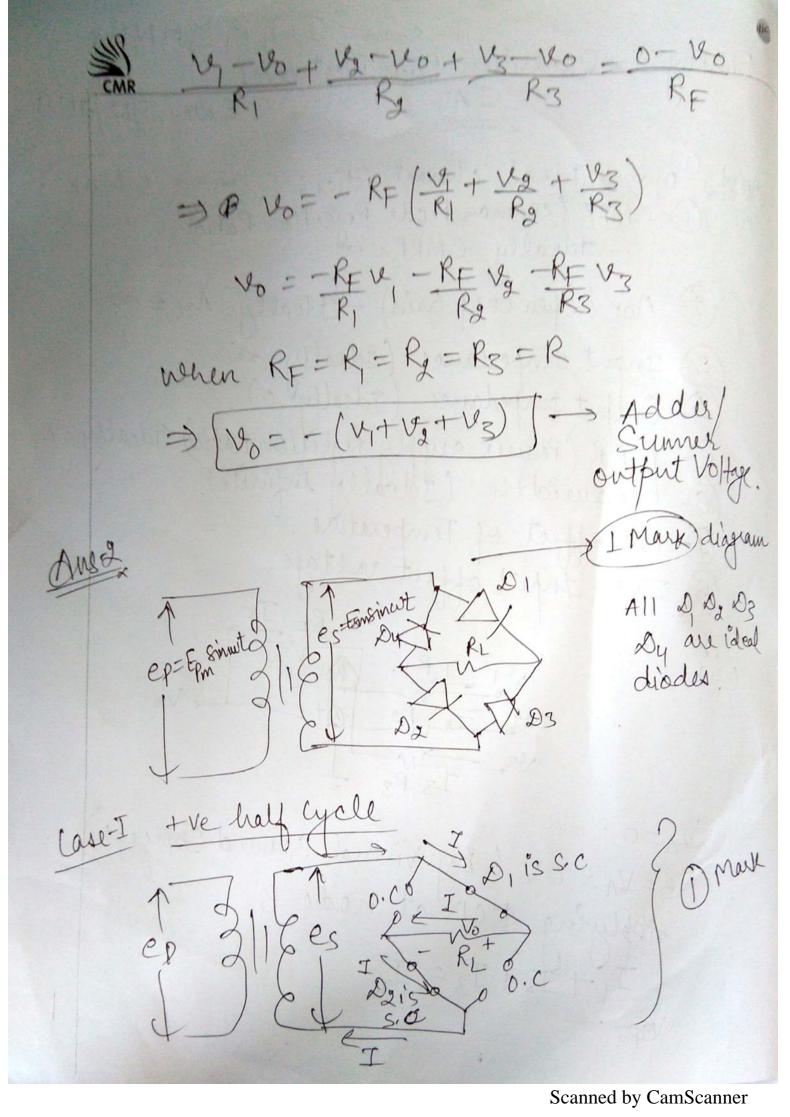


Marking Scheme Q Colution Basic Electronics

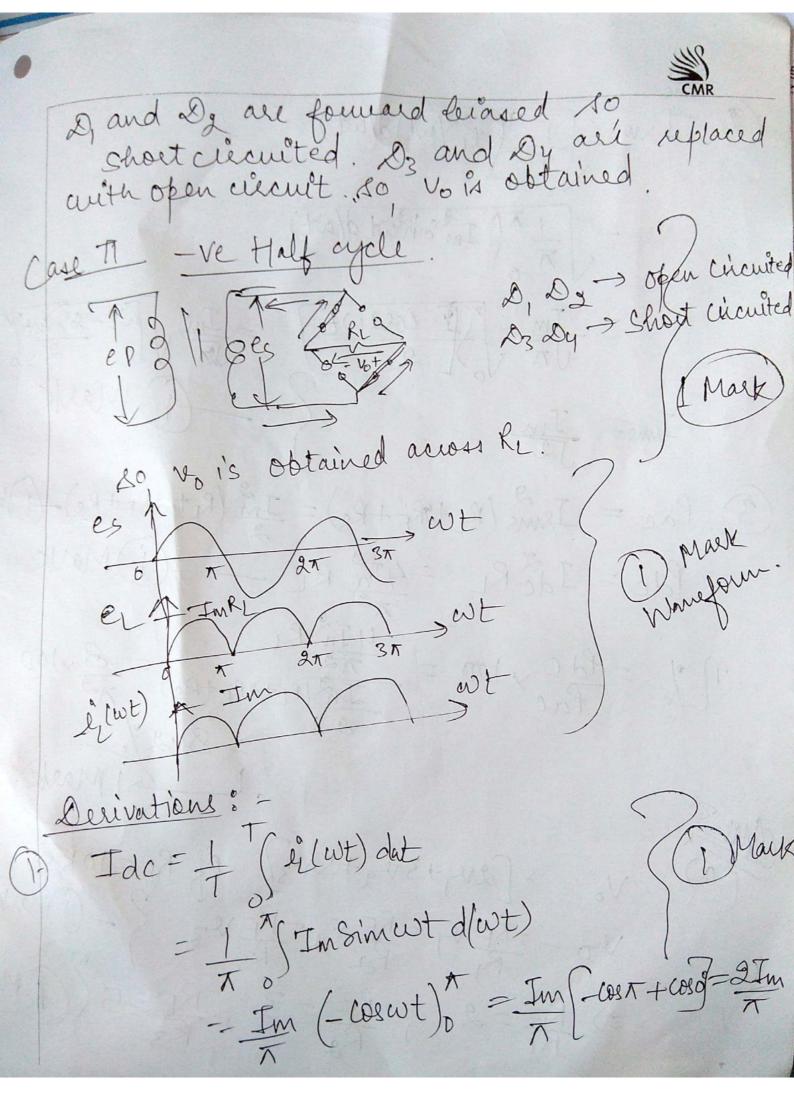
Marking Scheme Q Colu One Common Made Rejection Ratio)

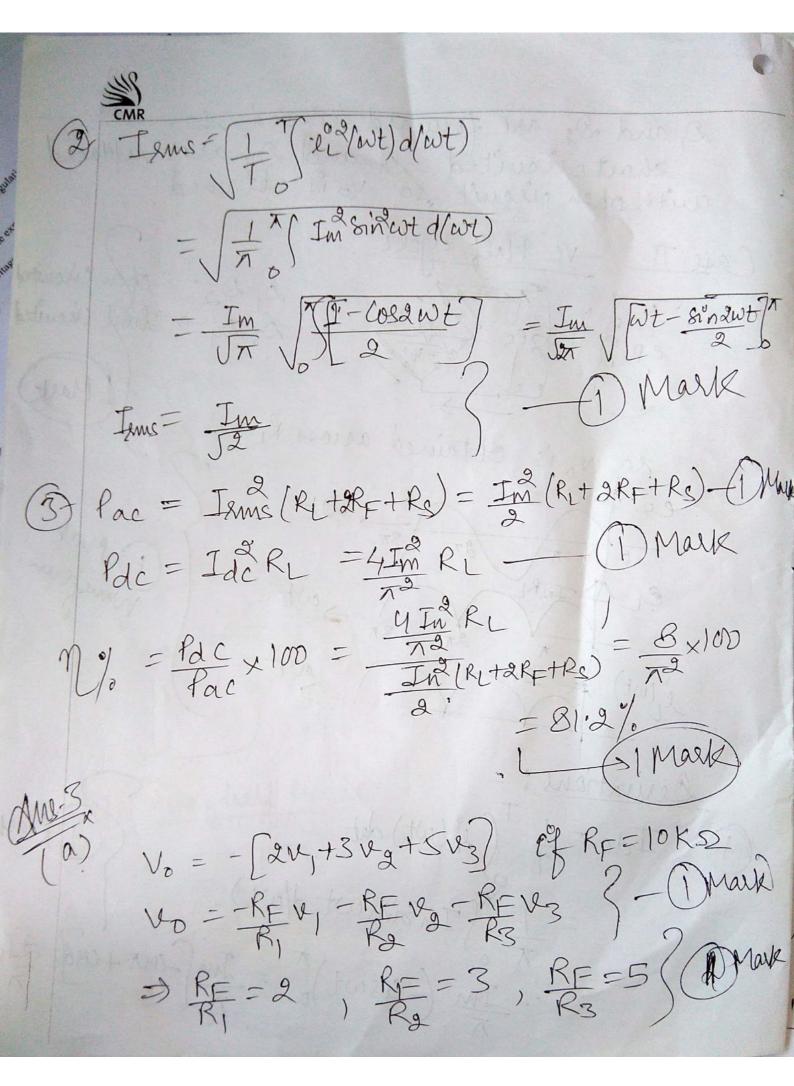
Adeally CMRR = & (2) Au Lopen Loop Gain) - Ideally Aor = 00 3) Input Impedance (Ideally 0) 4) Output surpedance (Ideally 0) SPERR (Power supply Rejection Ratio) Adeally = 0 6) Bandwidth (Ideally Infinite). D NO effect of Temperature. 3) zero Inpuil offset voltage. RF. IF Je Tarke B VB = VA = OV (By Virtual Ground Concept).

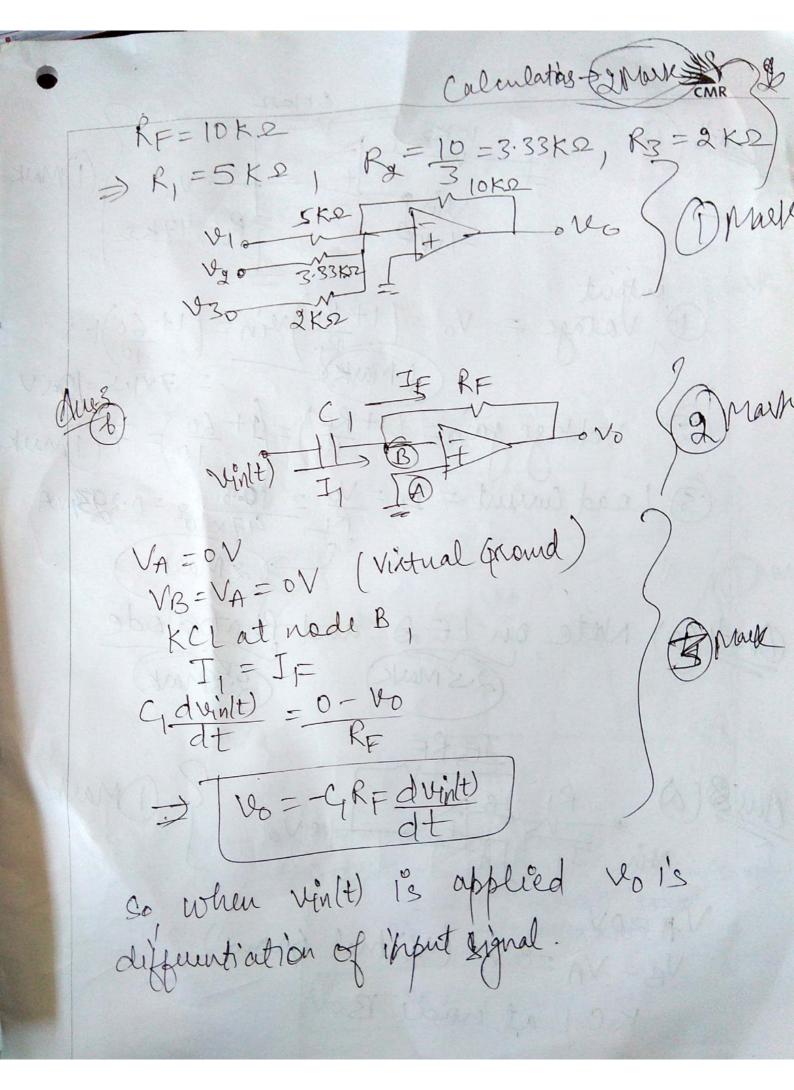
Applying KCL at node B, ゴーナなり I3= IF

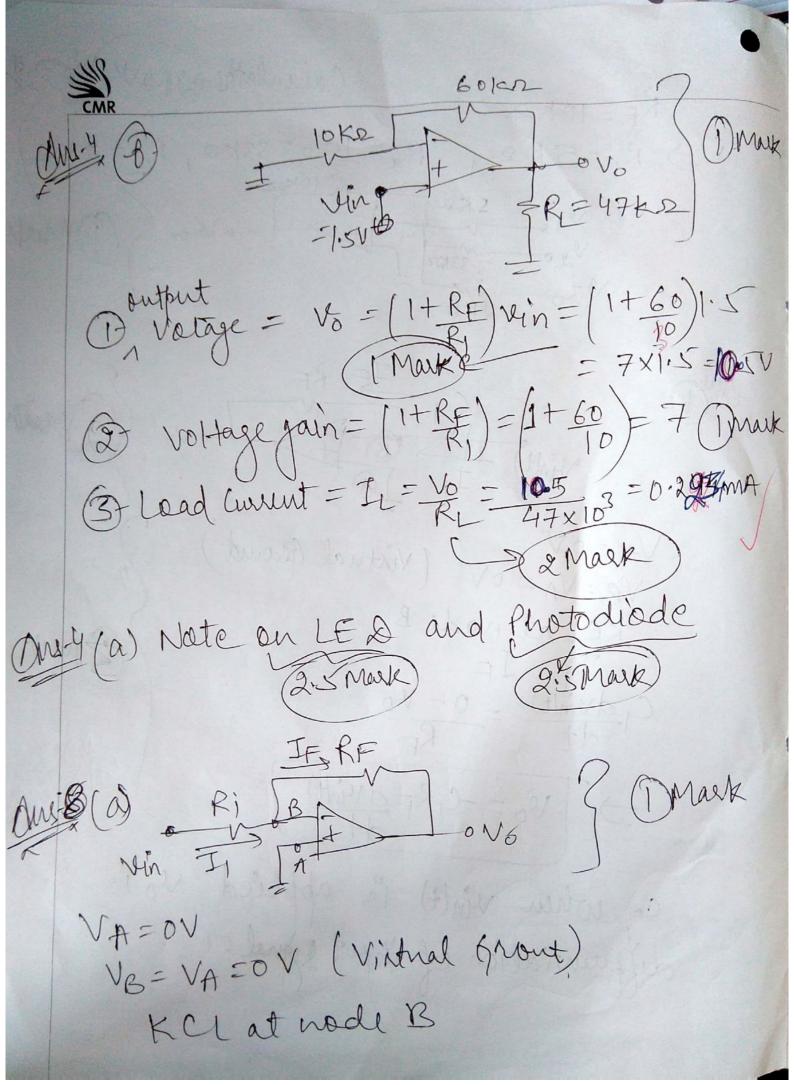


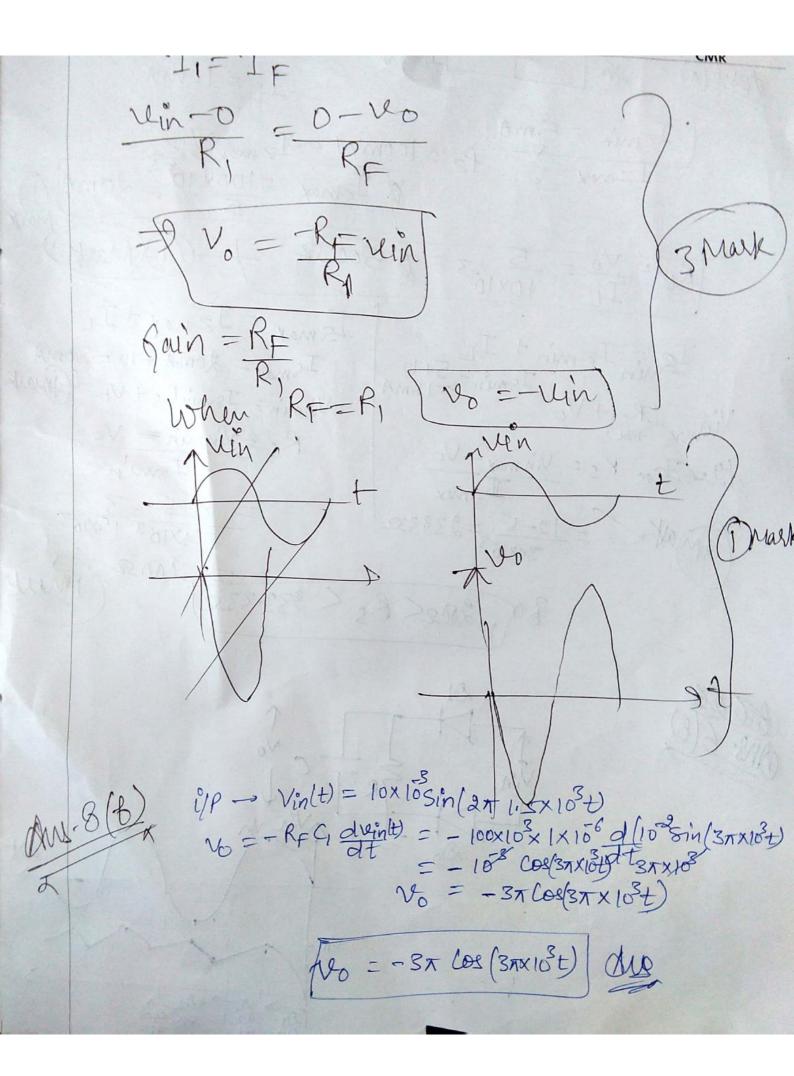
Scanned by CamScanner

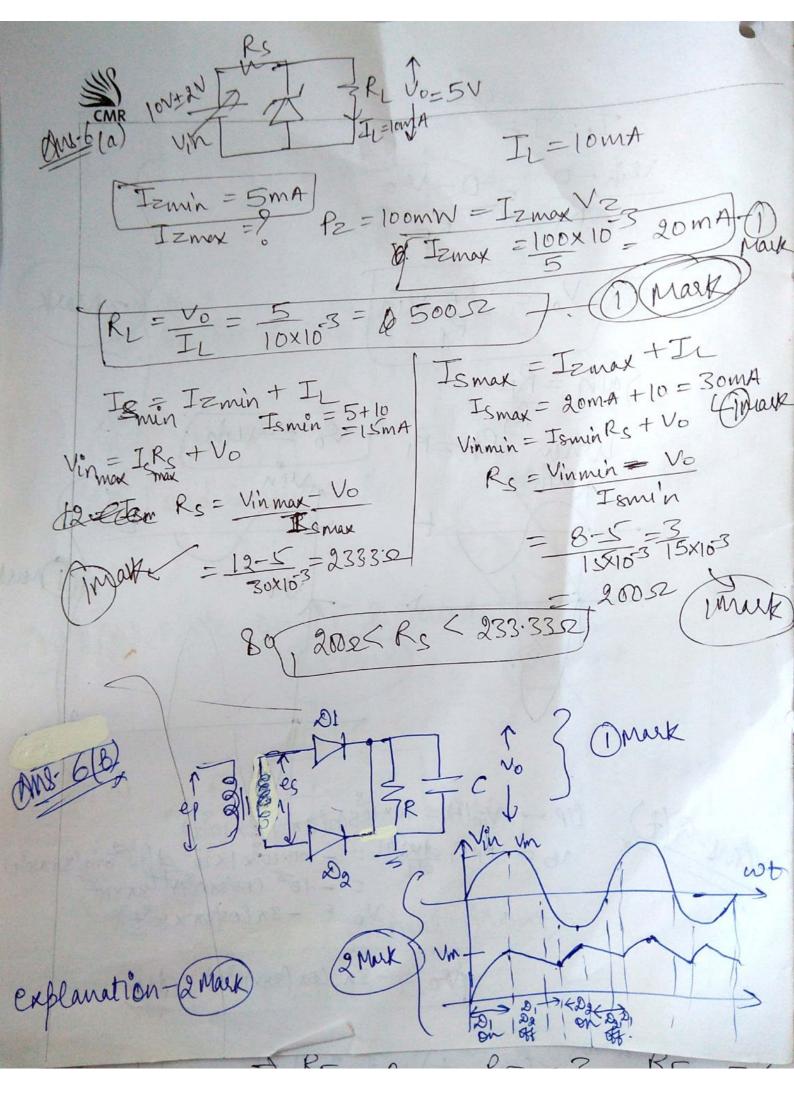












Scanned by CamScanner