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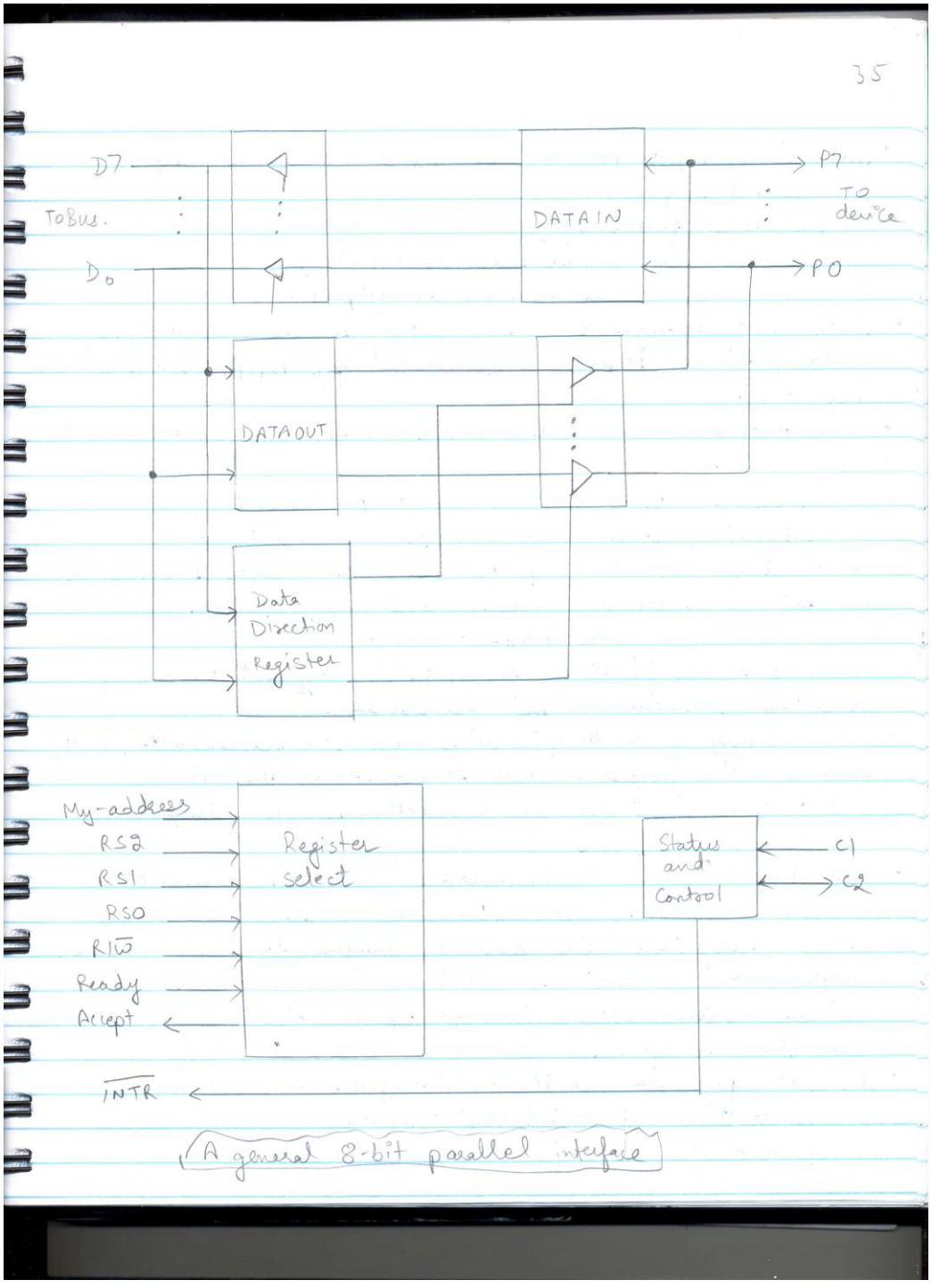
Internal Assesment Test 2 – OCT. 2018- Scheme and Solution

Sub:	COMPUTER ORGANIZATION					Sub Code:	17CS34	Branch:	CSE	
Date:	/ 10 / 2018	Duration:	90 mins	Max Marks:	50	Sem / Sec:	3(A,B,C)			OBE

Answer **FIVE** FULL questions selecting AT LEAST ONE question **FROM EACH PART**

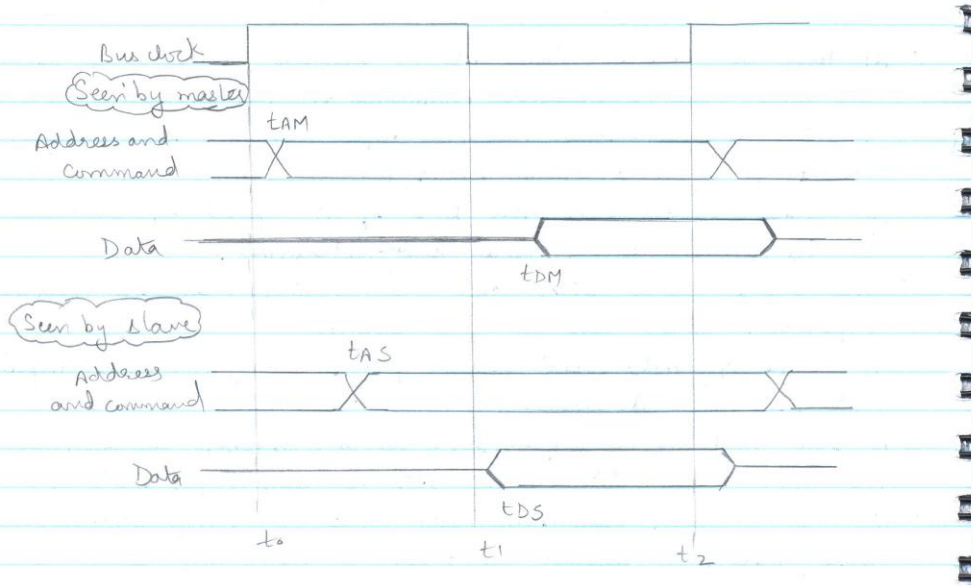
		MARKS	CO	RBT
	PART A			
1 (a)	With a neat diagram, explain general 8-bit Parallel interface. (diagram -5 explanation-5)	[10]	CO2	L2



Data lines P_7 to P_0 can be used for either input or output purposes.
For increased flexibility,
→ some lines can be used as inputs, and
→ some lines can be used as outputs.
The DATAOUT register is connected to data lines via 3-state drivers that are controlled by DDR (Data Direction Register).
The processor can write any 8-bit pattern into DDR.
If DDR = 1,
Then, dat line acts as an output-line;
otherwise, data-line acts as an input-line.
Two lines, C_1 and C_2 are used to control the interaction between interface-circuit and I/O device.
These two lines are programmable.
Line C_2 is bidirectional to provide different modes of signaling, including the handshake.
The Ready and Accept lines are the handshake control lines on the processor-bus side. Hence, the Ready and Accept lines can be connected to the ~~output of~~ Master-ready and Slave-ready.
The input signal My-address should be connected to the output of an address decoder. The address decoder recognizes the address assigned to the interface.
There are 3 register select lines: $RS_0 - RS_2$.
Three register select lines allow up to eight registers in the interface.
An interrupt-request INTR is also provided. It should be connected to the interrupt-request line on the computer bus.

OR

2 (a)	With neat timing diagrams, explain synchronous bus. (diagram-8 explanation-2)	[10]	CO2	L2



Detailed timing diagram for input transfer

→ The master sends the address and command signals on the rising edge of ~~ϕ~~ at beginning of clock period 't_0'. But this signal actually will not appear on the bus until 't_{AM}' due to delay in the bus ~~to~~ driver circuit.

→ A while later at time 't_{AS}' the signal reaches the slave.

→ The slave decodes the address at 't_1' and sends the requested data. Here also, data signals donot appear on the data lines until 't_{DS}', as data is to be taken from memory.

→ Data travels towards master and arrives at time 't_{DM}'.

→ At time 't_2', the master loads the data to its buffer. Here time $t_2 - t_{DM}$ is the setup time for the master's input buffer.

Response signals from the device inform the master that the slave has recognized its address and that it is ready to participate in a data-transfer operation. These signals also make it possible to adjust the duration of the data transfer period to suit to the needs of the participating devices. A high-frequency clock signal is used such that a complete data transfer cycle would span several clock cycles. No. of clock cycles involved can vary from one device to another.

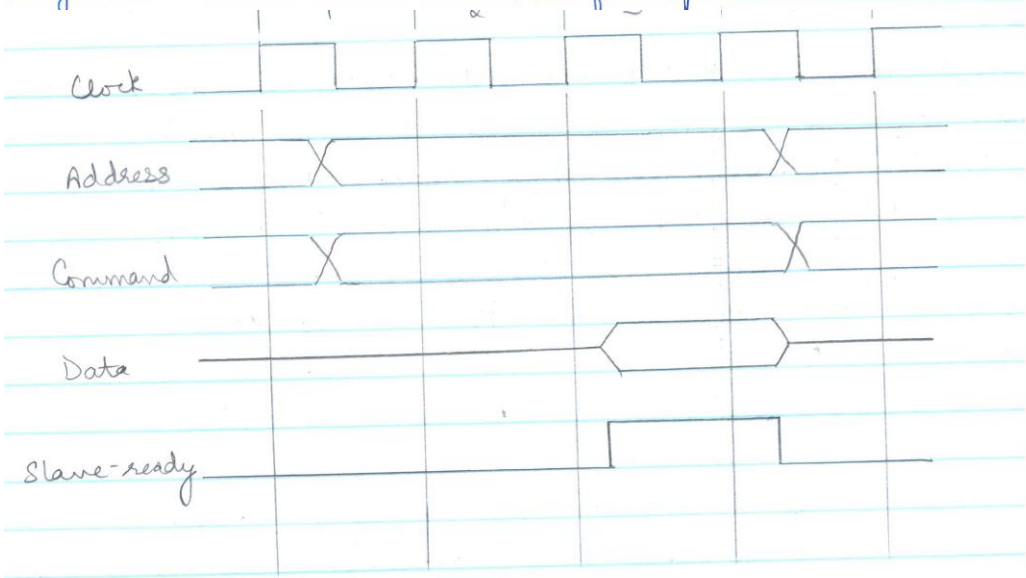
In the figure on previous page, during clock cycle 1, the master sends address and command to the bus, requesting a 'Read' operation.

At the beginning of clock cycle 2, the slave makes the decision to respond and begins access to the requested data.

At clock cycle 3, slave places acknowledgement for the request and the requested data on the bus.

The master strobes the data from the bus at the end of the 3rd cycle, and stores in buffer.

The bus transfer operation is now complete and processor may start with new data transfer operation.



An input transfer using multiple clock cycles.

PART B

3 (a)	Explain SCSI bus. (Introduction-, phases- 2, read operation-2, timing diagram-2)	[10]	CO2	L2

(2) SCSI (Small Computer System Interface) Bus.

- It is a standard bus defined by ANSI (American National St
  and Institute).
- It has several options :
  - → Narrow bus – 8 data lines, transfers 1 byte at a time.
  - → Wide bus – 16 data lines, transfers 2 byte at a time
  - → Single-ended (SE) – each signal uses one wire, with a comm
    Transmission ground return for all signals.
  - → Differential – Separate return wire for each signa
    Signaling

2 voltage levels possible

HVD	LVD
High Voltage Differential)	(Low Voltage Differential)
5 V	3.3 V

Because of these various options, SCSI connector may have 50, 68 or 80 pins. The data transfer rate ranges from 5 M to 160 MB/s, 320 MB/s, 640 MB/s.

Transfer rate depends on:
- → length of cable
- → Number of devices connected.

Bus length may be limited to achieve high data transfer rate. However, manufacturers often provide special bus expanders to connect devices that are farther away.

A single read or write request may involve several bursts of data. SCSI protocol is designed to support the transfer of multiple bursts of data which may result in

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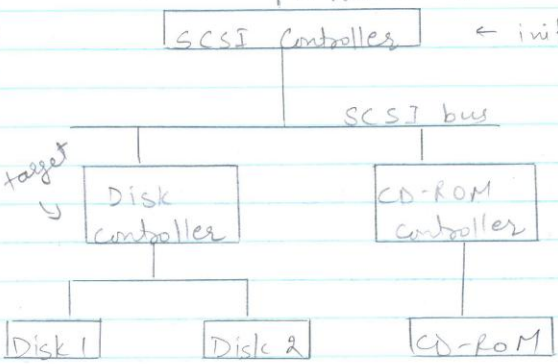
accessing several disk sectors that may not be ~~contiguous~~ contiguous.



- The SCSI bus is connected to the processor-bus through SCSI controller.
- A controller connected to SCSI bus is one of two types:

→ Initiator - It has ability to select a particular target & to send commands specifying the operation to be performed. These are controllers on the processor side.
Eg- SCSI controller in above diagram

→ Target - It carries out commands it receives from the initiator
Eg- Disk controller in above diagram
The initiator establishes a logical connection with the intended target.

- Data transfers on SCSI bus are always controlled by the target controller. To send a command to a target, an initiator requests control of the bus and, after winning arbitration, selects the controller it wants to communicate with and hands control of the bus over to it (target).

OR

4 (a) Consider sixteen words and each word having eight bits. Draw internal organization of the specified RAM memory chip. [10] CO5 L3
(diagram-7, explanation-3)

- Memory-cells are organized in the form of array (Figure 8.2).
- Each cell is capable of storing 1-bit of information.
- Each row of cells forms a memory-word.
- All cells of a row are connected to a common line called as **Word-Line**.
- The cells in each column are connected to **Sense/Write** circuit by 2-bit-lines.
- The Sense/Write circuits are connected to data-input or output lines of the chip.
- During a write-operation, the sense/write circuit
  → receive input information &
  → store input info in the cells of the selected word.

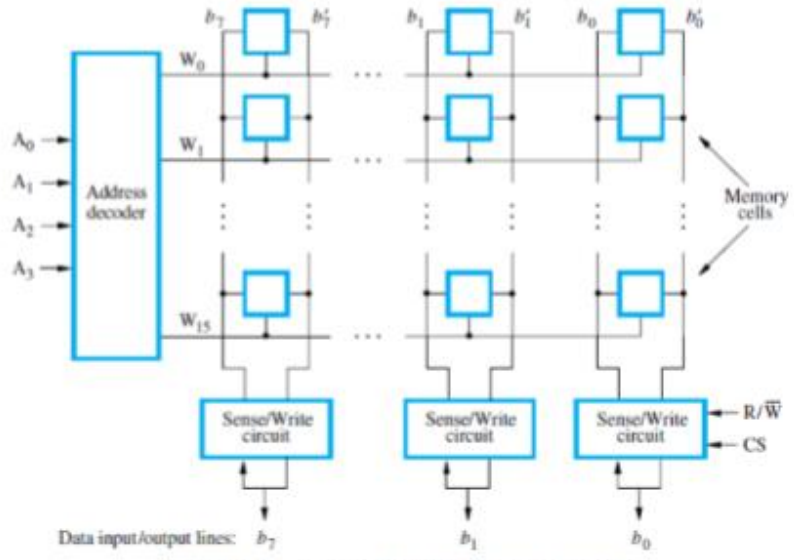


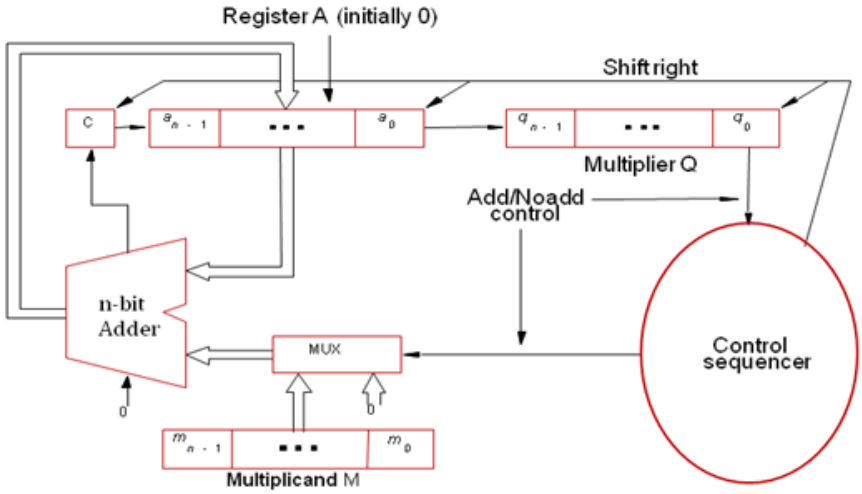
Figure 8.2 Organization of bit cells in a memory chip.

- The data-input and data-output of each Sense/Write circuit are connected to a single bidirectional data-line.
- Data-line can be connected to a data-bus of the computer.
- Following 2 control lines are also used:
  1) R/W' → Specifies the required operation.
  2) CS' → Chip Select input selects a given chip in the multi-chip memory-system.

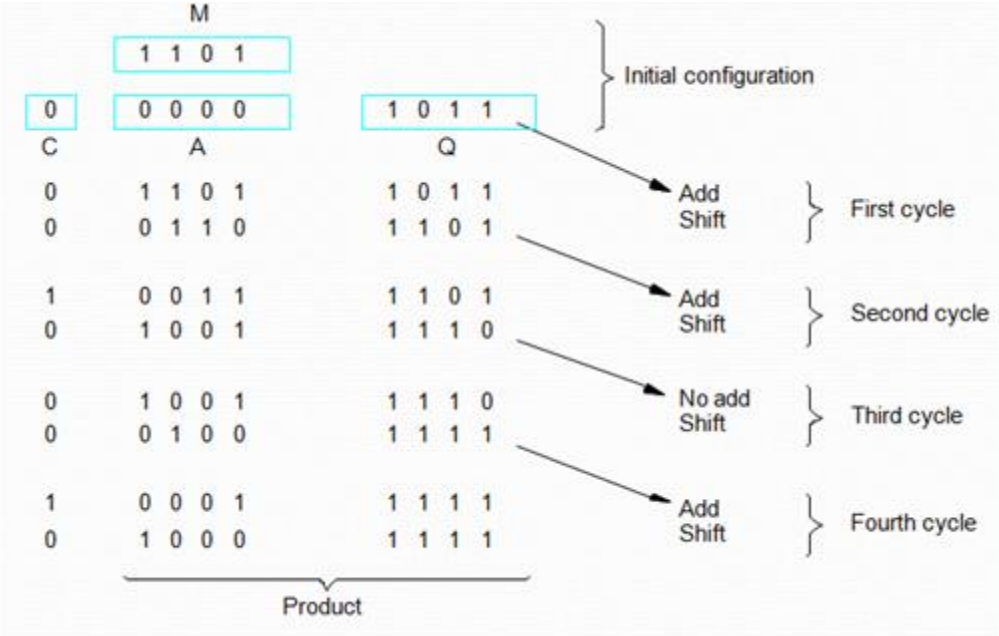
5 (a)		[10]	CO3	L3
6 (a)		[5]	CO3	L3
(b)	Perform multiplication for -27 and +11 using Bit-pair recoding. Answer= -297	[5]	CO3	L3

PART D

7 (a)	Explain hardware arrangement for sequential multiplication (diagram-5, explanation-5)	[10]	CO3	L2



Sequential circuit binary multiplier/ register configuration for hardware arrangement for sequential multiplication



OR

8 (a)	**PART C** With a figure, explain circuit arrangement for binary division. (Diagram-5, any one algorithm-5)	[10]	CO3	L2

- An n-bit positive-divisor is loaded into register M.
  An n-bit positive-dividend is loaded into register Q at the start of the operation.
  Register A is set to 0 (Figure 9.21).
- After division operation, the n-bit quotient is in register Q, and
  the remainder is in register A.

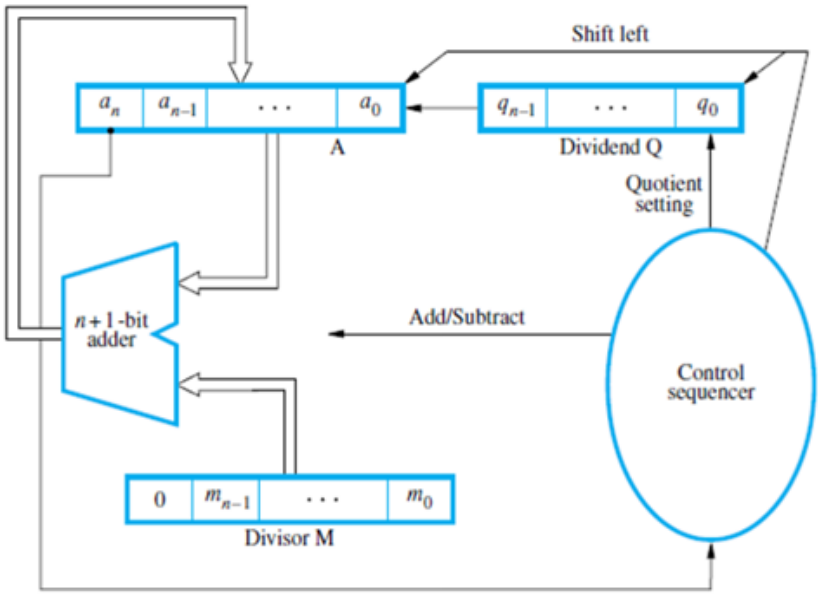


Figure 9.23 Circuit arrangement for binary division.

NON-RESTORING DIVISION

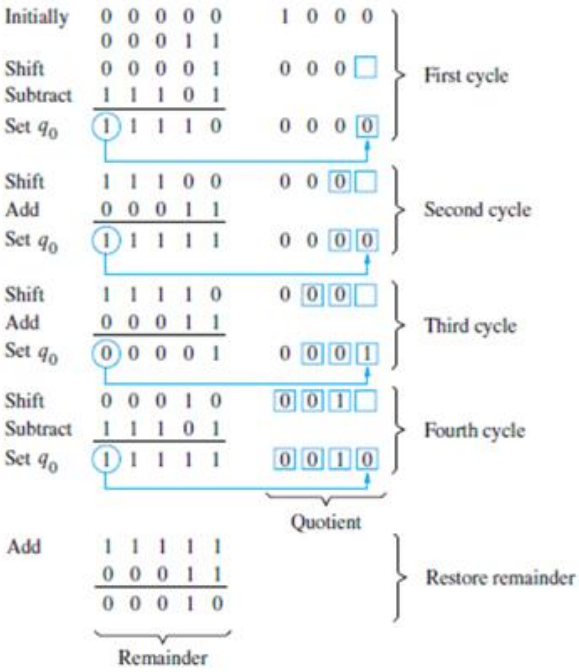
- Procedure:

  Step 1: Do the following n times

  i) If the sign of A is 0, shift A and Q left one bit position and subtract M from otherwise, shift A and Q left and add M to A (Figure 9.23).

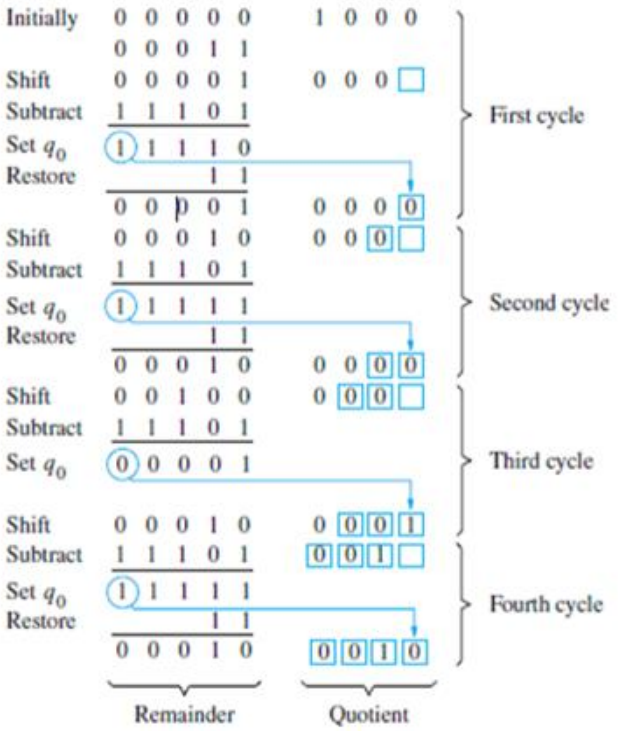
  ii) Now, if the sign of A is 0, set q_0 to 1; otherwise set q_0 to 0.

  Step 2: If the sign of A is 1, add M to A (restore).



RESTORING DIVISION

- Procedure: Do the following n times
  1) Shift A and Q left one binary position (Figure 9.22).
  2) Subtract M from A, and place the answer back in A
  3) If the sign of A is 1, set q_0 to 0 and add M back to A(restore A).
     If the sign of A is 0, set q_0 to 1 and no restoring done.



Explain 16-bit carry look-ahead adder.
(diagram-4, derivation-6)

Carry-Lookahead adder (CLA)

Improving speed of addition will improve speed of all other arithmetic operations.

CLA improves speed by reducing carry propagation delay. It calculates carry signal in advance, based on input signals instead of waiting for them to ripple through the adders.

Recall the equations:

$$s_i = x_i \oplus y_i \oplus c_i$$

$$c_{i+1} = x_i y_i + x_i c_i + y_i c_i$$

Second equation can be written as:

$$c_{i+1} = x_i y_i + (x_i + y_i) c_i$$

We can write:

$$c_{i+1} = G_i + P_i c_i$$

$$where\ G_i = x_i y_i\ and\ P_i = x_i + y_i$$

- G_i is called generate function and P_i is called propagate function
- G_i and P_i are computed only from x_i and y_i and not c_i, thus they can be computed in one gate delay after X and Y are applied to the inputs of an n-bit adder.

$$c_{i+1} = G_i + P_i c_i$$
$$c_i = G_{i-1} + P_{i-1} c_{i-1}$$
$$\Rightarrow c_{i+1} = G_i + P_i(G_{i-1} + P_{i-1} c_{i-1})$$
continuing
$$\Rightarrow c_{i+1} = G_i + P_i(G_{i-1} + P_{i-1}(G_{i-2} + P_{i-2} c_{i-2}))$$
until
$$c_{i+1} = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + .. + P_i P_{i-1} .. P_1 G_0 + P_i P_{i-1} ... P_0 c_0$$

c_{i+1} is given in terms of c_0.

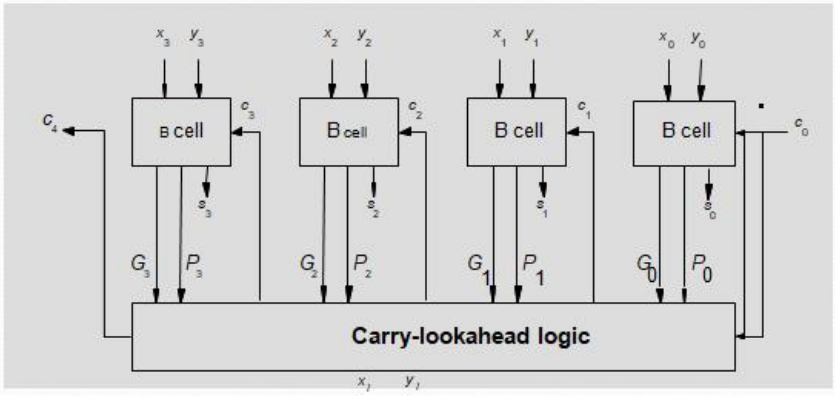
Consider 4-bit CLA:

$c_1 = G_0 + P_0 c_0$

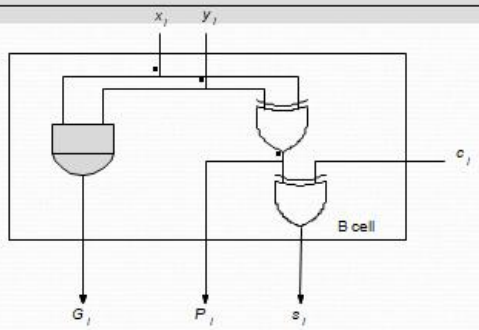
$c_2 = G_1 + P_1 G_0 + P_1 P_0 c_0$

$c_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0$

$c_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0$



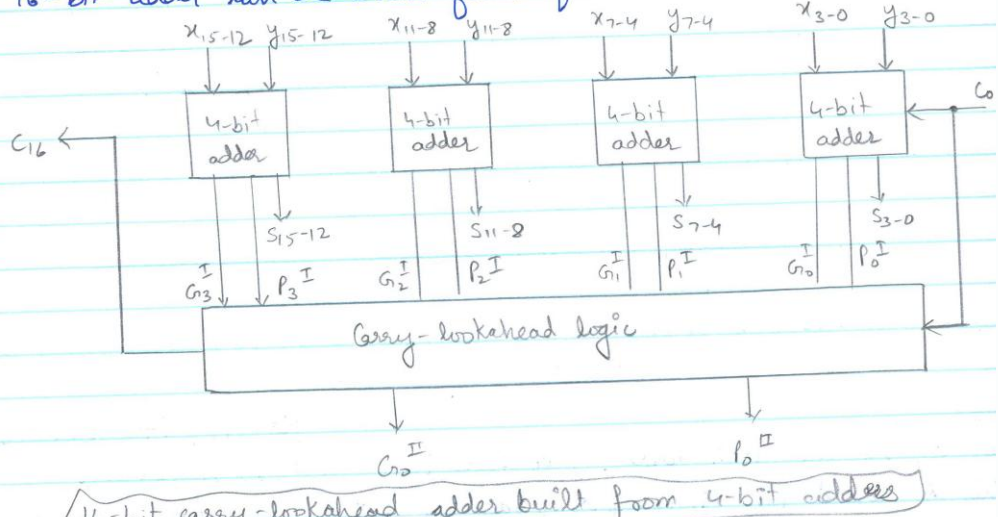
4-bit carry-lookahead adder



B-cell for a single stage

Higher-level Generate and Propagate functions

16-bit adder can be built from four 4-bit adder blocks.



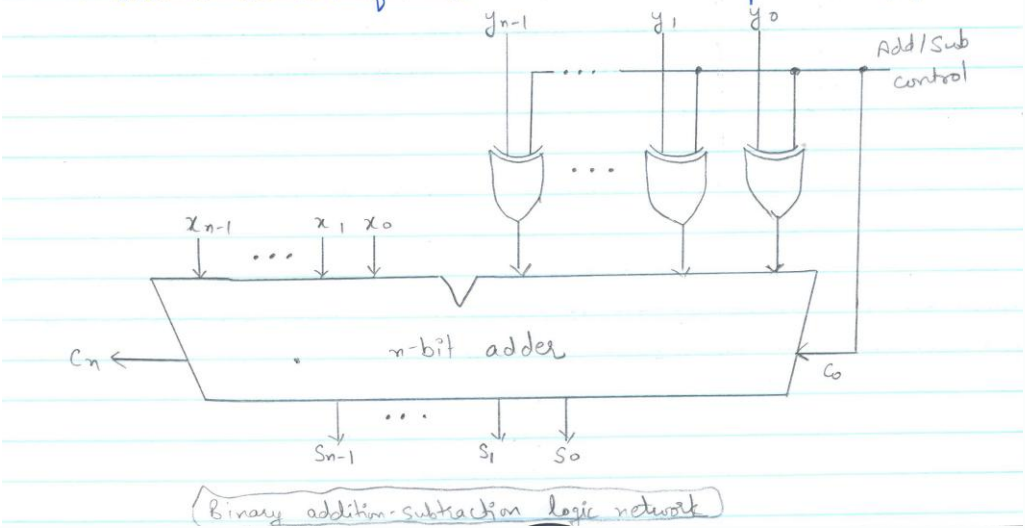
16-bit carry-lookahead adder built from 4-bit adders

These blocks provide new output functions defined as G_K^I and P_K^I, where K=0 for first 4 bit block,

OR

9 (a)	Perform multiplication for +16 and -7 using Booth algorithm Answer= -112	[6]	CO2	L2
(b)	**Define** • **Memory Cycle Time:** It is the minimum time delay that required between the initiation of the two successive memory-operations. • **Memory Access Time:** It is the time that elapses between → initiation of an operation & → completion of that operation. **Fast Page Mode** ➢ Transferring the bytes in sequential order is achieved by applying the consecutive sequence of column-address under the control of successive CAS' signals. ➢ This scheme allows transferring a block of data at a faster rate. ➢ The block of transfer capability is called as *fast page mode*.	[4]	CO2	L2

OR

10 (a)	Draw and explain the addition subtraction logic circuit. Overflow occurs when the carry bits C_n and C_{n-1} are different. Therefore, overflow can be obtained by implementing the expression $C_n \oplus C_{n-1}$ with XOR gate. for subtraction X−Y on 2's-complement numbers X and Y, we form the 2's complement of Y and add it to X. The ~~circuit~~ network for addition/subtraction is shown below. Add/Sub input control line is set to 0 for addition & C_0=0. (applying Y unchanged). This line is set to 1 for subtraction (Y is complemented) and C_0=1.  Binary addition-subtraction logic network	[5]	CO5	L2
(b)	Explain various types of ROM. (PROM-1, EPROM-1, EEPROM-1, Flash memory-2)	[5]	CO2	L2

PROM(Programmable Read Only Memory)

- PROM allows the data to be loaded by the user.
- Programmability is achieved by inserting a 'fuse' at point P in a ROM cell.
- Before PROM is programmed, the memory contains all 0's.
- User can insert 1's at required location by burning-out fuse using high current-pulse.
- This process is irreversible.
- **Advantages:**
  1) It provides flexibility.
  2) It is faster.
  3) It is less expensive because they can be programmed directly by the user.

EPROM (Erasable Reprogrammable Read Only Memory)

- EPROM allows
  → stored data to be erased and
  → new data to be loaded.
- In cell, a connection to ground is always made at 'P' and a special transistor is used.
- The transistor has the ability to function as
  → a normal transistor or
  → a disabled transistor that is always turned 'off'.
- Transistor can be programmed to behave as a permanently open switch, by injecting charge into it.
- Erasure requires dissipating the charges trapped in the transistor of memory-cells.
  This can be done by exposing the chip to ultra-violet light.
- **Advantages:**
  1) It provides flexibility during the development-phase of digital-system.
  2) It is capable of retaining the stored information for a long time.
- **Disadvantages:**
  1) The chip must be physically removed from the circuit for reprogramming.
  2) The entire contents need to be erased by UV light.

A significant disadvantage of EPROMs is that a chip must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultraviolet light. It is possible to implement another version of erasable PROMs that can be both programmed and erased electrically. Such chips, called EEPROMs, do not have to be removed for erasure. Moreover, it is possible to erase the cell contents selectively. The only disadvantage of EEPROMs is that different voltages are needed for erasing, writing, and reading the stored data.

FLASH MEMORY

- Has similar approach to EEPROM.
- Read the contents of a single cell, but need to write the contents of an entire block of cells. Prior to writing, previous contents of the block are erased.
- Flash devices have greater density so have higher capacity and low storage cost per bit.
- Power consumption of flash memory is very low, hence, making it attractive for use in portable equipment that is battery-driven. E.g., MP3 music players, cell phones, digital cameras.
- Single flash chips are not sufficiently large, so larger memory modules are implemented using flash cards and flash drives.

1) Flash Cards

- One way of constructing larger module is to mount flash-chips on a small card.
- Such flash-card have standard interface.
- The card is simply plugged into a conveniently accessible slot.
- Memory-size of the card can be 8, 32 or 64MB.
- Eg: A minute of music can be stored in 1MB of memory. Hence 64MB flash cards can store an hour of music.

2) Flash Drives

- Larger flash memory can be developed by replacing the hard disk-drive.
- The flash drives are designed to fully emulate the hard disk.
- The flash drives are solid state electronic devices that have no movable parts.

Advantages:

1) They have shorter seek & access time which results in faster response.
2) They have low power consumption. .'. they are attractive for battery driven application.
3) They are insensitive to vibration.

Disadvantages:

1) The capacity of flash drive (<1GB) is less than hard disk (>1GB).
2) It leads to higher cost per bit.
3) Flash memory will weaken after it has been written a number of times (typically at least 1 million times).