CMR
INSTITUTE OF
TECHNOLOGY

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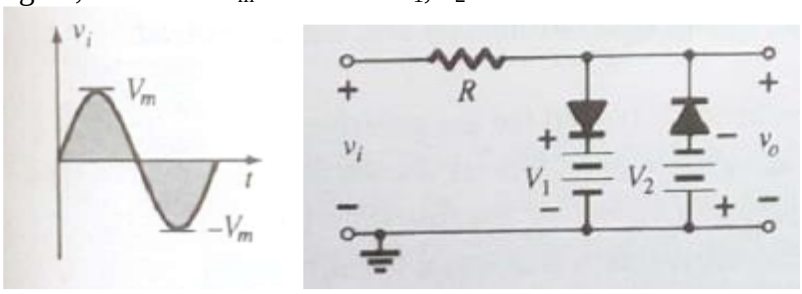
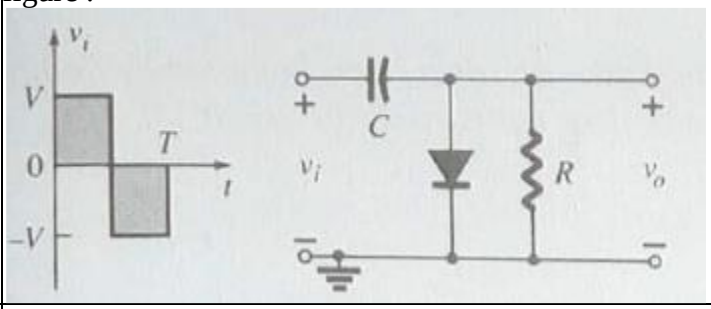
Internal Assesment Test - I

Sub:	ANALOG ELECTRONIC CIRCUITS							Code:	17EE34
Date:	08/09/2018	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	EEE

Answer For FIFTY marks

		Marks	OBE	
			CO	RBT
1a.	Analyse the circuit and draw the pattern of the output(V_o) of the circuit shown in figure, Provided V_m=10V and V_1,V_2=5V. 	5	CO1	L3
1b.	Analyse the circuit and draw the pattern of the output (V_o)of the circuit shown in figure . 	5	CO1	L3
2.	What are the different biasing circuits? Find the expression for stability factor S(I_{CBO}) of each biasing circuit?	10	CO2	L2
3.	Draw the circuit of voltage divider bias circuit. The circuit parameters are, V_{cc} = 10V, R_2 = 17 kΩ, R_1 = 83 kΩ, R_c = 2 kΩ, R_E = 0.5 kΩ, find Q-point and terminal voltages.The transistor has β =100 and V_{BE}=0.7V	10	CO2	L3
4a.	Explain the reasons for instability of Operating point.	5	CO2	L2
4b.	Describe procedure to find the Q-point of a BJT circuit.	5	CO2	L2
5a.	Mention the applications of clippers and clampers.	5	CO1	L1
5b.	Design emitter bias circuit using the following specifications: $I_{c(sat)}$= 10mA, I_{CQ} = 0.5 $I_{c(sat)}$, V_c= 20V, V_{cc}=30V.Assume silicon transistor with β =100	5	CO2	L3
6.	Design a voltage divider bias circuit with V_{cc} = 10V, R_c = 1.5 kΩ, I_c= 2mA,V_{CE}=5V, β =50.Assume silicon transistor and stability factor = 5	10	CO2	L3

******All the Best*****