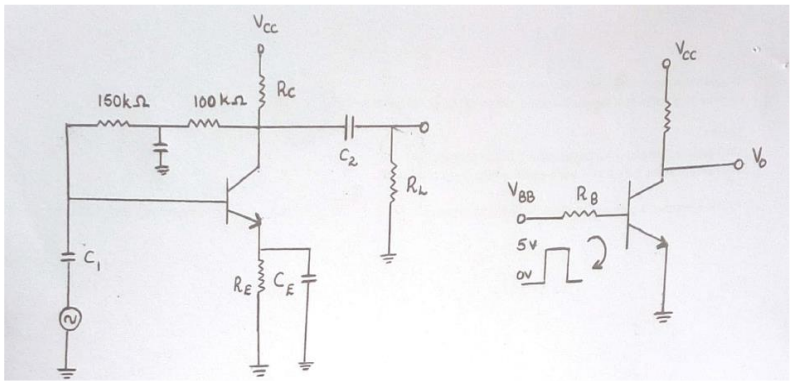
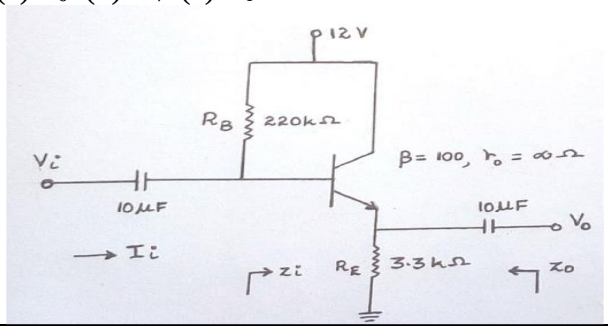
CMR
INSTITUTE OF
TECHNOLOGY

USN | | | | | | | | | | |

Internal Assesment Test - II

Sub:	ANALOG ELECTRONIC CIRCUITS							Code:	17EE34
Date:	16/10/2018	Duration:	90 mins	Max Marks:	50	Sem:	3rd	Branch:	EEE

Answer For FIFTY marks

		Marks	OBE	
			CO	RBT
1a.	Explain the DC analysis of collector feedback bias configuration.	5	CO2	L2
1b.	For Fig(a), find Q-point. Take V_{cc} = 10V, R_c = 1 kΩ, R_E = 0.5 kΩ, β = 50 and V_{BE}=0.7V  Fig(a) Fig(b)	5	CO2	L3
2a.	Explain the operation of transistor as a switch with the help of neat circuit diagram and waveforms.	6	CO3	L2
2b.	For the circuit shown in figure(b) , calculate the value of R_B that saturates the transistor when V_i = 5V, Given that R_c = 1 kΩ, β = 100, V_{cc} = 5V, $V_{CE(SAT)}$ = 0.2V	4	CO3	L3
3a.	For fixed bias circuit, derive expressions for S_{ICO} and S_{VBE} .	4	CO2	L2
3b.	For the voltage divider bias circuit, R_c = 1 kΩ, R_E = 470Ω, R_1 = 10 kΩ, R_2 = 5 kΩ, β = 100. Determine the stability factor S_{ICO} .	6	CO2	L3
4.	Draw the circuit of common emitter amplifier with volatage divider biasing . Derive the expression for current gain, voltage gain, input and output impedance using model.	10	CO2	L2
5.	For the emitter follower network shown below, determine (a) r_e (b) Z_i (c) Z_0 (d) A_v (e) A_i 	10	CO2	L3
6.	Explain hybrid equivalent model for transistor. Develop h-parmeter model for a transistor in CE and CB modes.	10	CO2	L2