CMR INSTITUTE OF TECHNOLOGY

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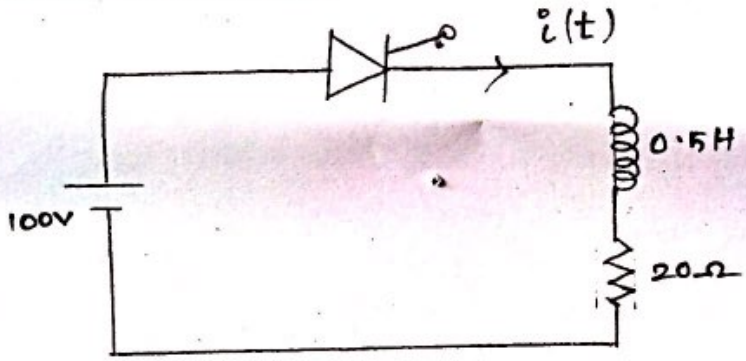
Internal Assesment Test II –Oct 2018

Sub:	POWER ELECTRONICS						Code:	15EE53
Date:	17/10/2018	Duration:	90 mins	Max Marks:	50	Sem: V	Section :	A & B

Note: Answer any **five FULL** Questions

Sketch neat figures wherever necessary. Answer to the point. ***Good luck!***

		Marks	OBE CO	OBE RBT
1 (a)	With necessary waveforms explain the switching characteristics of an IGBT.	[5]	CO2	L2
(b)	Discuss the importance of providing isolation of gate and base drive from power circuit and explain two methods.	[5]	CO2	L1
2 (a)	Explain the anti saturation control of BJT.	[5]	CO2	L2
(b)	The base drive circuit of anti saturation control has supply voltage 500V, collector resistance 5Ω, Vd1 = 3.5V, Vd2 = 0.8V, Vbe (sat) = 0.7V. The voltage to the base circuit is 15V. RB = 1.2Ω and β = 10. Find: i) collector current without clamping ii) collector clamping voltage and iii) collector current with clamping.	[5]	CO2	L1
3 (a)	Explain the V-I characteristics of SCR. Also define : i) Holding current and ii) Latching current	[5]	CO3	L2
(b)	Explain the different methods of triggering thyristor	[5]	CO3	L2
4 (a)	With the help of two transistor model, derive an expression for anode current of a thyristor and explain why gate loses its control over the device once thyristor is turned on	[10]	CO3	L1
5 (a)	For the SCR shown in the figure, has a latching current of 20mA and is fired by a pulse width of 50μs. Determine whether the SCR turn on or not and comment on the result obtained 	[5]	CO2	L2
(b)	Ten thyristors are used in string to withstand a DC voltage of Vs = 18kV. The maximum leakage current and reverse recovery charge differences of thyristors are 12mA and 150μC respectively. Each thyristor has voltage sharing resistance of 60kΩ and capacitance of 0.6μF. Determine: i. The maximum steady state voltage sharing ii. Steady state voltage derating factor iii. The maximum transient voltage sharing iv. The transient voltage derating factor	[5]	CO3	L2
6	With neat circuit diagram and waveform explain the working of UJT triggering of SCR	[10]	CO3	L2

7 (a)	Design the values of di/dt inductor and RC snubber circuit components for an SCR working in a 230V system. Given di/dt rating is 90A/μs and dv/dt rating is 200V/ μs.	[5]	CO3	L2
(b)	A string of SCRs are connected in series to withstand a dc voltage of 15kV. The maximum leakage current and recovery charge difference of thyristor are 10mA and 150μC respectively. If the maximum steady state voltage sharing is 1000V. Calculate i) steady state voltage sharing R for each thyristor ii) transient voltage capacitance. ASSUME DRF = 0·2 for both conds.	[5]	CO3	L2
8	Explain the VI characteristics of DIAC and TRIAC with circuit diagram	[10]	CO3	L2

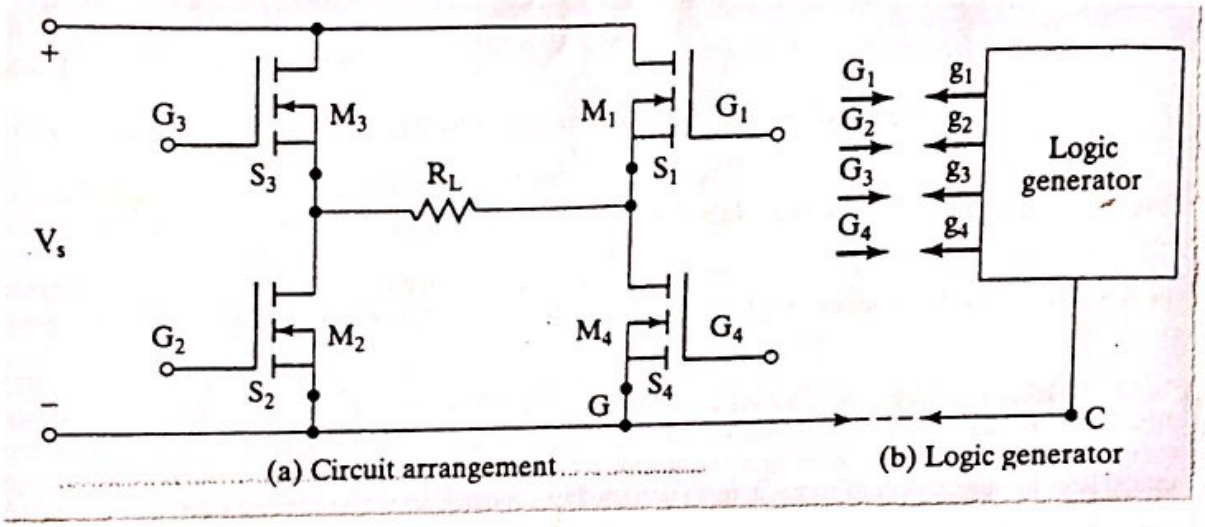
M2

*** ALL THE BEST ***

Isolation of gate and base drives:-

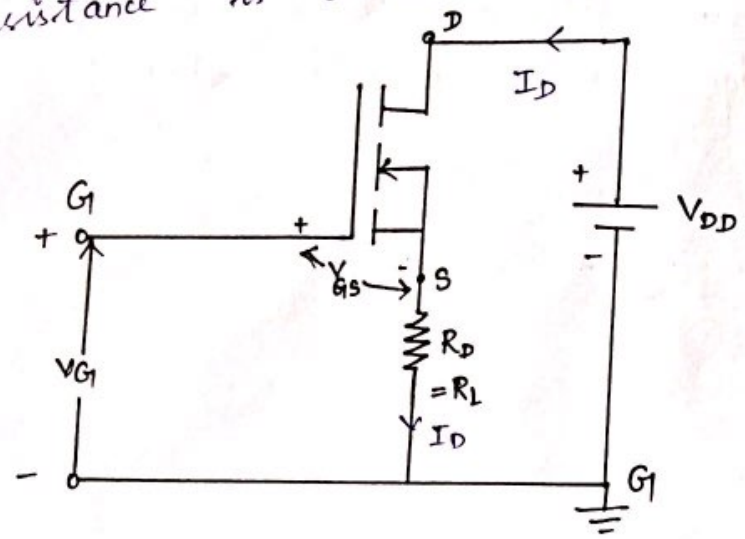
Need for isolation:

To understand why isolation is required b/w the triggering source and control terminals of a semiconductor switch, consider 1ϕ bridge inverter circuit shown below,



* There are four MOSFETS M_1, M_2, M_3 and M_4 and logic circuit which generate four pulses.
* To turn-on M_1, G_1 should be more +ve w.r.t S_1 so that $V_{G1S1} > V_T$ and similarly to turn-on M_3, G_3 should be more +ve w.r.t S_3.
* Therefore it is clear that, each device should have its source terminal as reference and not a common point (ground) as reference.
* So when there is no common datum node for control input of all the semi-conductor devices in a converter, we need to isolate the control signal source from the control terminals.

The importance of gating a transistor b/w its gate and source instead of gate and common ground can be demonstrated using the figure below where load resistance is connected b/w source and ground.



$V_{GS} = V_G$

Applying KVL, $V_G - V_{GS} - I_D R_L = 0$.

$$V_{GS} = V_G - I_D R_L$$

↳ I_D varies with V_{GS} - when transistor turns-on, V_{GS} decreases as and reaches a steady-state value, which is required to balance the load or drain current. ie the value of V_{GS} is unpredictable.

There are basically two ways of floating or isolating the control terminals with respect to ground.

↳ pulse transformer
↳ opto couplers.

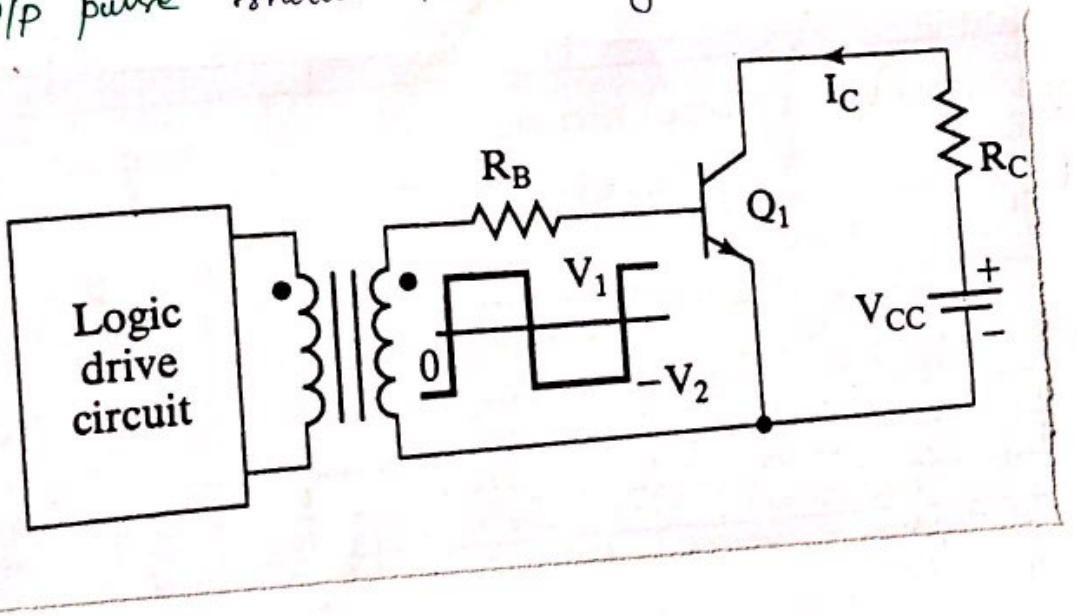
PULSE TRANSFORMERS:-

↳ pulse transformer – 1 primary winding and one or more secondary winding

↳ multiple primary winding allows simultaneous triggering of many switches.

↳ transformer - isolated gate - drive arrangement is shown below

↳ transformer should have a very small leakage inductance and O/P pulse should have very small rise time.



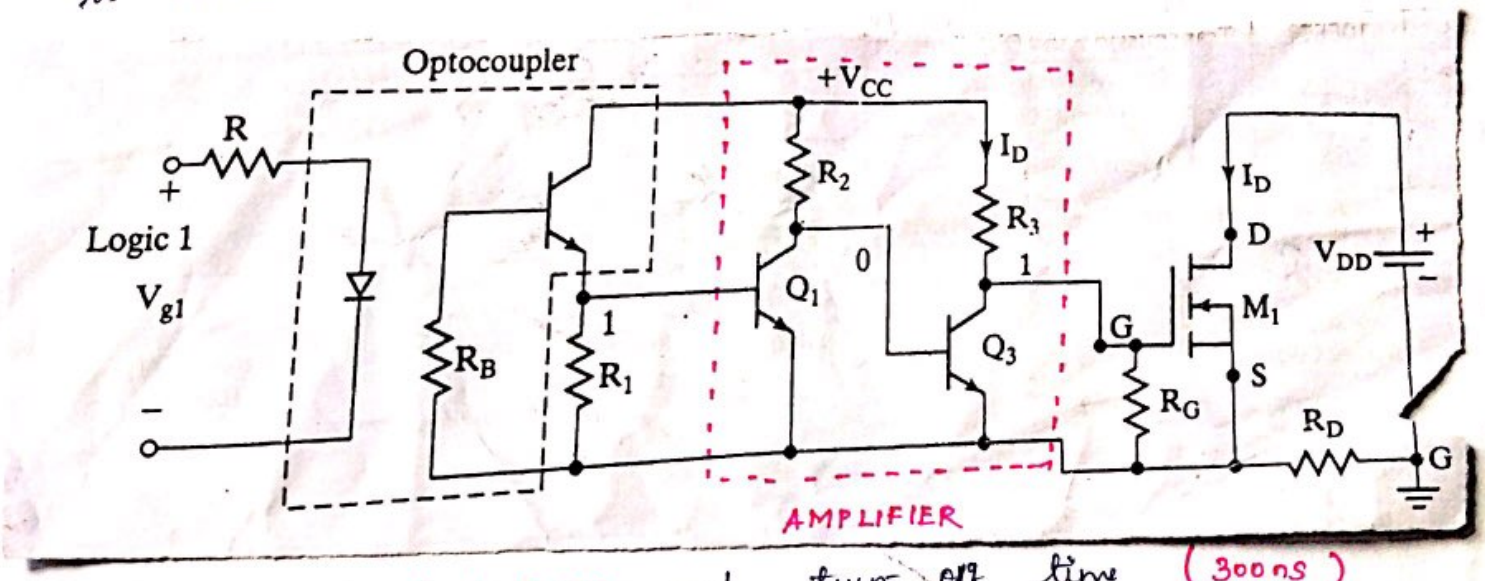
OPTO COUPLERS:

↳ Opto - couplers combine an infrared LED and a silicon photo - transistor

↳ Input is given to ILED and o/p is taken from photo - transistor.

↳ This signal is amplified and then applied to control terminals of the semiconductor device to be controlled.

↳ gate isolation circuit using photo - transistor is shown below,



↳ the time (2 to 5 μs) and turn off time (300 ns) of photo-transistors are very small.

↳ this method of isolation requires additional amplifier in the control circuit.

The turns ratio,

$$\frac{N_2}{N_1} = \frac{I_C}{I_B} = \beta.$$

* The transistor can be turned-off by applying -ve pulse thro RC circuit.
* Additional circuitry is required to discharge C_1 (drawback)

Anti saturation Control :-

Hard saturation :-

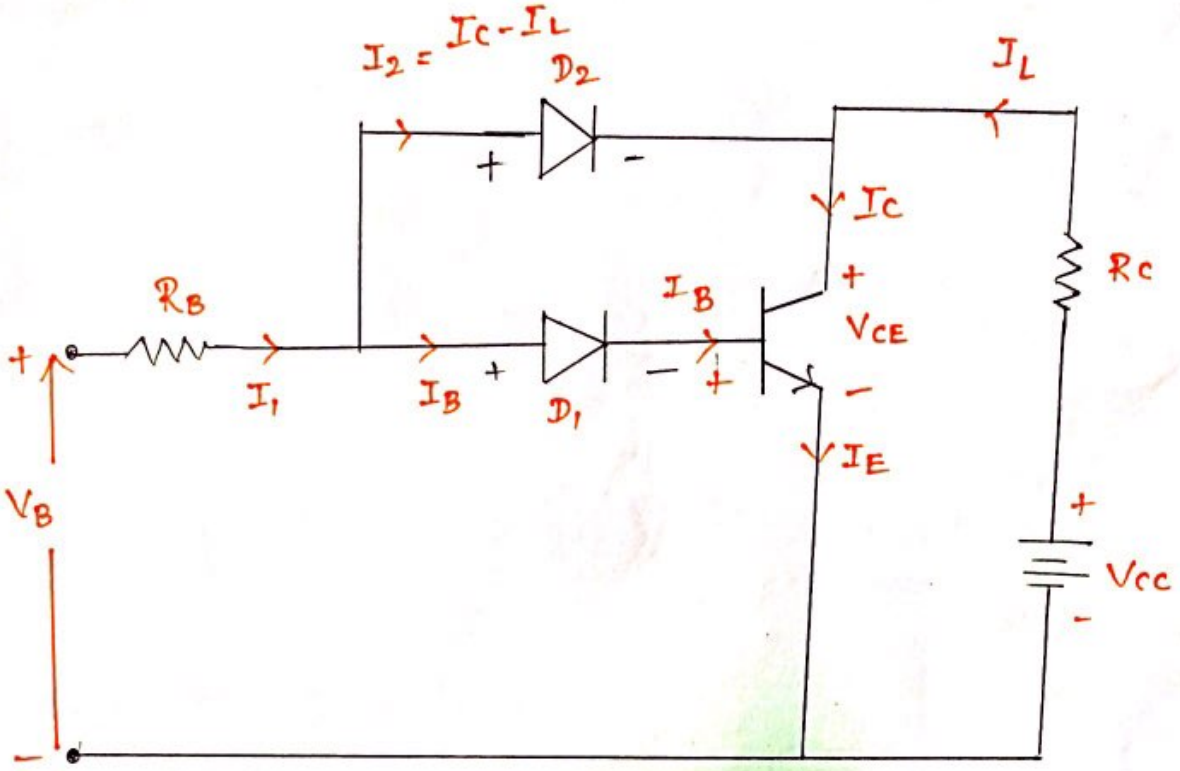
=> When excess base current is given it increases the storage time. which in turn increases the turn-off time i.e reduction in switching speed.

=> Such excess base drive is called **hard saturation**. Therefore transistors must be operated in **quasi saturation** i.e the base current must be given the carriers which are sufficient to drive the transistor in just saturation (quasi saturation)

=> This can be achieved by clamping the collector emitter voltage to a predetermined level.

=> A circuit with such clamping action is known as. **Baker's clamp**

D_2 - anti - saturation diode,



Initially diode D_2 is not forward biased, bcoz transistor is not turned ON,

$\therefore$ The base current without clamping

$$I_1 = I_B \quad (\text{bcoz } I_2 = 0)$$

$$I_B = \frac{V_B - V_{d_1} - V_{BE}}{R_B} \quad \text{— (1)}$$

and corresponding $I_{C_1} = \beta I_B$ — (2).

Once collector current rises, transistor is turned ON and clamping takes place,

$$V_{CE} = V_{BE} + V_{d_1} - V_{d_2} \quad - \quad (3)$$

load current,

$$I_L = \frac{V_{CC} - V_{CE}}{R_C} \quad - \quad (4)$$

(3) in (4),

$$I_L = \frac{V_{CC} - V_{BE} - V_{d_1} + V_{d_2}}{R_C}$$

and corresponding $I_C = \beta I_B$

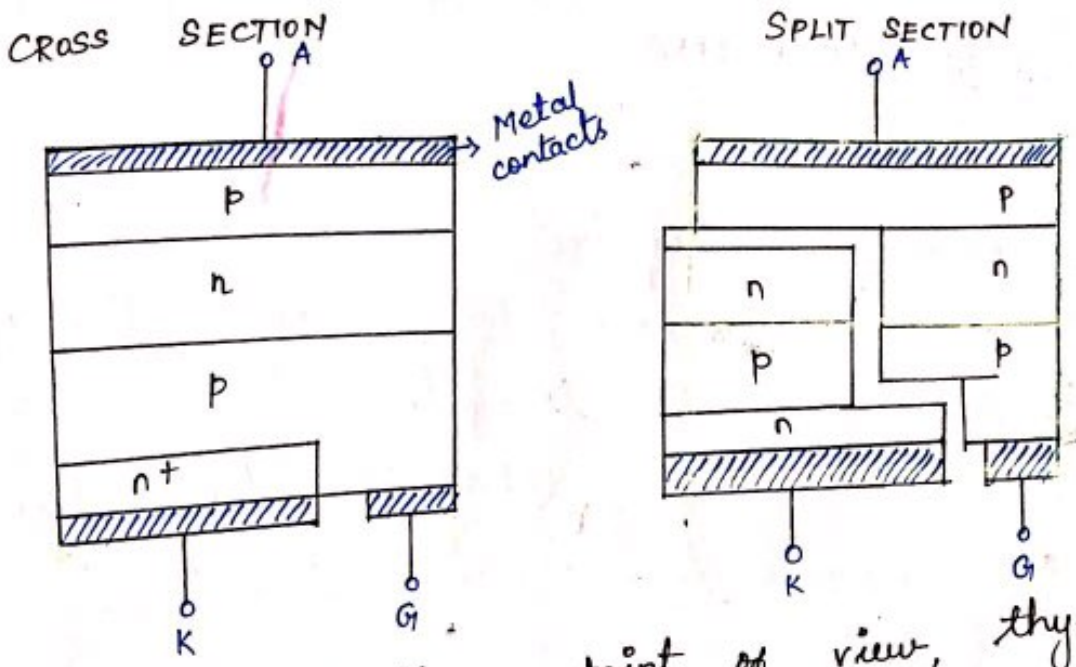
$$= \beta (I_1 - I_2)$$

$$I_C = \beta (I_1 - I_C + I_L)$$

$$I_C = \beta I_1 - \beta I_C + \beta I_L$$

$$I_C + \beta I_C = \beta (I_1 + I_L)$$

$$I_C = \left(\frac{\beta}{1+\beta}\right) I_1 + I_L$$

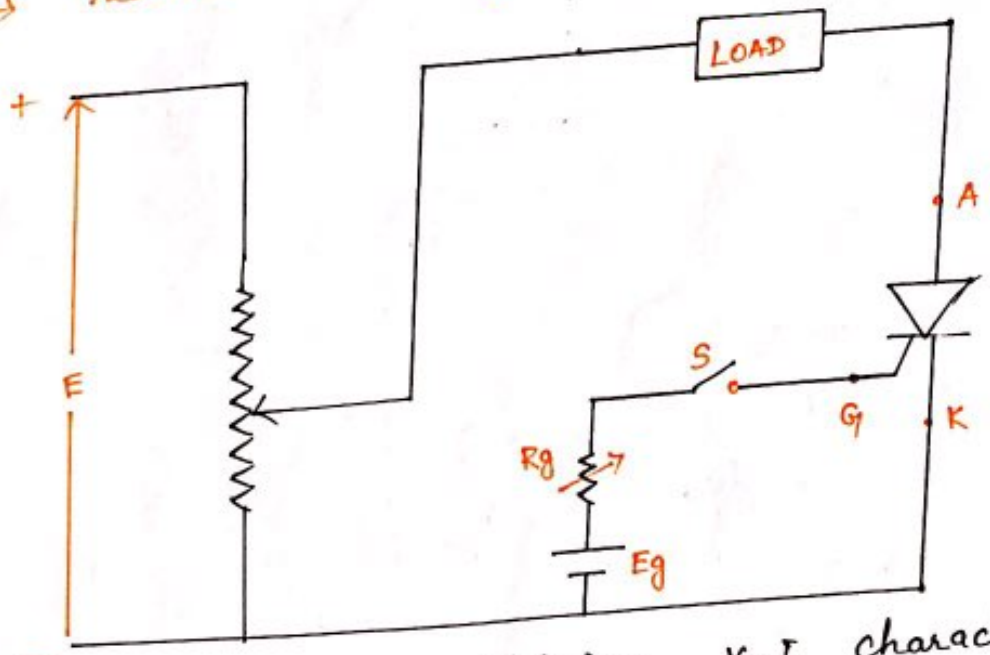


↳ From construction point of view, thyristors can be best viewed as two transistors (npn - pnp) connected together

THYRISTOR CHARACTERISTICS:-

Thyristor has 3 modes of operation

↳ forward blocking mode
↳ forward conduction mode
↳ reverse blocking mode

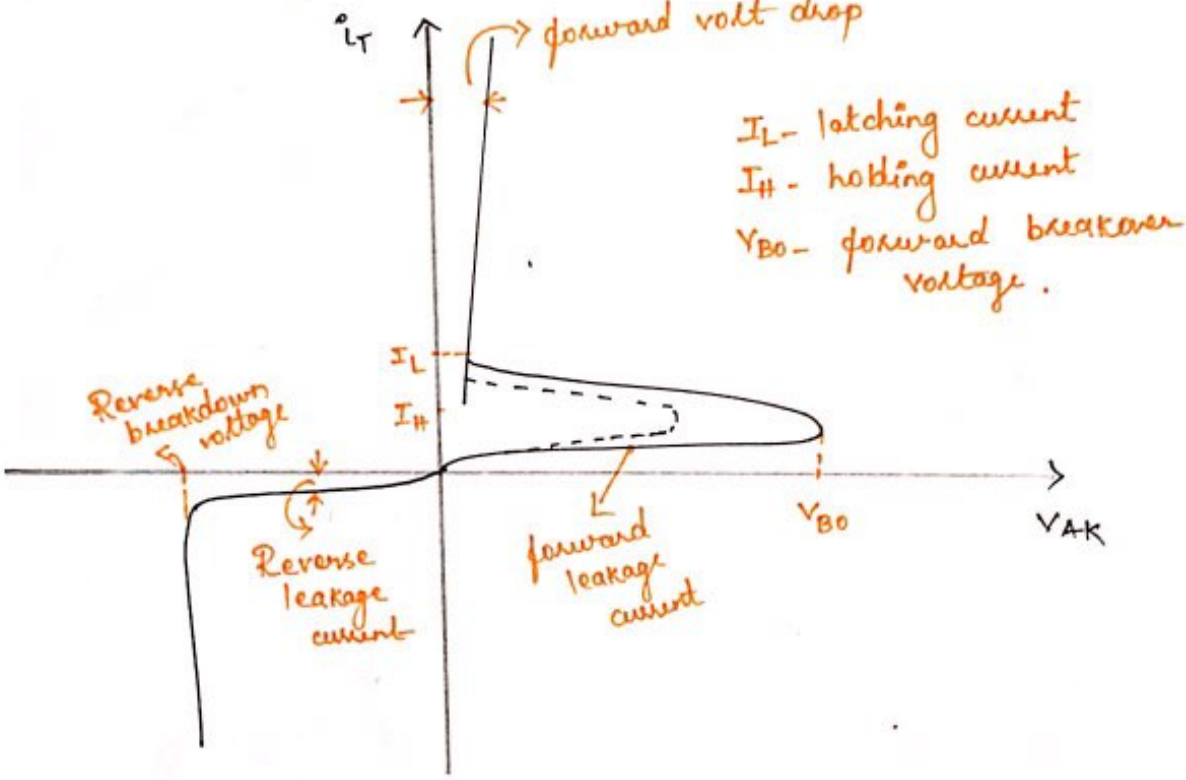


The basic circuit for obtaining V-I characteristics of a thyristor is shown above.

1. Forward Blocking Mode:-

↳ When A is made +ve w.r.t K, the junctions J_1 and J_3 are forward biased. - junction J_2 is reverse biased

↳ thyristor is in OFF state and the leakage current is known as off-state current I_D.



I_L - latching current
I_H - holding current
V_{BO} - forward breakover voltage.

2. Forward Conduction Mode:-

↳ If the anode to cathode voltage V_{AK} is increased to a sufficiently large value called forward breakdown voltage V_{BO}, the reverse biased jxn J_2 breaks down (avalanche breakdown occurs).

↳ Since all other two jxns (J_1 and J_3) are already forward biased, there is free movement of carriers across all 3 jxns, resulting in large forward anode current.

↳ the device is said to be in conducting or on-state.

↳ during on state, the anode current is limited by load resistance.

↳ the anode current must be more than a value known as latching current I_L to maintain the device in ON state, otherwise the device reverts to blocking state if V_{AK} is reduced.

LATCHING CURRENT I_L :-

→ minimum anode current required to maintain the thyristor in ON state, immediately after a thyristor has been turned on and the gate signal has been removed.

↳ Once the thyristor is completely turned on, gate loses the control i.e the device continues to conduct irrespective of gate signal.

↳ However if anode current is reduced below holding current I_H (depletion region develops around J_2 due to reduced no of carriers), thyristor goes back to blocking state

Holding current is the order of mA and is should be always less than latching current.

i.e $I_H < I_L$

HOLDING CURRENT I_H :-

→ minimum anode current to maintain thyristor in on state below which the device goes to off state

Reverse Blocking Mode:-

↳ When cathode is made +ve w.r.t anode, the jcns J_1 and J_3 are reverse biased and J_2 is forward biased.

↳ Similar to two diodes connected in series with reverse voltage applied across them.

↳ Reverse leakage current I_R flows thro the thyristor and device is in blocking state.

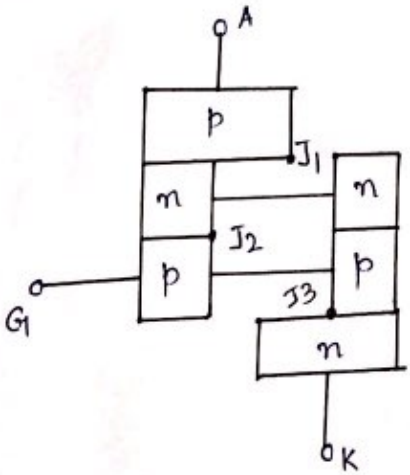
Requirement of gate voltage:-

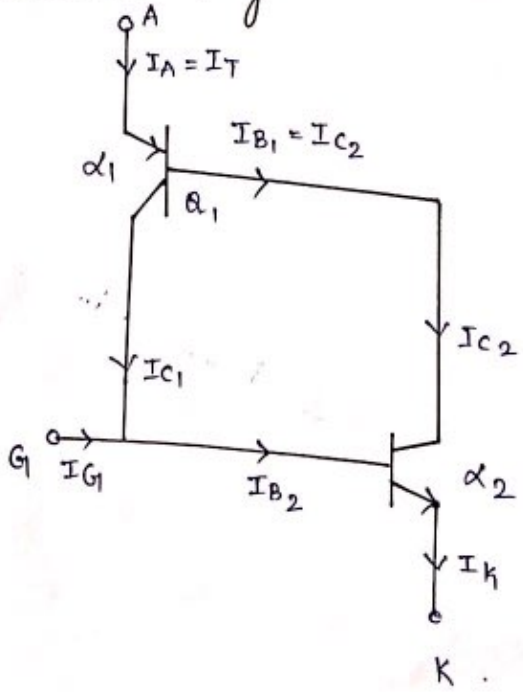
* The thyristor can be turned on by increasing V_{AK} beyond V_{BO}, but that could be destructive.

Usually, thyristor is turned ON by applying +ve voltage b/w gate and cathode (keeping V_{AK} below V_{BO}).

Two Transistor Model of Thyristor.

* A thyristor can be considered as two complementary transistors (PNP and NPN) connected together.





THYRISTOR TURN-ON METHODS

* A thyristor is turned on by increasing the anode current which can be accomplished in one of the following methods.

1. Thermal or temperature triggering
2. Light triggering
3. High voltage or forward voltage triggering.
4. dv/dt triggering
5. Gate triggering.

Thermal Triggering :-

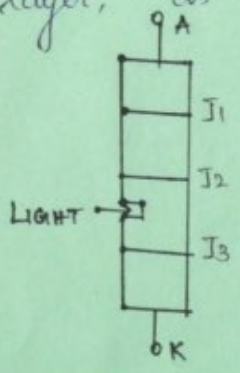
When the device is in forward blocking mode, most of the applied voltage appears across reverse biased junction J_2 - this voltage along with leakage current will increase the temperature. This results in increase in electron-hole pairs, which increases the leakage current. As a result α_1 and α_2 increases - due to regenerative action $\alpha_1+\alpha_2$ approaches unity and the device may be turned on.

This type of turn on may cause thermal run-away and is hence normally avoided.

Light Triggering :

If light is allowed to strike junctions of thyristor, electron-hole pair is and the device may be turned on.

For light triggered SCRs a recess is made in the inner p layer, as shown below,



When the intensity of this light thrown, exceeds certain value, forward biased SCR is turned on. Such a thyristor is known as LASCR (Light Activated SCR).

Forward / High Voltage Triggering :.

If the forward anode to cathode V_{AK} voltage is greater than forward breakdown voltage V_{BO}, sufficient leakage current flows to initiate regenerative turn-on. This type of turned-on is destructive and should be avoided.

dv/dt triggering :-

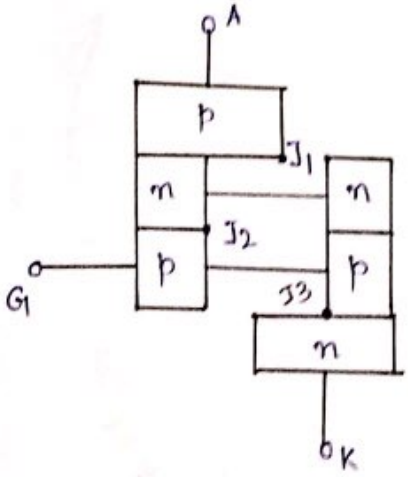
With high rate of rise of the anode to cathode voltage is high, the charging current of the junction capacitances are sufficient enough to turn-on the thyristors. High value of charging current may damage the device, therefore device must be protected against high dv/dt.

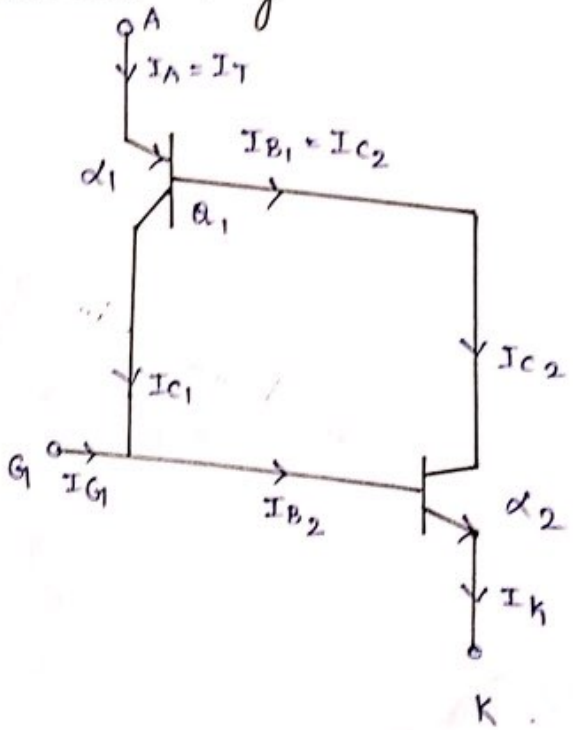
Gate (current) triggering :-

When the thyristor is forward biased, the injection of gate current by applying +ve gate voltage b/w the gate and cathode terminals turns on the thyristor.

TWO TRANSISTOR MODEL OF THYRISTOR.

* A thyristor can be considered as two complementary transistors (PNP and NPN) connected together.





In general, for a $I_C = \beta I_B + I_{CBO}$ (5)

$$I_C = \alpha I_E + I_{CBO} \quad \text{.... (1)}$$

where I_C - collector current

I_E - emitter current

I_{CBO} - leakage current of CB junction

Current gain, $\alpha \simeq \frac{I_C}{I_E}$.

Consider transistor Q_1, $I_C = I_{C1}$, $I_E = I_A$, $I_{CBO} = I_{CBO_1}$

$\alpha = \alpha_1$

$$I_{C_1} = \alpha_1 I_A + I_{CBO_1} \quad \text{.... (2)}$$

similarly for transistor Q_2,

$I_C = I_{C_2}$, $I_E = I_K$, $I_{CBO} = I_{CBO_2}$

$$I_{C_2} = \alpha_2 I_K + I_{CBO_2} \quad \text{.... (3)}$$

Referring to the figure,

$$I_A = I_{C_1} + I_{C_2} \quad \text{.... (4)}$$

$$= \alpha_1 I_A + \alpha_2 I_K + I_{CBO_1} + I_{CBO_2} \quad \text{.... (5)}$$

Also, $I_K = I_A + I_{G_1}$, ... (6)

(6) in (5) and simplifying,

$$I_A = \alpha_1 I_A + \alpha_2 \left[I_A + I_{G_1} \right] + I_{CBO_1} + I_{CBO_2}$$

$$= \alpha_1 I_A + \alpha_2 I_A + \alpha_2 I_{G_1} + I_{CBO_1} + I_{CBO_2}$$

$$I_A - I_A(\alpha_1 + \alpha_2) = \alpha_2 I_{G_1} + I_{CBO_1} + I_{CBO_2}$$

$$I_A \left(1 - (\alpha_1 + \alpha_2)\right) = \alpha_2 I_{G_1} + I_{CBO_1} + I_{CBO_2}$$

$$\boxed{I_A = \frac{\alpha_2 I_{G_1} + I_{CBO_1} + I_{CBO_2}}{1 - (\alpha_1 + \alpha_2)}} \quad \text{.... (7)}$$

* The importance of gate current can be understood from eqn (7).

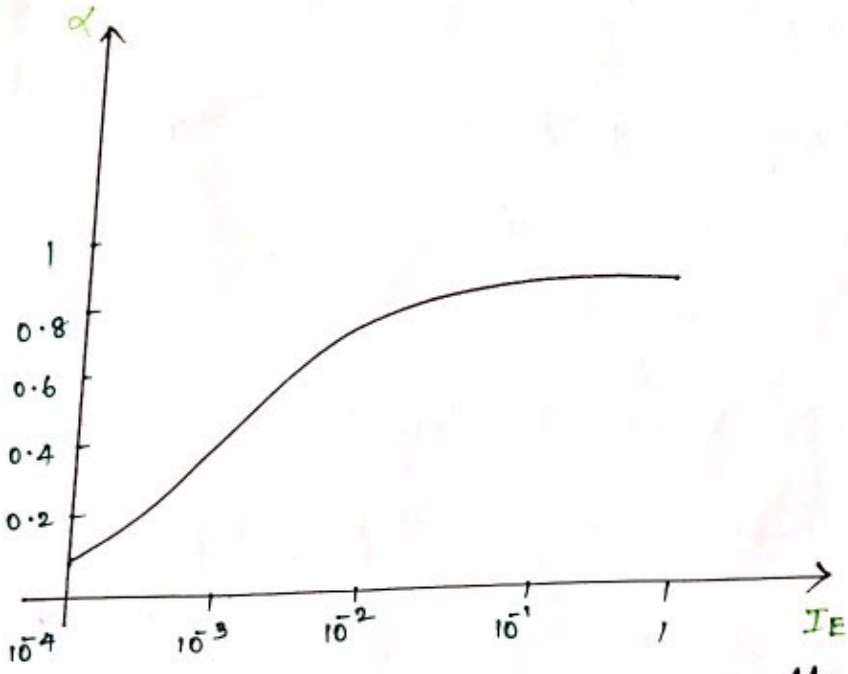
W.K.T α_1 depends on α_A varies with I_A b'coz $\alpha_1 \simeq \frac{I_{C1}}{I_A}$ ($\alpha_1 \simeq \frac{I_{A1}-I_{C2}}{I_A}$) and α_2 varies with I_K ($I_A + I_G$).

Say if I_G is increased suddenly, (say from 0 to 1mA) I_A will increase, which would further increase α_1 and α_2. This increase in α_1 and α_2 further increases I_A.

↳ Therefore, there is a regenerative (+ve feedback) effect. when $\alpha_1+\alpha_2$ tends to be unity, the denominator eqn (6) approaches zero, resulting in large value of I_A

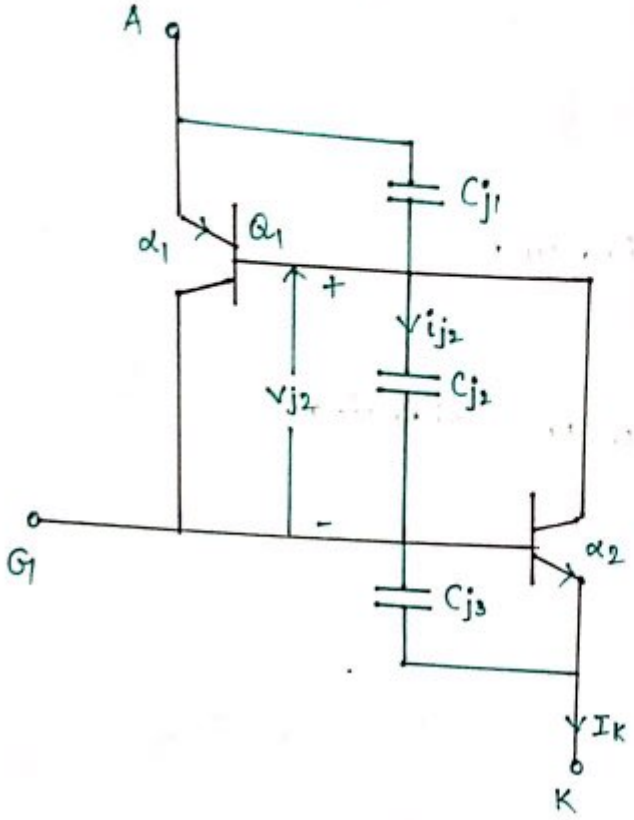
i.e thyristor turns on with a small gate current.

The variation of current gain with emitter current is shown below.



-X- i.e the method of turning on a thyristor is making $\alpha_1+\alpha_2$ to approach unity.

The characteristics of thyristors are greatly influenced by junction capacitance



* When the thyristor is in forward blocking state, a rapidly rising voltage across the device would cause high current flow through the junction capacitors.

Let i_{j2} be the current thro C_{j2}.

$$i_{j2} = \frac{d(q_{j2})}{dt}$$

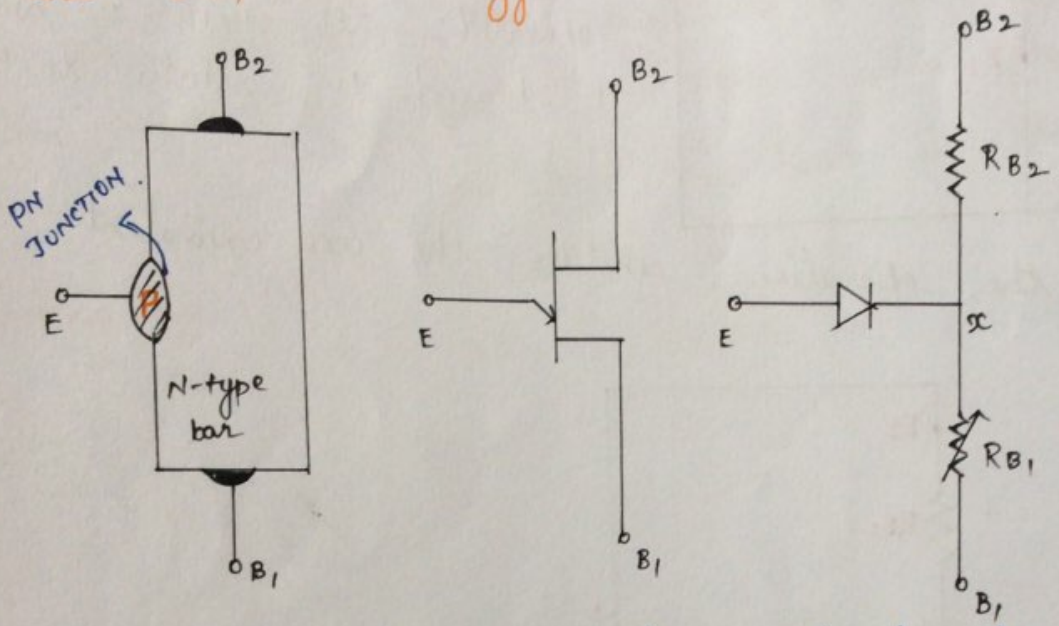
$$= \frac{d(C_{j2} V_{j2})}{dt}$$

$$= V_{j2} \frac{dC_{j2}}{dt} + C_{j2} \frac{dV_{j2}}{dt} \Rightarrow C_{j2} \frac{dV_{j2}}{dt}$$ (since C_{j2} is almost const)

* This current will increase the emitter current of both Q_1 and Q_2 and as a result $\alpha_1 + \alpha_2$ approaches unity and result in undesirable turn-on of the thyristor.

Unijunction Transistor (UJT)

↳ three terminal, single junction - operated as a switch finds its application in oscillators, timing circuits and SCR / TRIAC trigger circuits.



↳ Lightly doped N-type bar and heavily doped P region which forms the emitter terminal

↳ R_{BB} - resistance of N-type bar (4KΩ and 10KΩ) exist b/w B_1 and B_2

R_{BB} is broken up into two resistances,

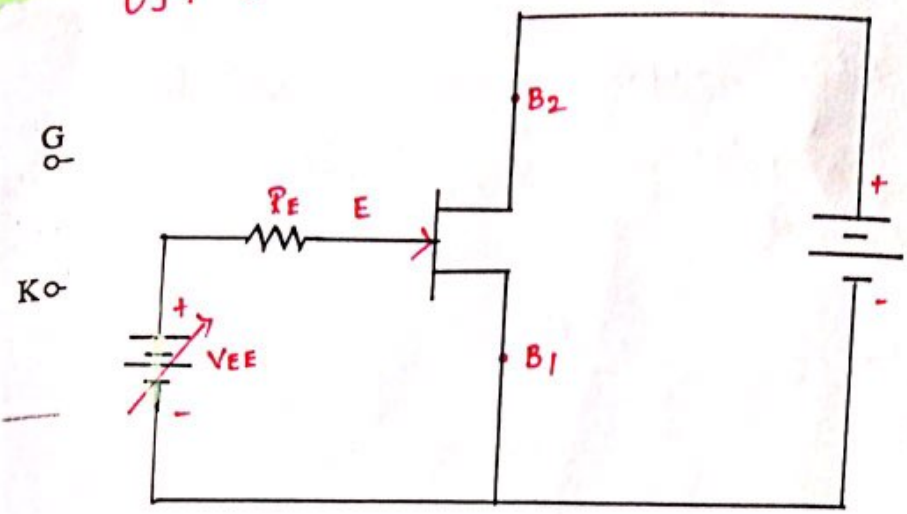
R_{B1} - resistance from B_1 to emitter (4KΩ down to 10Ω)

R_{B2} - " from B_2 to "

* When emitter diode is reverse biased, a very small emitter current flows i.e R_{B1} is high ≃ 4KΩ and device is in OFF state

* When emitter diode is forward biased, R_{B1} is low allowing emitter current to flow readily and device is in ON state.

UJT BIASING:

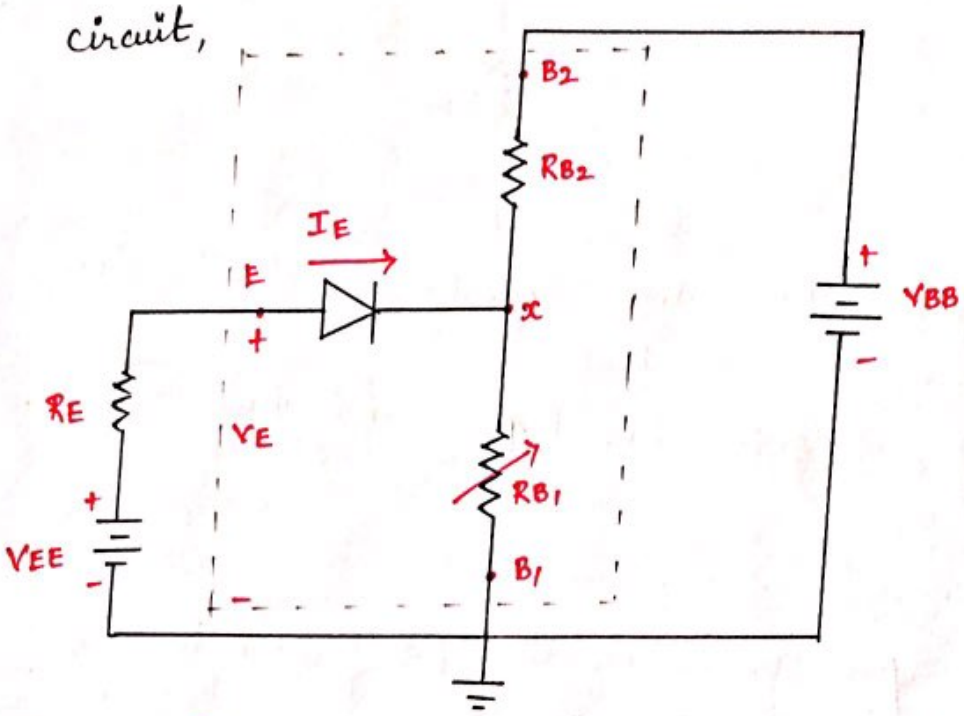


V_{BB} - constant source.

V_{EE} - variable source (usually voltage across capacitor)

* UJT is normally operated with both B_2 and E biased +ve relative to B_1

To understand the operation, consider the UJT equivalent circuit,



OFF STATE:-

Neglecting emitter, R_{B_1} and R_{B_2} forms voltage divider circuit,

$$\text{i.e } V_x = \frac{R_{B_1} V_{BB}}{R_{B_1} + R_{B_2}} \Rightarrow \frac{R_{B_1}}{R_{BB}} V_{BB}$$

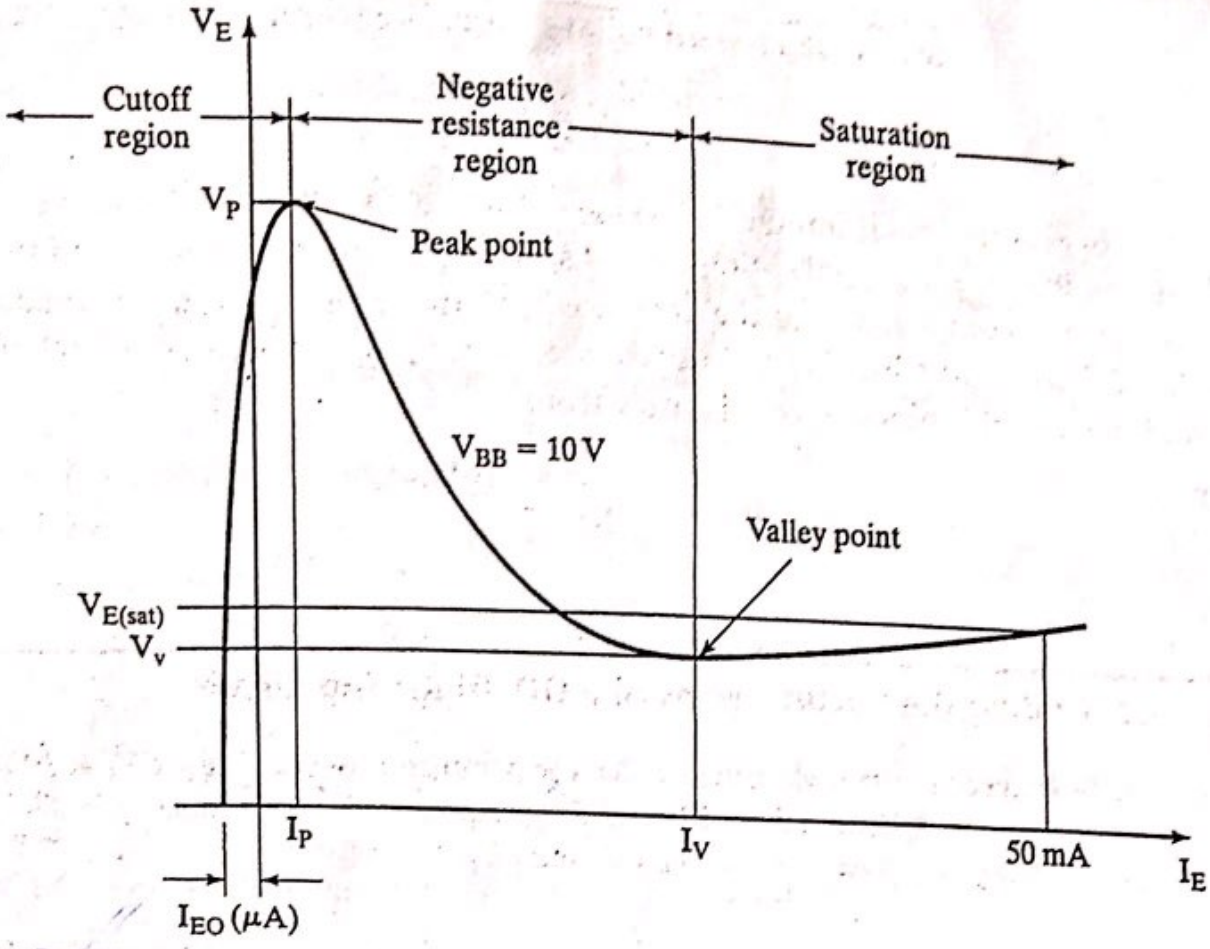
$$V_x = \eta V_{BB}$$

where η - intrinsic stand off ratio

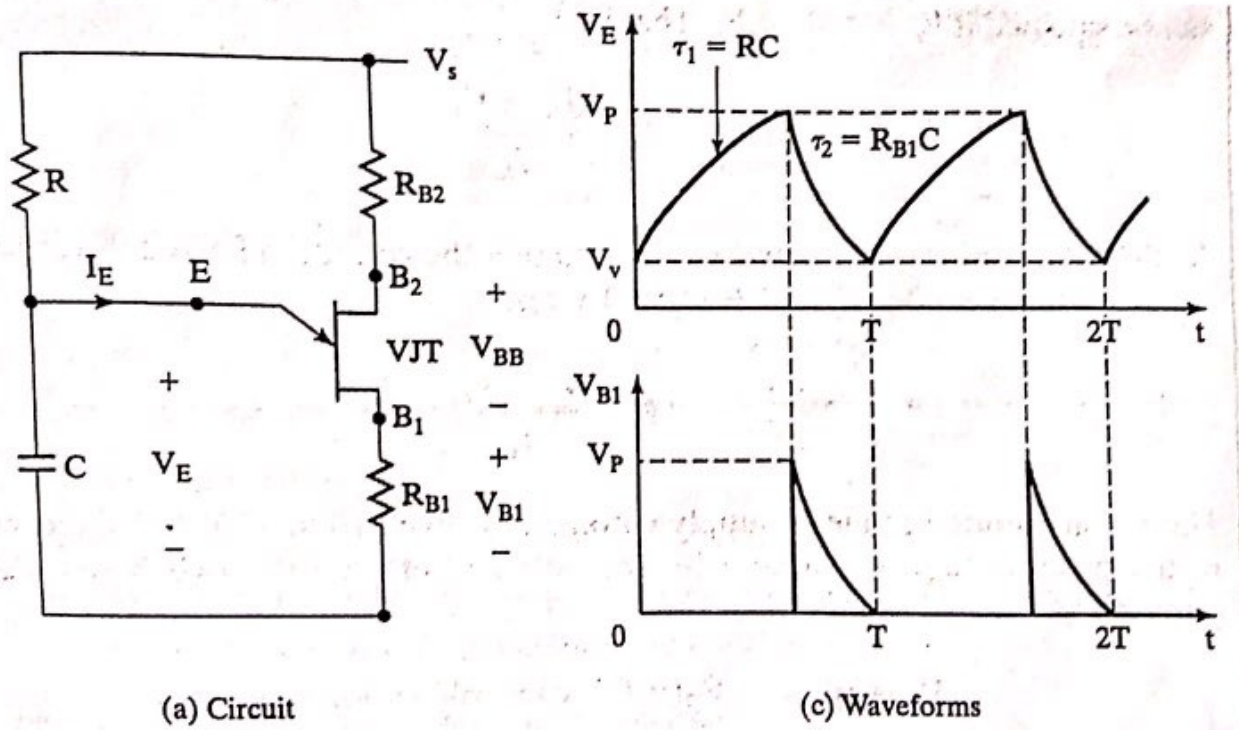
$$\eta = \frac{R_{B_1}}{R_{BB}}$$

η = varies b/w (0.5 to 0.8)

The static characteristics of UJT are shown below (21)



> UJT is generally used as an oscillator.



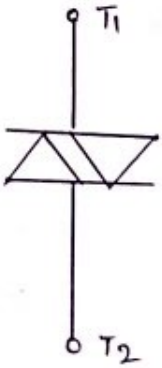
(a) Circuit

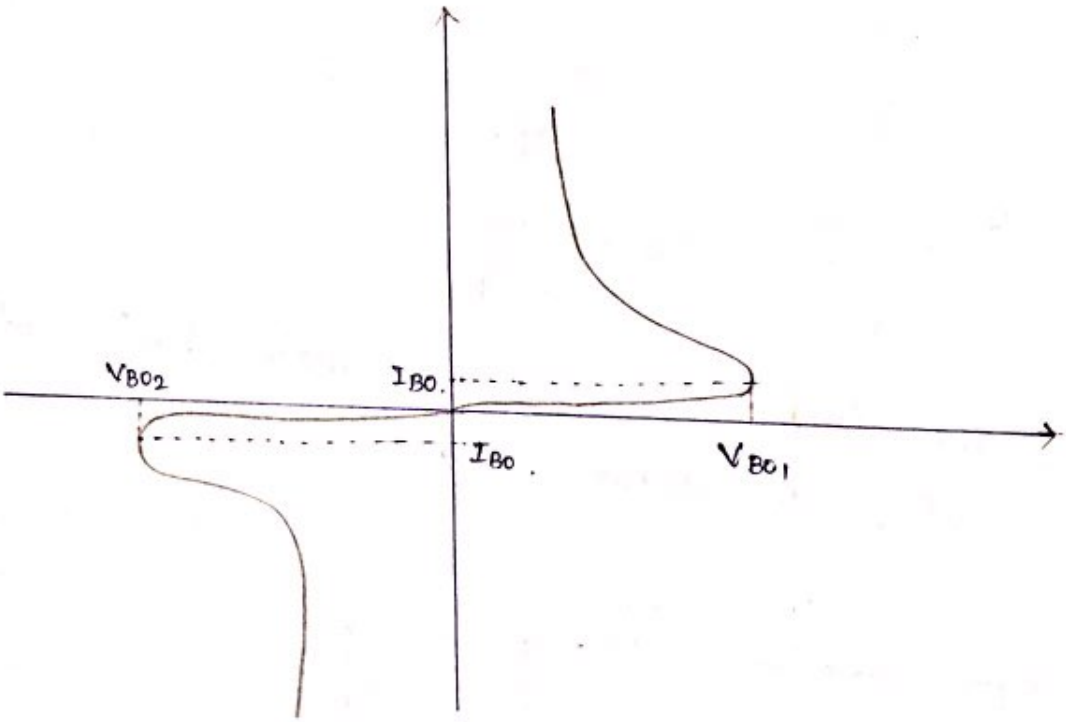
(c) Waveforms

DIAC (Bi- directional Diode)

* A DIAC is a two electrode, bi- directional avalanche diode which can be switched from OFF state to ON state for either polarity of applied voltage.

* DIAC - diode that can work on ac





* The device conducts in both the directions i.e when T_1 is +ve w.r.t to T_2 or T_2 is +ve w.r.t T_1 the device conducts once the voltage crosses breakover voltages.

2 b) $V_{CC} = 500V$. $R_C = 5\Omega$, $V_{d1} = 3.5V$, $V_{d2} = 0.8V$.

$V_{BE(sat)} = 0.7V$ $V_B = 15V$. $R_B = 1.2\Omega$, $\beta = 10$.

i) Collector current without clamping :-

$$I_C = \beta I_B$$

$$I_B = \frac{V_B - V_{BE} - V_{d1}}{R_B} \Rightarrow I_1$$

$$= \frac{15 - 0.7 - 3.5}{1.2} \Rightarrow 9A.$$

$$I_C = 10 \times 9 \Rightarrow 90A. \quad \boxed{I_C = 90A}$$

ii) collector clamping voltage :-

$$V_{CE} = V_{BE} + V_{d1} - V_{d2}$$

$$= 0.7 + 3.5 - 0.8 \Rightarrow 3.4V.$$

$$\boxed{V_{CE} = 3.4V}$$

iii) collector current with clamping,

$$I_C = \left(\frac{\beta}{1+\beta}\right)(I_1 + I_L) \quad ; \quad I_1 = I_B \Rightarrow 9A.$$

$$I_L = \frac{V_{CC} - V_{CE}}{R_C} \Rightarrow \frac{500 - 3.4}{5} \Rightarrow 99.32A.$$

$$I_C = \frac{10}{11}(9 + 99.32) \Rightarrow 98.47A.$$

5 a) $I_L = 20mA$, $t_{on} = 50\mu s$.

$$i(t) = \frac{V_S}{R}\left(1 - e^{-t/\tau}\right)$$

$$= \frac{100}{20}\left[1 - e^{-\left((50\times10^{-6})\times\frac{20}{0.5}\right)}\right]$$

$i(t) = 10mA$.

SCR is not turned on since $i(t) < I_L$.

5 b) $n_S = 10$; $E_S = V_S = 18kV$, $I_{bmax} = \Delta I_b \Rightarrow 12\times10^{-3}A$.

$\Delta Q_{max} = 150\times10^{-6}C$. $R = 60K\Omega$, $C = 0.6\times10^{-6}F$.

i) Max steady state voltage sharing $= E_{D(SS)}$

$$E_{D(SS)} = \frac{(n_S-1)RI_{bmax} + E_S}{n_S}$$

$$= \frac{(9)(60\times10^{3})\times(12\times10^{-3}) + (18\times10^{3})}{10}$$

$$= 2118$$

$$\boxed{E_{D\,SS} = 2.5kV.}$$

ii) $DRF = 1 - \frac{E_S}{n_S E_{DSS}} = 1 - \frac{(18\times10^{3})}{10\times(2.5\times10^{3})}$

$= 0.28$ (28%)

iii) Max transient voltage sharing :-

$$E_{D(trans)} = \frac{\Delta Q_{max}(n_S-1)}{C} + E_S \Rightarrow \frac{\left(\frac{150\times10^{-6}\times9}{0.6\times10^{-6}}\right) + (18\times10^{3})}{10}$$

$$E_{D(trans)} = .2025 \Rightarrow 2.02kV.$$

iv) $DRF = 1 - \frac{E_S}{n_S E_{D(trans)}} = 1 - \frac{18\times10^{3}}{10\times2.02\times10^{3}} \Rightarrow 0.1089$

10.89%.

7 a) $V_S = 230V$, $\frac{di}{dt}$ rating $= 90 A/\mu s$.

$\frac{dv}{dt}$ " $= 200 V/\mu s$

i) $L_S = V_S / \frac{di}{dt} \Rightarrow 230 \times / 90 \times 10^{-6}$.

$L_S = 2.55 \mu H$.

ii) $\frac{dv}{dt} = \frac{0.632 V_S}{R_S C_S}$.

$R_S = \frac{dv/dt}{di/dt} = \frac{200}{90} \Rightarrow 2.22 \Omega$.

$C_S = \frac{0.632 V_S}{R_S \, dv/dt} \Rightarrow \frac{0.632 \times 230}{2.22 \times 200 \times 10^{+6}} \Rightarrow 327 nF$.

b) $E_S = 15 kV$. $I_{b\,max} = 10 \times 10^{-3} A$; $\Delta Q_{max} = 180 \times 10^{-6} C$

$E_{DSS} = 1000$.

i) $DRF = 1 - \frac{E_S}{n_S E_{DSS}}$.

$\frac{E_S}{n_S E_{DSS}} = 1 - DRF$.

$n_S = \frac{E_S}{E_{DSS}(1 - DRF)} \Rightarrow \frac{15 \times 10^3}{10 \times 10^3 (1 - 0.2)}$.

$= 18.75$

$n_S = 19$.

$$R = \frac{E_{D\,SS}\,n_3 - E_S}{(n_3 - 1)\, I\, b_{max}} \Rightarrow$$

$$= \frac{(1000 \times 19) - (15 \times 1000)}{18 \times 10 \times 10^{-3}} \Rightarrow 22.22\,K\Omega$$

$$C = \frac{\Delta Q_{max}\,(n_3 - 1)}{E_D n_3 - E_S} \Rightarrow \frac{150 \times 10^{-6} \times 18}{(1000 \times 19) - (15 \times 1000)}$$

$$C = 675\,nF$$