CMR
INSTITUTE OF
TECHNOLOGY

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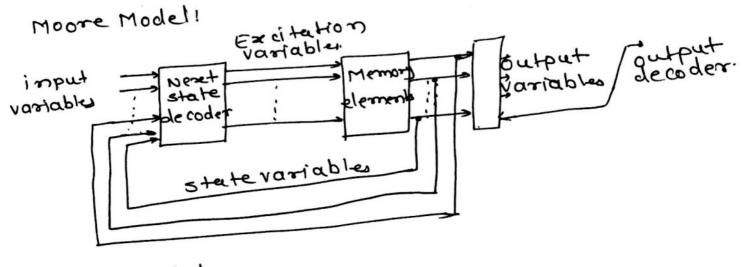


Internal Assesment Test - III

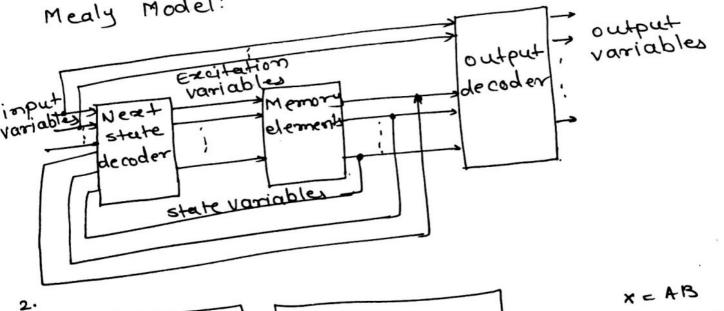
	Internal Assesment Test - III	1		
Sub:	DIGITAL SYSTEM DESIGN	Code:	17EE35	
Date:	22/11/2018 Duration: 90 mins Max Marks: 50 Sem: 3rd (A)	Branch:	Е	EE
	Answer any FIFTY marks.		1	
l		Marks OBE		
<u> </u>		10	CO	RBT
	Define state variables, excitation variables and write a note on Moore and Mealy sequential model.	10	CO4	L1
	Give output function, transition table and state diagram by analyzing the sequential circuit shown above.	10	CO4	L3
3.	Realize a 3 bit synchronous up counter using JK flip flop. Write excitation table, transition table and logic diagram.	10	CO4	L4
	Design the sequential logic circuit for system shown above using D flip flop.	10	CO4	L3
	For the logic diagram given in fig.) Derive the excitation and output equations ii) write the next equation iii) construct a transition table iv) draw the state diagram.	10	CO4	L4
6.	Design a sequence detector to detect sequence 110 using JK flip flop.(Use Moore Machine model)	10	CO4	L3

State variable: The output of Hipflops (memory) defines the state of a sequential machine. Therefore steete variables are the flip-flop outputs.

Excitation variable: Excitation variables are the imputs to the flip-flops. Excitation variables are generated by the input combinational logic operation on the state variables and input variables.



Mealy Model:



B

XEAB SALA RALA SB - AB RB - AB

