Internal Assessment Test I Solutions – Sep 2018

Sub: DSP Algorithms and architecture Subject code: 15EC751

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1 (a) An analog signal is sampled at the rate of 8khz. If 512 samples of this signal are used to compute DFT X(k). Calculate the analog and digital frequency spacing between adjacent X(k) elements. Also, calculate analog and digital frequencies corresponding to k=64

Sol:

$$\text{Frequency Spacing } \Delta f = \frac{F_s}{N} = \frac{8khz}{512} = 15.625 \quad [2M]$$

$$\text{Analog Frequency Corresponding to} k = 64 \text{ is } \Delta f \times k = 15.625 * 64 = 1000HZ \ [2M]$$

1 (b) With a neat diagram explain the scheme of a DSP system

Sol:

DSP is a technique of performing the mathematical operations on the signals in digital domain. As real time signals are analog in nature we need first convert the analog signal to digital, then we have to process the signal in digital domain and again converting back to analog domain. Thus ADC is required at the input side whereas a DAC is required at the output end. A typical DSP system is as shown in figure 1.1

Fig 1.1: A Typical DSP System

A computer or a processor is used for digital signal processing. Antialiasing filter is a LPF which passes signal with frequency less than or equal to half the sampling frequency in order to avoid Aliasing effect. Similarly at the other end, reconstruction filter is used to reconstruct the samples from the staircase output of the DAC (Figure 1.2). [3 M]

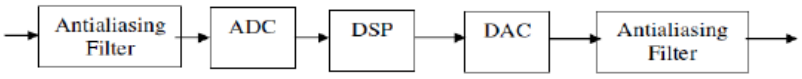


Fig 1.2 The Block Diagram of a DSP System

Signals that occur in a typical DSP are as shown in figure 1.3.

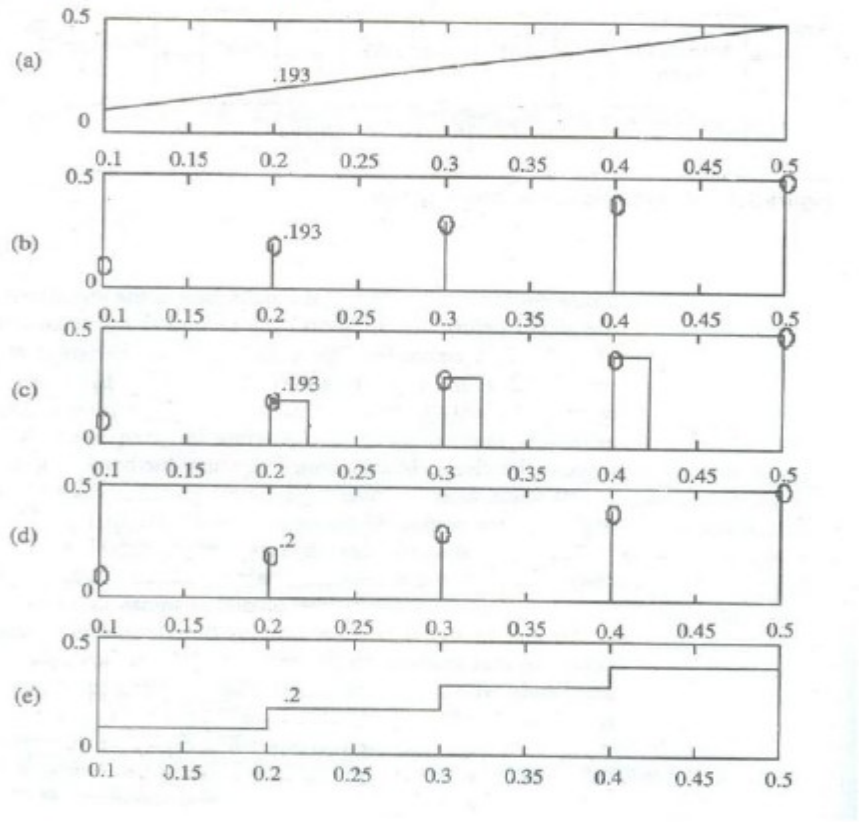


Fig 1.3: (a) Continuous time signal (b) Sampled Signal (c) Sampled Data Signal (d) Quantized Signal (e) DAC Output

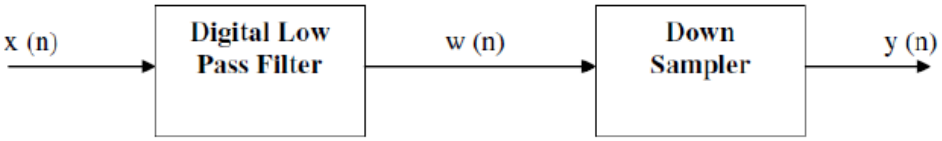
2 (a) Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagrams.

Sol:

Decimation is a process of dropping the samples without violating sampling theorem. The factor by which the signal is decimated is called as decimation factor and it is denoted by M. It is given by,

$$y(m) = w(mM) = \sum_{k=-\infty}^{\infty} b_k x(mM - k)$$

where $w(n) = \sum_{k=-\infty}^{\infty} b_k x(n-k)$ [2 M]



[1M]

Interpolation is a process of increasing the sampling rate by inserting new samples in between. The input output relation for the interpolation, where the sampling rate is increased by a factor L, is given as, $y(m) = \sum_{k=-\infty}^{\infty} b_k w(m-k)$ where $w(n) = \begin{cases} x\left(\frac{m}{L}\right), m = 0, \pm 1L, \pm 2L, \pm 3L \ldots\ldots \\ 0, otherwise \end{cases}$ [2M]

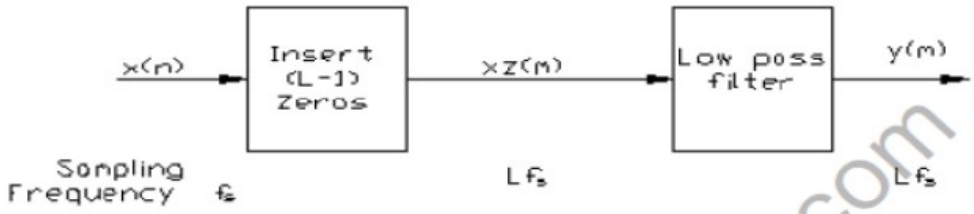
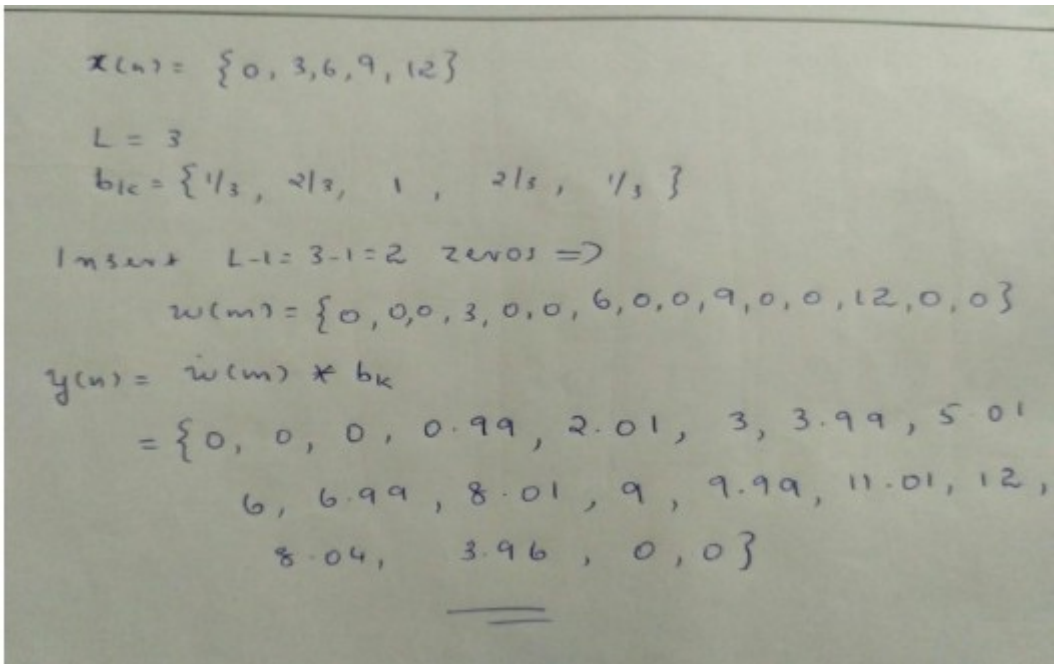


Fig 1.13 Interpolation Process

2 (b) Let $x(n)$=[0,3,6,9,12] be interpolated with L=3. If the filter coefficients of the filters are $b_k=[1/3,2/3,1,2/3,1/3]$, Determine the interpolated sequence.

Sol:



3 For the FIR filter $y(n)=0.5x(n)+0.5x(n-1)$ Determine i) System Function ii) Magnitude response iii) phase response iv) impulse response v) group Delay

Sol:

(i) $\cos(\Theta/2)e^{-j\Theta/2}$

(ii) $\cos(\Theta/2)$

(iii) $(\Theta/2)$

(iv) [0.5, 0.5]

(v) -1/2

4 Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier

Sol:

The advent of single chip multipliers paved the way for implementing DSP functions on a VLSI chip. Parallel multipliers replaced the traditional shift and add multipliers now a days. Parallel multipliers take a single processor cycle to fetch and execute the instruction and to store the result. They are also called as Array multipliers.

The key features to be considered for a multiplier are:

a. Accuracy

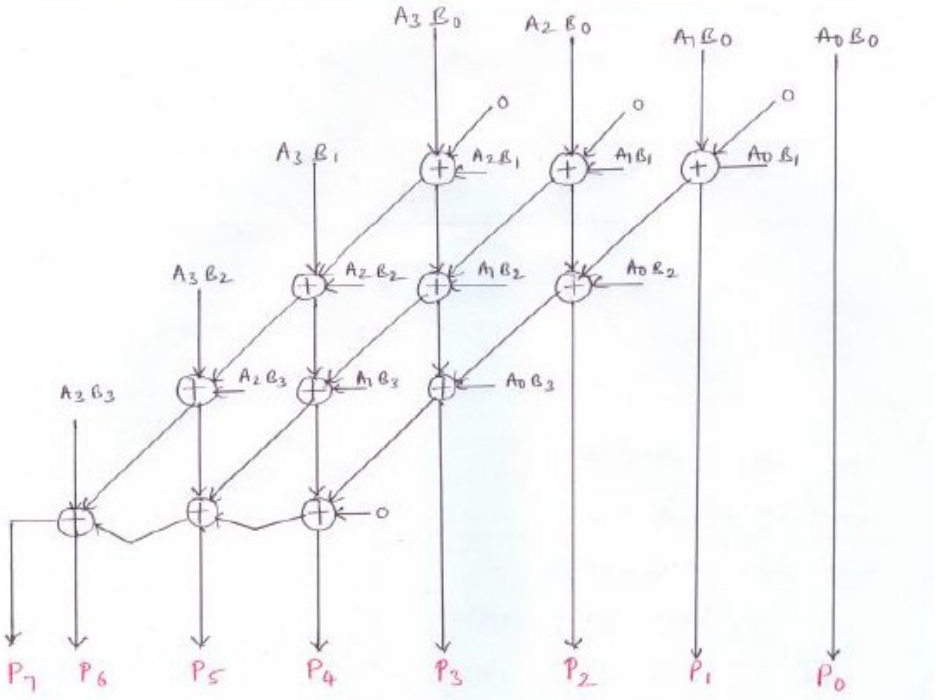
b. Dynamic range

c. Speed

The number of bits used to represent the operands decide the accuracy and the dynamic range of the multiplier. Whereas speed is decided by the architecture employed. If the multipliers are implemented using hardware, the speed of execution will be very high but the circuit complexity will also increases considerably. Thus there should be a tradeoff between the speed of execution and the circuit complexity. Hence the choice of the architecture normally depends on the application.

						A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0
				A_3B_0	A_2B_0	A_1B_0	A_0B_0
			A_3B_1	A_2B_1	A_1B_1	A_0B_1	
		A_3B_2	A_2B_2	A_1B_2	A_0B_2		
	A_3B_3	A_2B_3	A_1B_3	A_0B_3			
P7	P6	P5	P4	P3	P2	P1	P0

This operation can be implemented paralleling using Braun multiplier whose hardware structure is as shown in the figure



Multipliers for Signed Numbers

In the Braun multiplier the sign of the numbers are not considered into account. In order to implement a multiplier for signed numbers, additional hardware is required to modify the Braun multiplier. The modified multiplier is called as Baugh-Wooley multiplier.

Consider two signed numbers A and B,

$$A = -A_{m-1}2^{m-1} + \sum_{i=0}^{m-2} A_i 2^i$$

$$B = -B_{n-1}2^{n-1} + \sum_{j=0}^{n-2} B_j 2^j$$ [2M]

Product $P = P_{m+n-1} \ldots\ldots P_1 P_0$

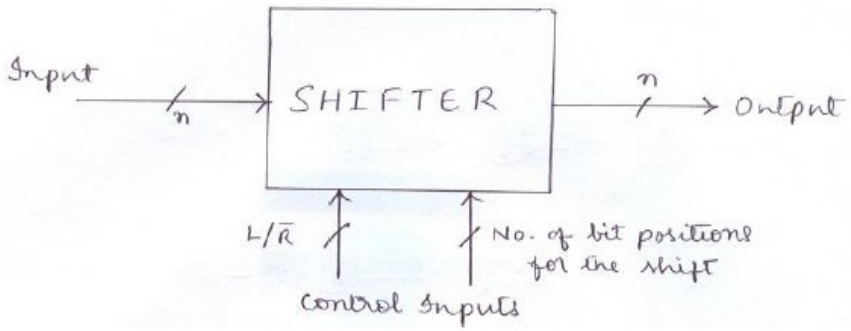
$$P = A_{m-1}B_{n-1}2^{m+n-2} + \sum_{i=0}^{m-2}\sum_{j=0}^{n-2} A_iB_j2^{i+j} - \sum_{i=0}^{m-2} A_iB_{n-1}2^{n-1+i} - \sum_{j=0}^{n-2} A_{m-1}B_j2^{m-1+j}$$

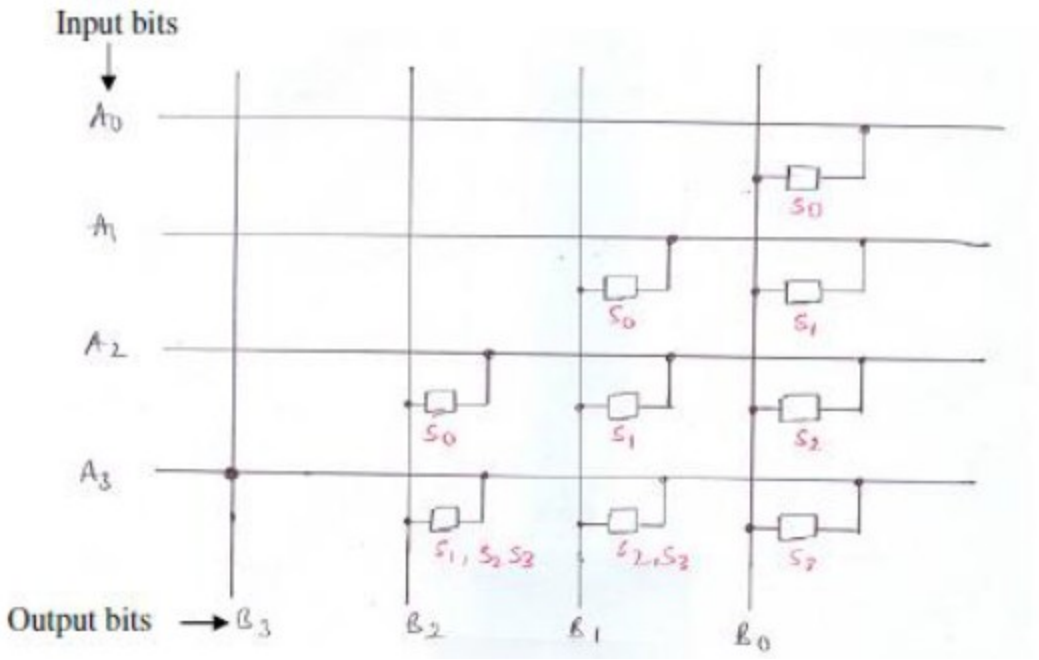
Speed: Conventional Shift and Add technique of multiplication requires n cycles to perform the multiplication of two n bit numbers. Whereas in parallel multipliers the time required will be the longest path delay in the combinational circuit used. As DSP applications generally require very high speed, it is desirable to have multipliers operating at the highest possible speed by having parallel implementation.

5 (a) What is the role of a shifter in DSP? Explain the implementation of 4-bit, shift- right barrel shifter, with a diagram

Sol:

In conventional microprocessors, normal shift registers are used for shift operation. As it requires one clock cycle for each shift, it is not desirable for DSP applications, which generally involves more shifts. In other words, for DSP applications as speed is the crucial issue, several shifts are to be accomplished in a single execution cycle. This can be accomplished using a barrel shifter, which connects the input lines representing a word to a group of output lines with the required shifts determined by its control inputs. For an input of length n, $\log_2 n$ control lines are required. And an additional control line is required to indicate the direction of the shift. The block diagram of a typical barrel shifter is as shown in figure [3M]





INPUT				SHIFT (SWITCH)	OUTPUT (B_3 B_2 B_1 B_0)			
A_3	A_2	A_1	A_0	0 (S_0)	A_3	A_2	A_1	A_0
A_3	A_2	A_1	A_0	1 (S_1)	A_3	A_3	A_2	A_1
A_3	A_2	A_1	A_0	2 (S_2)	A_3	A_3	A_3	A_2
A_3	A_2	A_1	A_0	3 (S_3)	A_3	A_3	A_3	A_3

Fig 2.4 Implementation of a 4 bit Shift Right Barrel Shifter

Figure 2.4 depicts the implementation of a 4 bit shift right barrel shifter. Shift to right by 0, 1, 2 or 3 bit positions can be controlled by setting the control inputs appropriately.

5 (b) Draw the schematic diagram of the saturation logic and explain the same

Sol:

Overflow/ underflow will occur if the result goes beyond the most positive number or below the least negative number the accumulator can handle. Thus the overflow/underflow error can be resolved by loading the accumulator with the most positive number which it can handle at the time of overflow and the least negative number that it can handle at the time of underflow. This method is called as saturation logic. A schematic diagram of saturation logic is as shown in figure 2.7. In saturation logic, as soon as an overflow or underflow condition is satisfied the accumulator will be loaded with the most positive or least negative number overriding the result computed by the MAC unit.[2M]

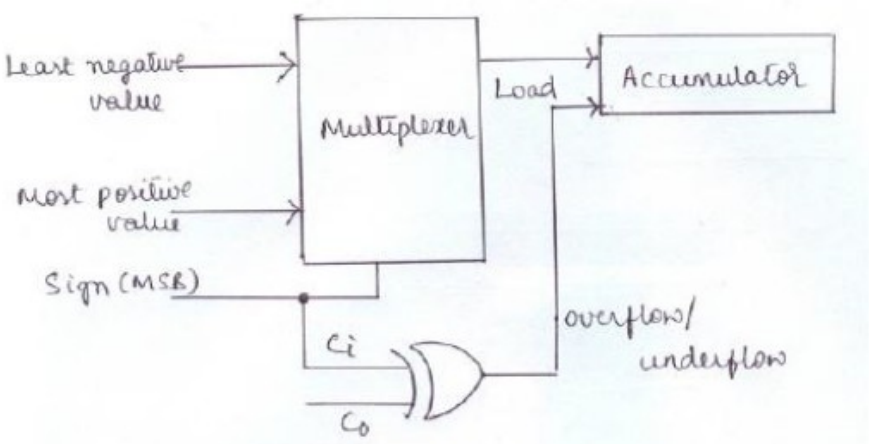


Fig 2.7 A Schematic Diagram of the Saturation Logic

6 (a) Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP

Sol:

While processing the data samples coming continuously in a sequential manner, circular buffers are used. In a circular buffer the data samples are stored sequentially from the initial location till the buffer gets filled up. Once the buffer gets filled up, the next data samples will get stored once again from the initial location. This process can go forever as long as the data samples are processed in a rate faster than the incoming data rate.

Circular Addressing mode requires three registers viz

a. Pointer register to hold the current location (PNTR)
b. Start Address Register to hold the starting address of the buffer (SAR)
c. End Address Register to hold the ending address of the buffer (EAR)

There are four special cases in this addressing mode. They are

a. SAR < EAR & updated PNTR > EAR
b. SAR < EAR & updated PNTR < SAR
c. SAR >EAR & updated PNTR > SAR
d. SAR > EAR & updated PNTR < EAR

The buffer length in the first two case will be (EAR-SAR+1) whereas for the next tow cases (SAR-EAR+1)

The pointer updating algorithm for the circular addressing mode is as shown below.

```
; Pointer Updating Algorithm

Updated PNTR ◄—— PNTR ± increment

If SAR < EAR
        And if Updated PNTR > EAR then
                New PNTR ◄—— Updated PNTR – Buffer size
        And if Updated PNTR < SAR then
                New PNTR        Updated PNTR + Buffer size
```

[2M]

If SAR > EAR

And if Updated PNTR > SAR then

New PNTR ← Updated PNTR – Buffer size

And if Updated PNTR < EAR then

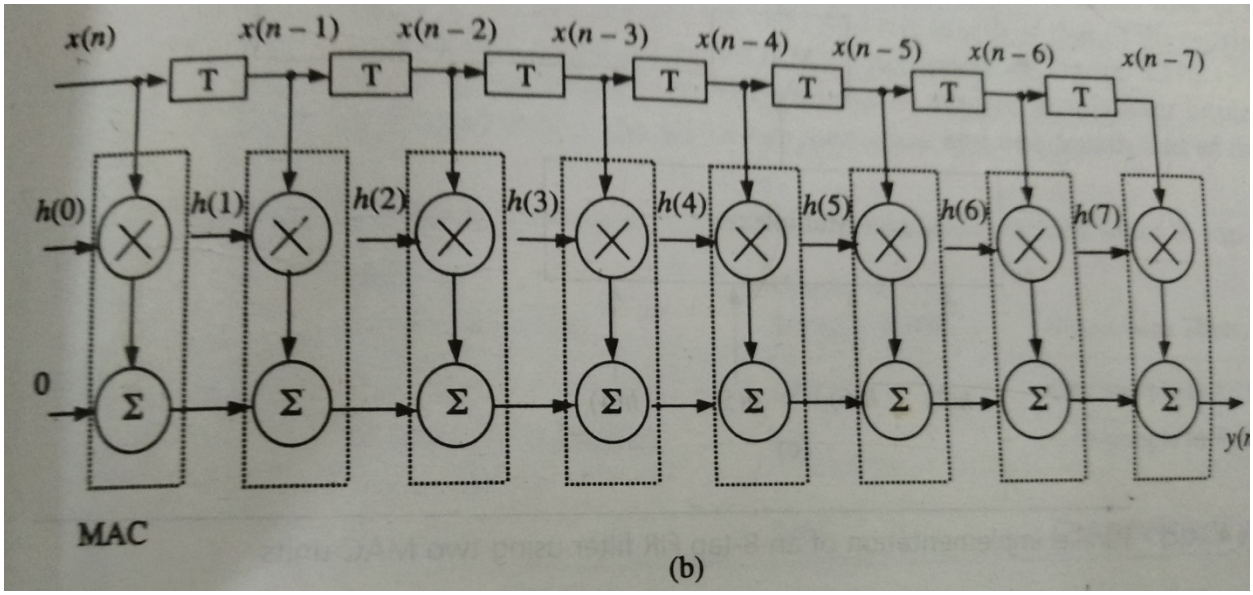
New PNTR ← Updated PNTR + Buffer size

Else

New PNTR ← Updated PNTR

6 (b) What is pipelining? Explain the implementation of 8-tap FIR filter using 8 MACs.

Sol:



- An architectural feature to increase the speed of DSP algorithm is known as ppelining
- The instruction to be executed is broken in to a number of steps
- As an example, execution of the instruction can be broken down into 5 different steps – Instruction fetch, decode, operand fetch, execute, save the result