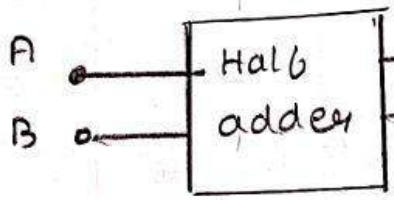
Q] Half adder: It is a combinational circuit which accepts two input and add the binary information Produces two outputs i.e sum and carry.

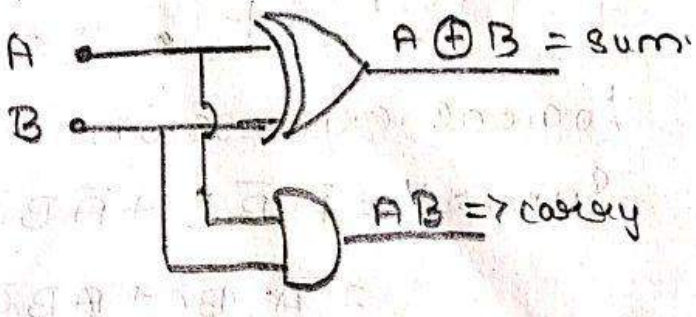
9



* Truth table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

* Representation

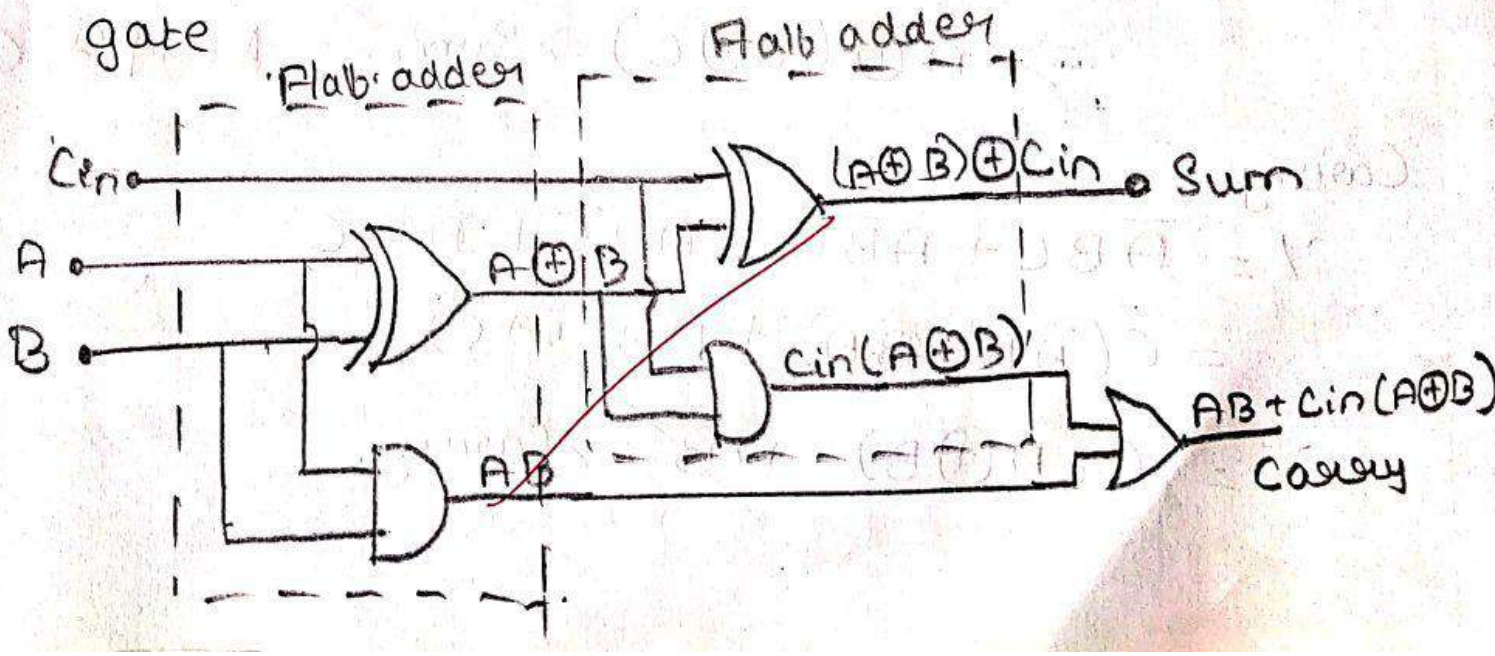


* logical Expression

$Y = A \oplus B = \bar{A}B + \bar{B}A = Sum$

$Carry = AB$

Fuller Adder using two half adder and an OR gate



A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logical expression

Sum: $Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$

Let us take $\bar{A} = x$, $B \oplus C = y$.

$= x\bar{y} + \bar{y}x$

$= x \oplus y$

$\Rightarrow \bar{A} \oplus (B \oplus C) \Rightarrow$ Sum $= A \oplus B \oplus C$

Carry.

$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= C(\bar{A}B + \bar{B}A) + AB(\bar{C} + C)$

$= C(A \oplus B) + AB \Rightarrow$ Carry.

Fulladder : It is a combinational circuit which accepts three input signal and produces a 2 output i.e Sum and carry.

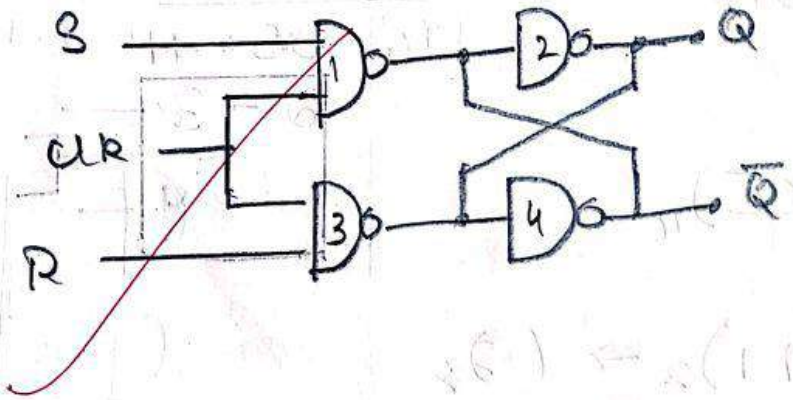
* The circuit is consists of 2 half adder and an OR gate.

5) a) RS flipflop

RS flip flop is a sequential circuit which requires a clock as one of the input and which produces 2 output.

The outputs are always complement to each other.

logic diagram.



Truth table:

Clk	S	R	Q	Qn+1	State
0	X	X	0	0	N.C
0	X	X	1	1	
↑	0	0	0	0	No change
↑	0	0	1	1	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	1	0	X	Invalid
↑	1	1	1	X	

Memory

Case1 When clk is not applied.
What ever be the value of S R it remains to be the same.

Case2: When clock is applied. when the S=R=0 the output remains the same. That is the memory condition.

Case2: When S=1 R=0 then it is the set condition and output turns to be 1.

S	R		
1	0	0	→ 1
1	0	1	→ 1

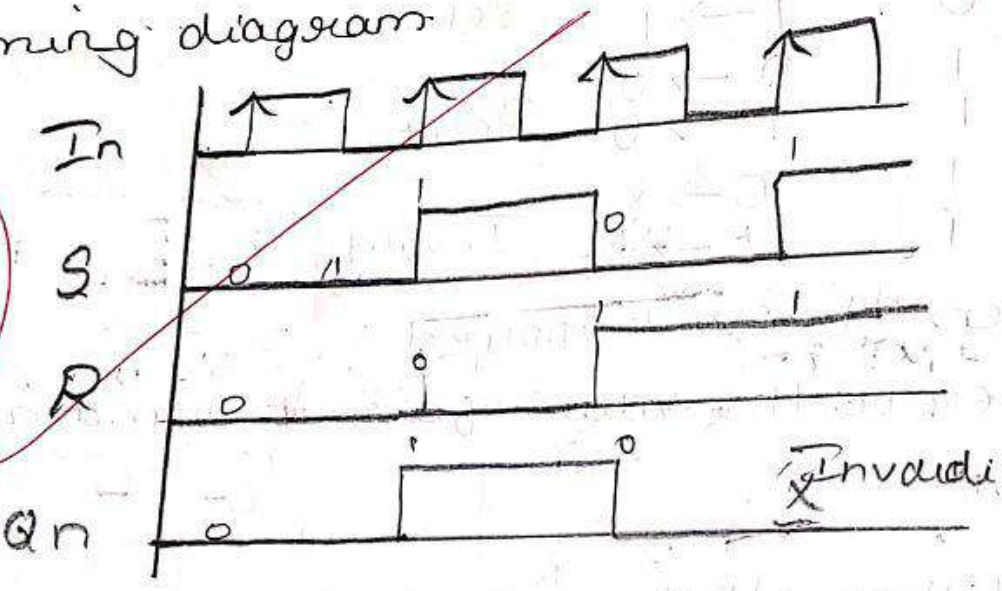
Case3: when S=0 R=1 then it is reset condition and output turns to be 0

S	R	Qn	Qn+1
0	1	0	→ 0
0	1	1	→ 1

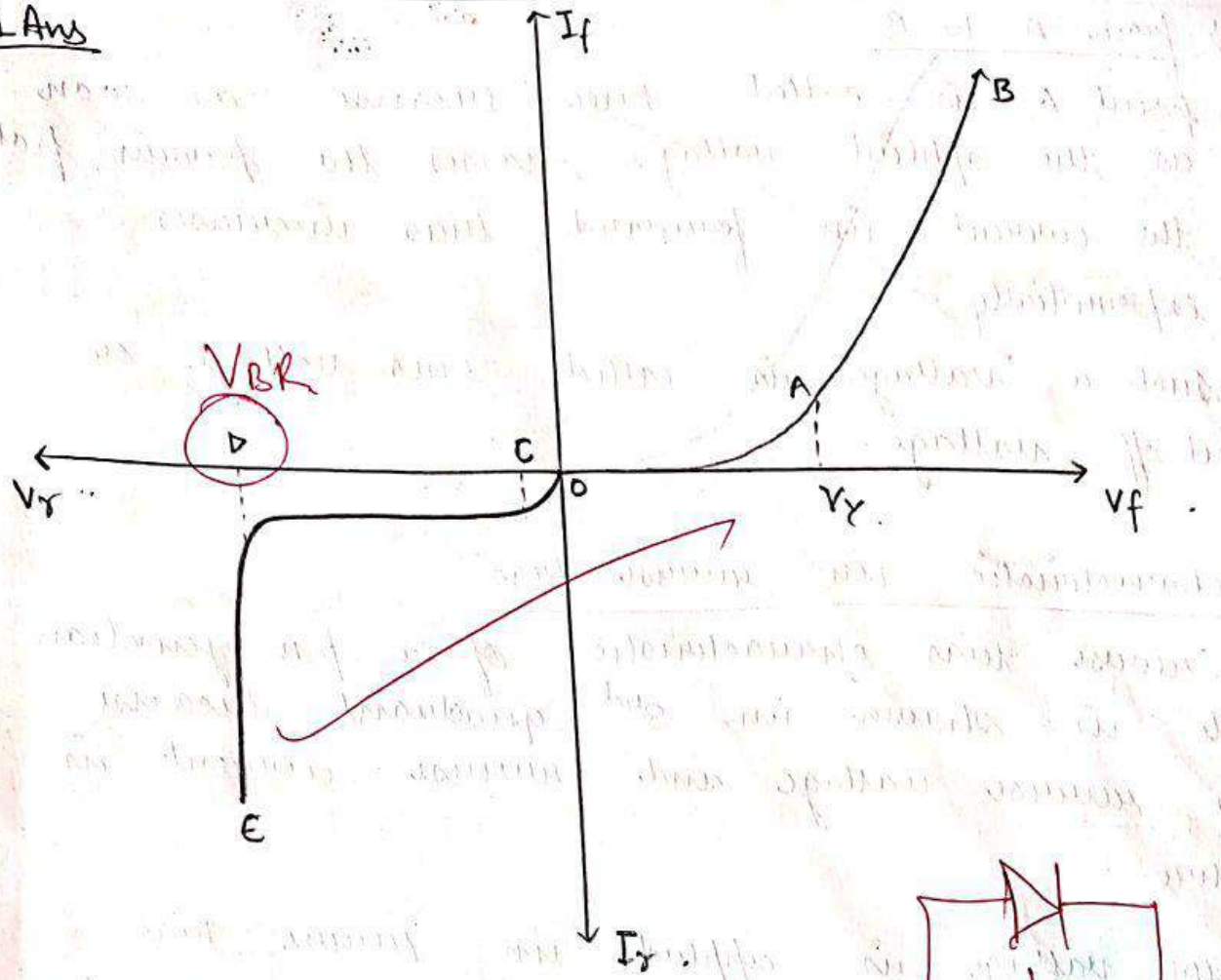
Case 4 : When both the ip input are 1 then it is Invalid condition that we can't predict the output

S	R	Qn	Qn+1	
1	1	0	→ X	} Invalid.
1	1	1	→ X	

Timing diagram



1 Ans



VI Characteristic in forward bias

The forward bias characteristic of a p-n junction diode is shown in the 1st quadrant because both forward voltage and current is +ve.

It can be divided into Two parts

i) from O to A.

From O to A the forward current is very less or almost equal to zero. Because the applied voltage is less than the barrier potential which is denoted by V_γ.

ii) from A to B.

point A is called knee because as soon as the applied voltage crosses the barrier potential the current in forward bias increases exponentially.

Such a voltage is called knee voltage or cut off voltage.

VI characteristic in reverse bias

The reverse bias characteristic of a p n junction diode is shown in 3rd quadrant because both reverse voltage and reverse current is negative.

As the voltage is applied in reverse bias first the current increases slowly but very less. Then from C to D the current remains constant for the applied increase in voltage. This current is called reverse saturation current.

At point D when the breakdown of p n junction takes place due to increase in reverse voltage, it is called reverse breakdown. At this point current through reverse bias increases drastically with almost no increase in voltage.

Diode Approximation

① Ideal diode

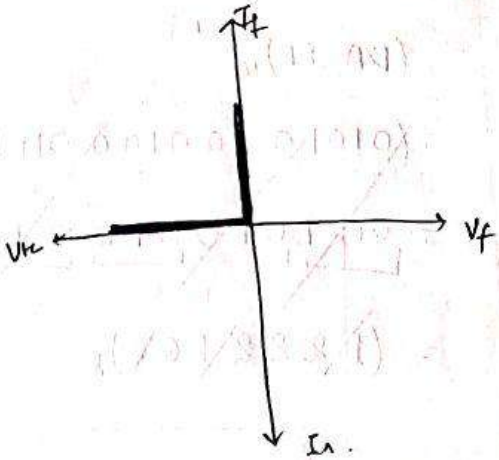
A diode in which cut off voltage is zero.

An ideal diode in forward bias acts as a wire.

of $R = 0$.

An ideal diode in reverse bias acts as short circuit

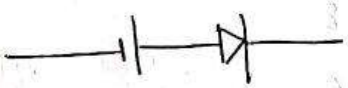
of $R = \infty$.

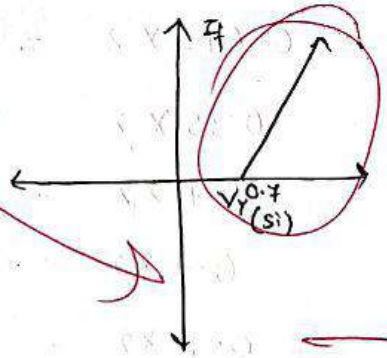


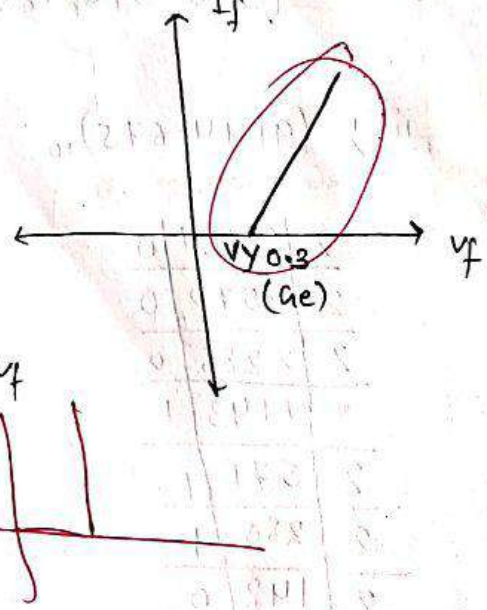
② Approximate diode

No diode is ideal.

Every diode has some resistance or cut off voltage.

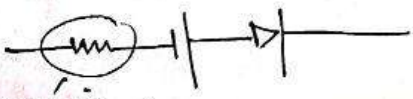


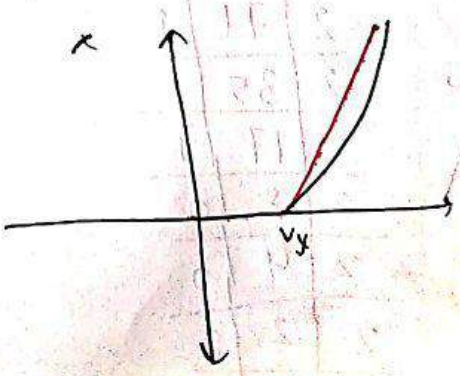




③ Piecewise linear approximation

Also has a dynamic resistance and turn on current increases.





4. i) $(DACFE)_{16} \longrightarrow (\ )_8$.

$(DACFE)_{16}$

$= (1101\,1010\,1100\,1111\,1110)_2$

$= 001\,101\,010\,100\,111\,110$

$= (1\,5\,2\,4\,7\,6)_8$

$(3\,3\,2\,6\,3\,7\,6)_8$

2

ii) $(834.446)_8 = (\ )_{10}$.

$= 8\times8^2 + 3\times8^1 + 4\times8^0 + 4\times8^{-1} + 4\times8^{-2} + 6\times8^{-3}$

$= 8\times64 + 3\times8 + 4 + \frac{4}{8} + \frac{4}{64} + \frac{6}{512}$.

$= 512 + 24 + 4 + 0.5 + 0.0625 + 0.01171875$

$= (540.57421875)_{10}$.

2

iii) $(9144.675)_{10} \longrightarrow (\ )_2 \longrightarrow (\ )_{16}$.

2	9144	0
2	4572	0
2	2286	0
2	1143	1
2	571	1
2	285	1
2	142	0
2	71	1
2	35	1
2	17	1
2	8	0
2	4	0
2	2	0
	1	

$0.675 \times 2 = 1.35$

$0.35 \times 2 = 0.7$

$0.7 \times 2 = 1.4$

$0.4 \times 2 = 0.8$

$0.8 \times 2 = 1.6$

$0.6 \times 2 = 1.2$

$0.2 \times 2 = 0.4$

$= (1000\,1110\,1110\,00.\,1010\,110)_2$.

0010 0011 1011 1000 · 10101100

(23B8 · AC)$_{16}$. (2)

iv) (10101·11011)$_2$ = ( )$_8$

010 101 · 110 110

(25·66)$_8$. (2)

v) (9FAC·58B)$_6$ = ( )$_{10}$

$= 9\times16^3 + 15\times16^2 + 10\times16^1 + 12\times16^0 + 5\times16^{-1} + 8\times16^{-2} + 11\times16^{-3}$

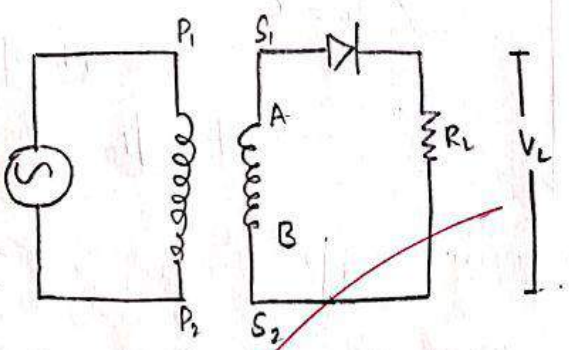
$= 9\times4096 + 15\times256 + 10\times16 + 12 + \frac{5}{16} + \frac{8}{256} + \frac{11}{4096}$

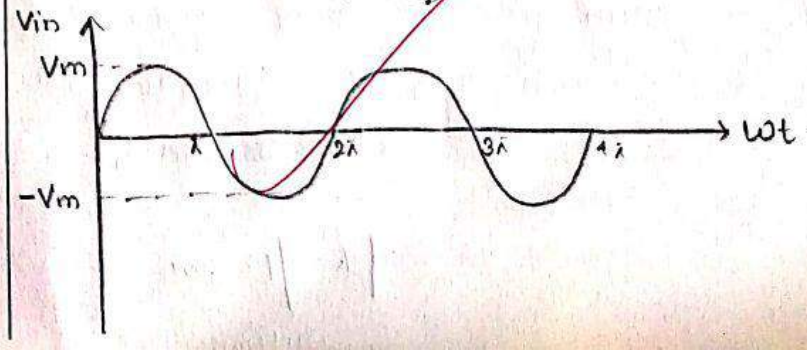
$= 9\times4096 + 15\times256 + 10\times16 + 12 + 0.3125 + 0.03125 + 2.6855\times10^{-3}$

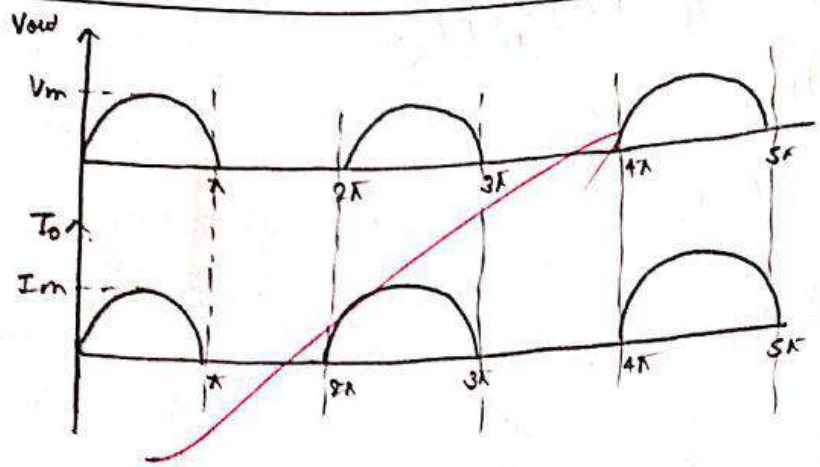
$= 36864 + 3840 + 172.346435$

$= (40876.34644)_{10}$. (2)

1. a) A rectifier is a device which convert ac signal into dc signal.







$V_o = V_m \sin \omega t$.

$I_o = I_m \sin \omega t$

Working

When an ac signal is passed then for 0 to π A is +ve and B is -ve . which means the diode is forward bias . and current passed

for π to 2π A is -ve and B is +ve which means the diode is reverse bias and no current passes to it

for 0 to π $V_o = V_m \sin \omega t$. $I_o = I_m \sin \omega t$.

for π to 2π $V_o = 0$. $I_o = 0$.

and this goes on .

b) $I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\omega t \, d\omega t$

$= \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\omega t \, dt + \int_{\pi}^{2\pi} \sin\omega t \, dt\right]$

$= \frac{I_m}{2\pi}\int_0^{\pi} \sin\omega t \, dt$

$= -\frac{I_m}{2\pi}\left[\cos\omega t \, dt\right]_0^{\pi}$

$= -\frac{I_m}{2\pi}\cos\pi - \cos 0$

$= -\frac{I_m}{2\pi}[-1-1]$

$= -\frac{I_m}{2\pi}(-2)$

$$\boxed{I_{dc} = \frac{I_m}{\pi}}$$

$V_{dc} = I_{dc} \times R_L$

$= \frac{I_m}{\pi} R_L$

$$\boxed{V_{dc} = \frac{R_L I_m}{\pi}}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_0^2 \, d\omega t}$$

$$= \frac{1}{\sqrt{2\pi}} \sqrt{\int_0^{2\pi} I_m^2 \sin^2 \omega t \, d\omega t}$$

$$= \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{2\pi} \sin^2 \omega t \, d\omega t}$$

$$= \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{\pi} \sin^2 \omega t \, d\omega t + \int_{\pi}^{2\pi} \sin^2 \omega t \, d\omega t}$$

$$= \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{\pi} \frac{1 - \cos 2\omega t}{2} \, d\omega t}$$

$$= \frac{I_m}{\sqrt{2\pi}} \sqrt{\int_0^{\pi} \frac{1}{2} \, d\omega t - \int_0^{\pi} \frac{\cos 2\omega t}{2} \, d\omega t}$$

$$= \frac{I_m}{\sqrt{2\pi}} \sqrt{\frac{1}{2}\pi - \left[\frac{\sin 2\omega t}{2}\right]_0^{\pi}}$$

$$= \frac{I_m}{\sqrt{2}\sqrt{\pi}} \times \frac{\sqrt{\pi}}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{2}$$

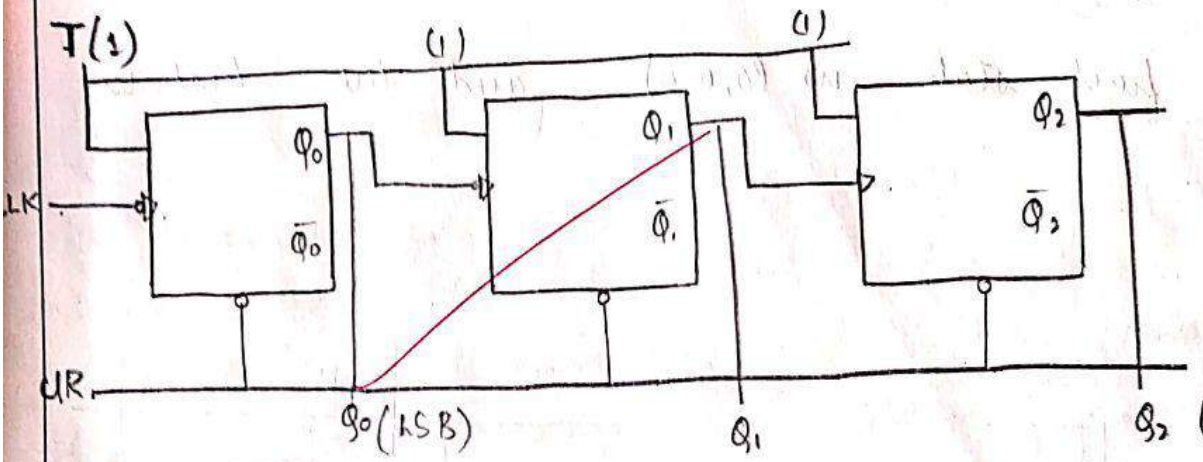
a) A 3 bit asynchronous counter is a sequential circuit which counts the number of clock pulses given to the J-K flip flop.

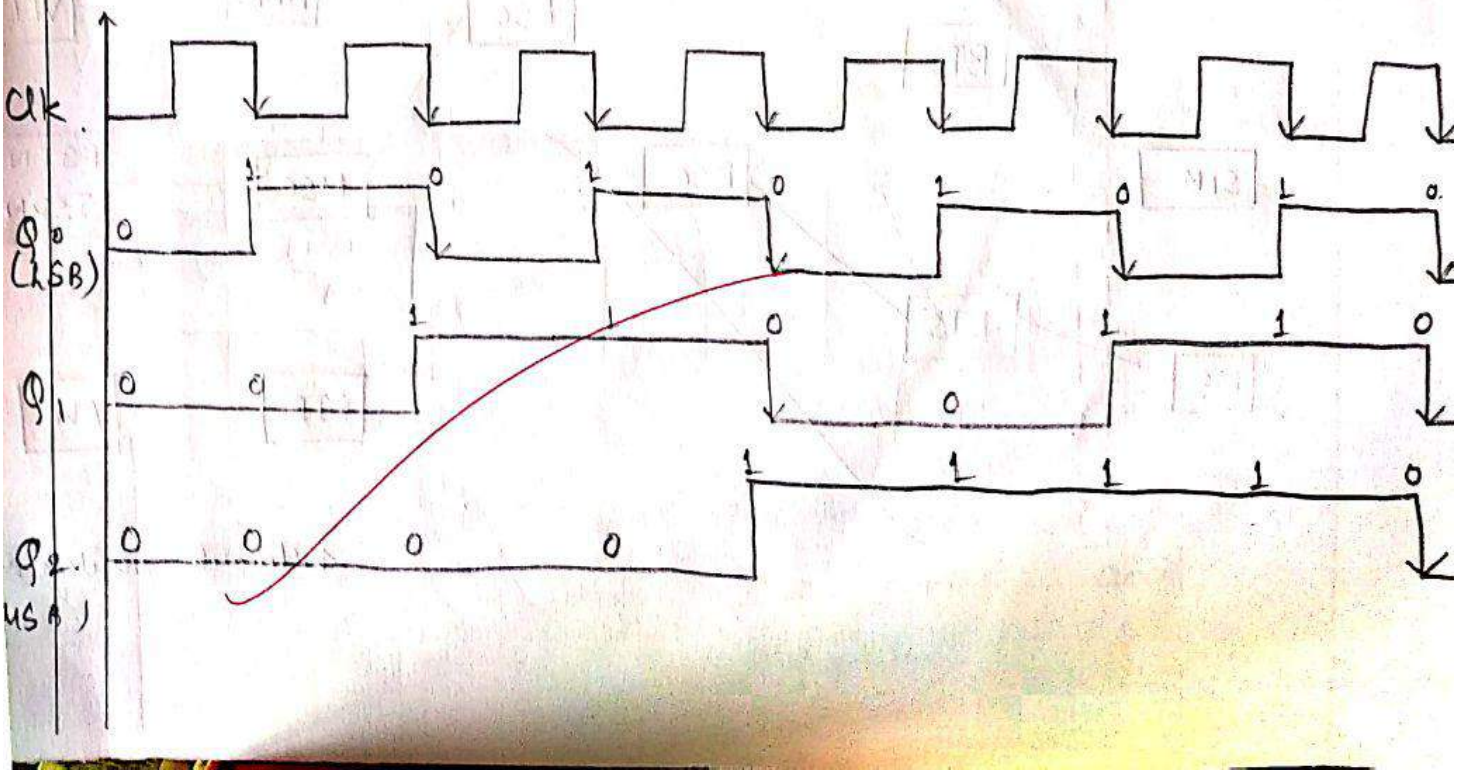
3 bit asynchronous counter:

no. of flip flop = 3 (n)

no. of states = $2^n = 2^3 = 8$.

max^m no. of counts it can go $= 2^n - 1 = 8 - 1 = 7$





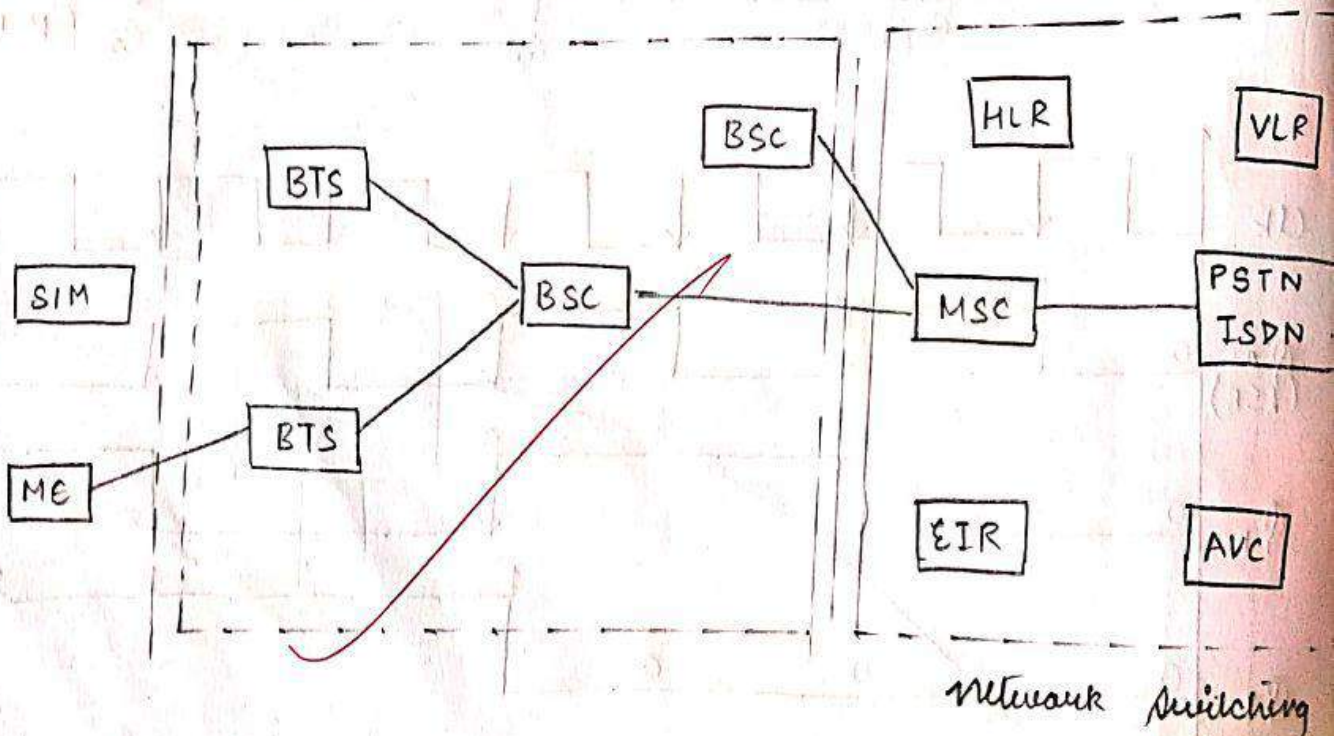
3 bit asynchronous counter means clock is given to the first JK flip flop and the output of first flip flop becomes the clock for next .. Q_0 is the LSB and Q_3 is the MSB.

After 7 states of counter the counter comes back to initial state.

For each clock pulse the counter goes to next state.

The first state is (0,0,0) and the last is (1,11).

b)



Network Switching

~~Mobile~~

GSM → Group Service Mobile is the 2nd Gennation of Mobile network.

The area is divided into different small areas called cell.

MSC → Mobile service switching Centre.

SIM → Subscriber Identity Module.

ME → Mobile Equipment.

SIM identifies the signal and passes it further.

The second parts consists of BTS (Basic Transceiver Station) and BSC (Basic station Controller) which has its own transmitter and receiver which provides communication b/w mobile network and MSC.

The network switching is the main part of mobile network. It consists of different registers. It provides main control.

HLR — Home Location Register.

consists of all the info of all subscribers.

VLR → Visitor Location Register.

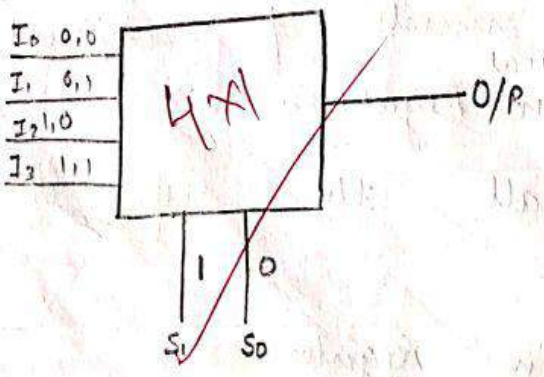
It selects info from HLR and provide it to subscriber.

EIR → Equipment Identity Register.
It decides whether the mobile device is of given network or not.

AUC → It has the authentication database of the user SIM card.

7. a) Multiplexer is a combination circuit which accepts multiple signals but gives output in a single signal. It is also called (MUX) and data selector.
It is of various types.
2X1 4X1 8X1 6X1

4X1



n → no. of input.
$n = 2^m$
m → no. of select lines.

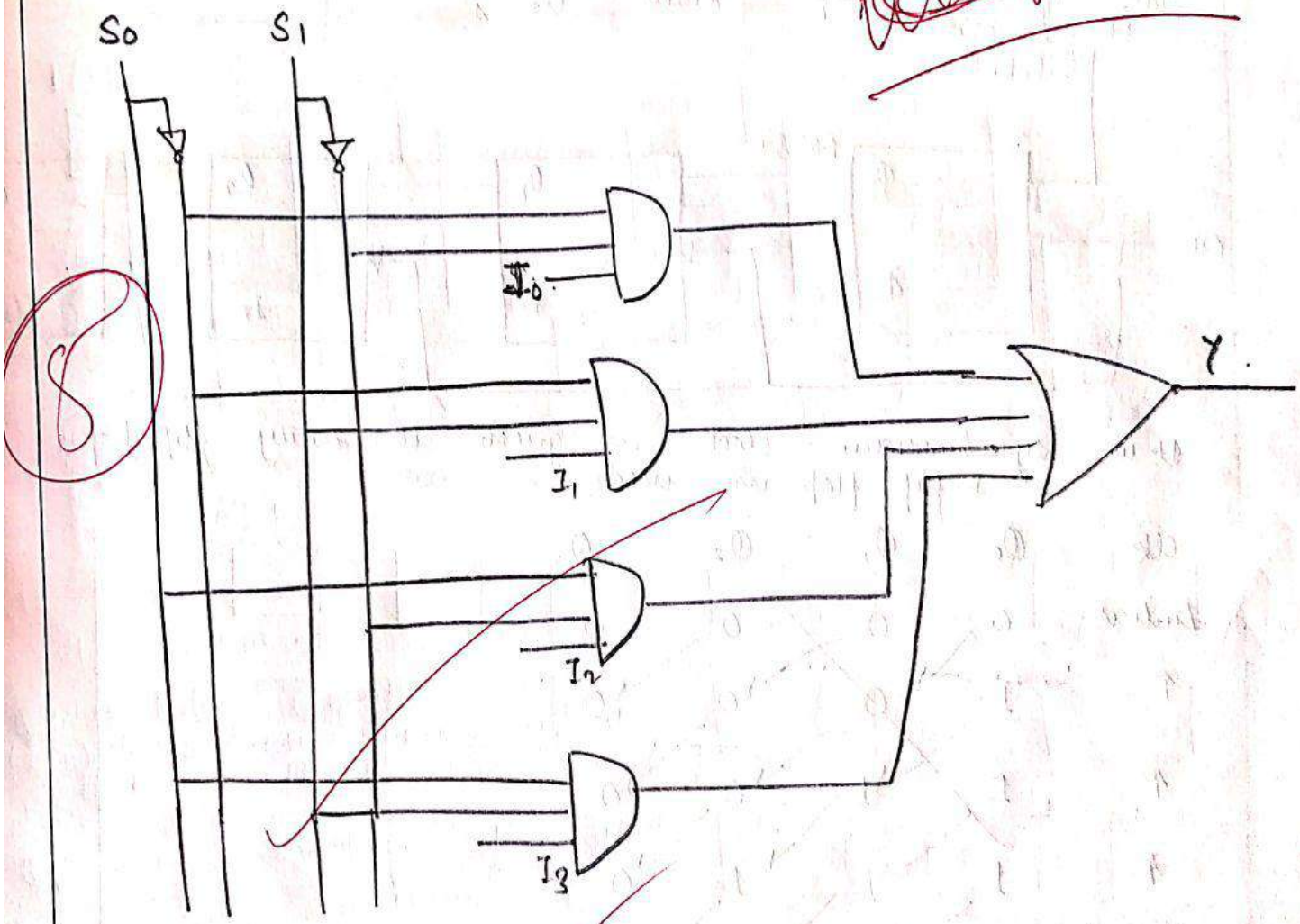
$4 = 2^2$

2 select lines are present in 4X1

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \overline{S_0}\,\overline{S_1} I_0 + \overline{S_0} S_1 I_1 + S_0 \overline{S_1} I_2 + S_0 S_1 I_3$$

Select lines select the input and gives them as output.



If S_0 is selected 1st and S_1 is selected next then output is 0,1 which is I_1.

If S_0 is selected twice then the output is (0,0) when is I_0 and so on.

This is the way it works.

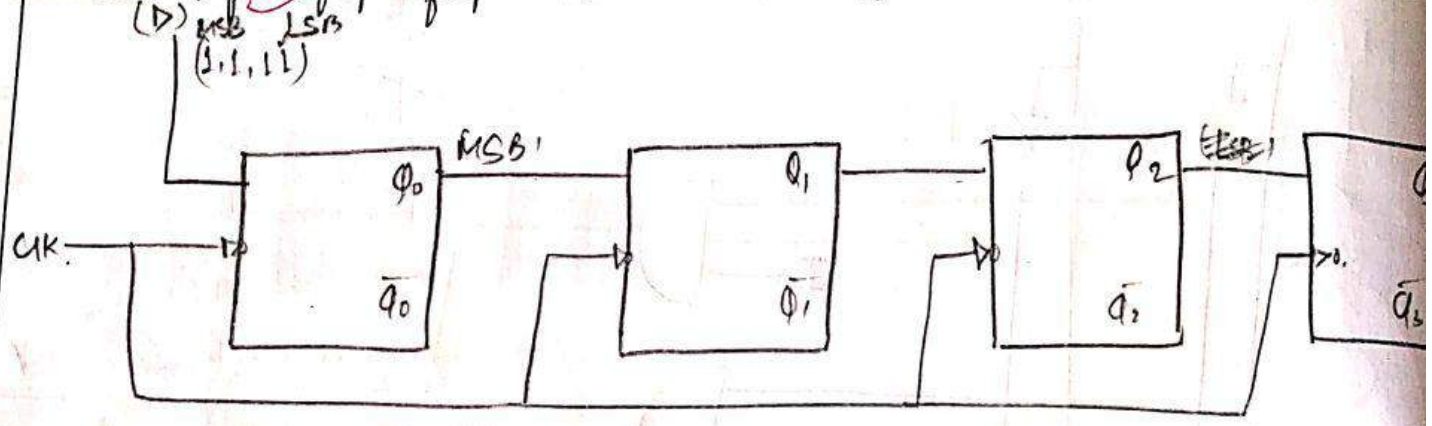
b) A J K flip flop can store only bit of information. when we have to store more than 1 bit of info than we combine many J K flip flop called register.

When a register can shift info from left to right or right to left is called shift register.

SISO — Sirial Input Serial Output.

4 bit shift register

No. of flip flop used is 4.

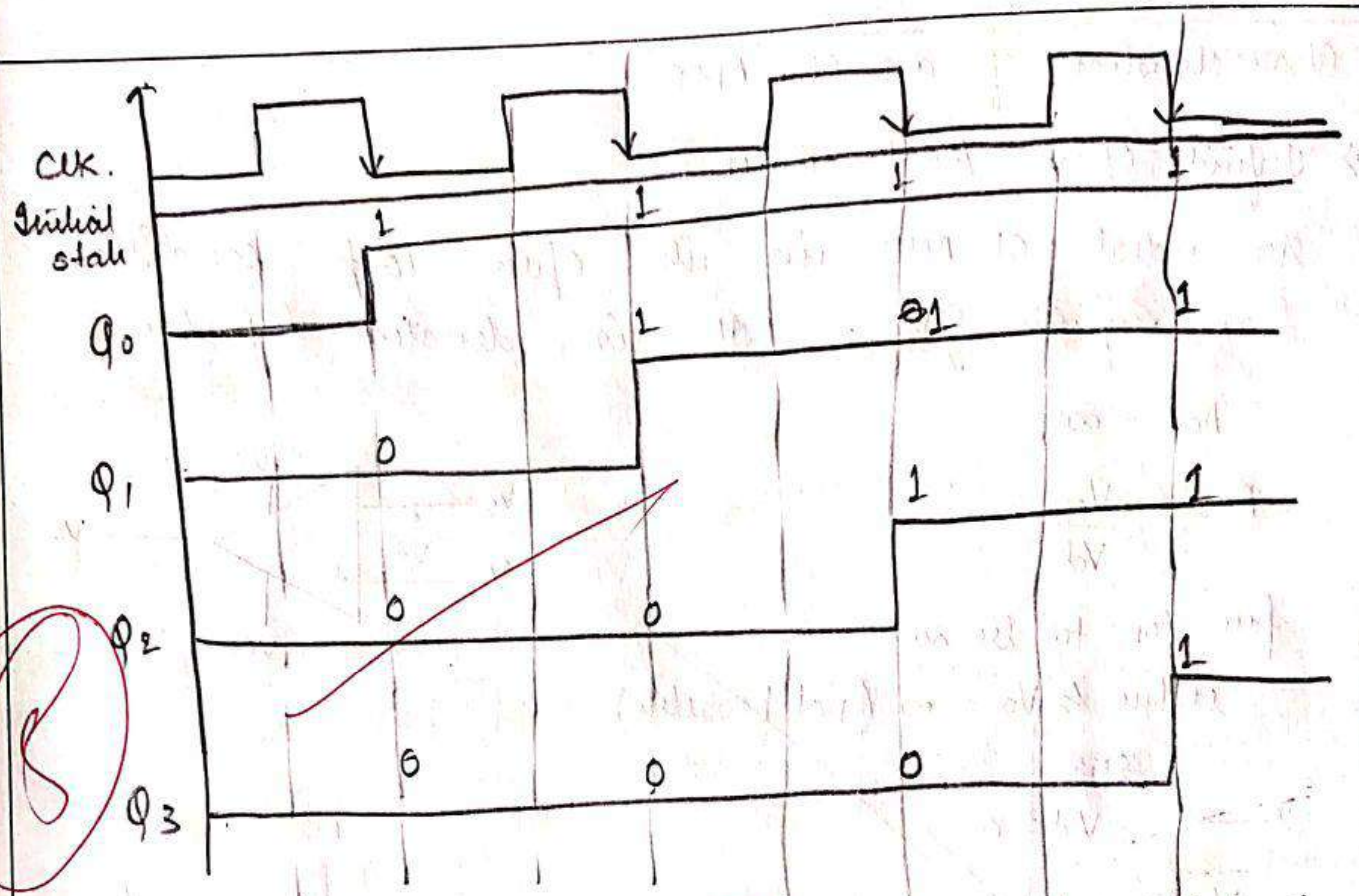


It is synchronous. Clock is given to every flip flop.

D flip flop is used.

Clk	Q_0	Q_1	Q_2	Q_3
Initial	0	0	0	0
↑	1	0	0	0
↑	1	1	0	0
↑	1	1	1	0
↑	1	1	1	1

(MSB) (LSB)



First LSB information is passed and then the data moves on shifting. Each J/K flip flop work one by one. First the 1st J/K works then the 2nd and so on:

Finally all the data shifts and we get (1, 1, 1, 1) as our output.

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Internal Assesment Test - I

Sub:	Basic Electronics							Code:	18ELN14
Date:	17/10 / 2018	Duration:	90 mins	Max Marks:	50	Sem:	I	SEC:	I,J,K,L,M,N,O

Answer Any **FIVE FULL** Questions

		Marks	OBE CO	OBE RBT
1	Draw and explain V-I Characteristics of Practical PN junction Diode. Also, explain diode Approximate DC equivalent model.	[10]	CO1	L2
2	Explain Half Adder circuit and Realize a Full Adder using two Half Adder and an OR Gate. Write truth table and expression for sum and carry output.	[10]	CO5	L2
3(a)	What is a rectifier? With a neat circuit diagram, explain the working of a half wave rectifier along with relevant waveforms.	[05]	CO2	L2
(b)	Derive the expressions for I_{dc}, V_{dc}, I_{rms} of a half-wave rectifier	[05]	CO5	L3
4	Perform the following Conversions. (i) $(DACFE)_{16} \rightarrow (?)_8$ (ii) $(834.446)_8 \rightarrow (?)_{10}$ (iii) $(9144.675)_{10} \rightarrow (?)_2 \rightarrow (\ )_{16}$ (iv) $(10101.11011)_2 \rightarrow (?)_8$ (v) $(9FAC.58B)_{16} \rightarrow (?)_{10}$	[10]	CO5	L3
5 (a)	With a logic diagram and truth table, explain the operation of a clocked RS flip- flop.	[05]	CO5	L2
(b)	Simplify the Boolean expression and implement using NAND gate . (i) Y=AC+ ABC+ A´ BC+ AB+ D (ii) Y=A B´ C´ + A´ B´ C´ + A´ B´ + A´ C´	[05]	CO5	L3

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USN	1	C	R							

Internal Assesment Test - III

Sub:	Basic Electronics							Code:	17ELN25
Date:	23/5 / 2018	Duration:	90 mins	Max Marks:	50	Sem:	II	SEC:	I,J,K,L,M,N,O

Answer Any **FIVE FULL** Questions

		Marks	OBE CO	OBE RBT
1	Draw and explain V-I Characteristics of Practical PN junction Diode. Also, explain diode Approximate DC equivalent model.	[10]	CO1	L2
2	Explain Half Adder circuit and Realize a Full Adder using two Half Adder and an OR Gate. Write truth table and expression for sum and carry output.	[10]	CO5	L2
3 (a)	What is a rectifier? With a neat circuit diagram, explain the working of a half wave rectifier along with relevant waveforms.	[05]	CO2	L2
(b)	Derive the expressions for I_{dc}, V_{dc}, I_{rms} of a half-wave rectifier.	[05]	CO5	L3
4	Perform the following Conversions. (ii) $(DACFE)_{16} \rightarrow (?)_8$ (ii) $(834.446)_8 \rightarrow (?)_{10}$ (iii) $(9144.675)_{10} \rightarrow (?)_2 \rightarrow (\ )_{16}$ (iv) $(10101.11011)_2 \rightarrow (?)_8$ (v) $(9FAC.58B)_{16} \rightarrow (?)_{10}$	[10]	CO5	L3
5 (a)	With a logic diagram and truth table, explain the operation of a clocked RS flip- flop.	[05]	CO5	L2
(b)	Simplify the Boolean expression and implement using NAND gate . (i) Y=AC+ ABC+ A´ BC+ AB+ D (ii) Y=A B´ C´ + A´ B´ C´ + A´ B´ + A´ C´	[05]	CO5	L3

6 (a)	What is a counter? With a neat timing and block diagram, explain three bit asynchronous counter operation.	[05]	CO5	L2
(b)	With a neat block diagram explain GSM system.	[05]	CO6	L2
7	(a)What is a multiplexer? Explain the working of 4:1 multiplexer.	[05]	CO5	L2
	(b) What is a shift register? Explain the working of a 4-bit SISO shift register.	[05]	CO5	L2

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