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		* CMR INSTITUTE O	TECHNOLOGY, E	
	Internal Assessment Test II – Oct. 2018			
S	Sub: DSP Algorithms and Architecture Sub Code: 15EC751 B	ranch:	EC1	Ξ
Da	ate: 17/10/2018 Duration: 90 mins Max Marks: 50 Sem / Sec: 7/A,B,C		OI	
	Answer any FIVE FULL Questions	MAR KS	CO	RBT
1	Explain Functional Architecture of TMS320C54XX Processor, with a Block Diagram.	[10]	CO3	L1
2 (a)	Discuss briefly about the Direct and Indirect addressing modes of TMS320C54XX Processor.	[07]	CO3	L2
(b)	Assuming the current content of AR3 to be 220h, what will be its contents after each of the following TMS320C54xx addressing modes is used? Assume that the	[03]	CO3	L3
3)	contents of AR0 are 10h. a. *AR3+0 b. *AR3-0 c. *AR3+ d. *AR3 e. *AR3 - f. *+AR3 (40h) Write an assembly language program of TMS320C54XX Processors to compute the sum of three product terms given by the equation,	f [10]	CO3	L3
4(a)	y(n) = h(0) x(n) + h(1) x(n-1) + h(2) x(n-2) with usual notations. Use MAC Instruction and Indirect Addressing mode. Explain the 6 level pipeline operation of TMS320C54XX.	[05]	CO3	L1
(b)	By means of a figure explain the pipeline operation of the following sequence of instruction is the initial values of AR1,AR3,A are 104,101, 2 and the values stored in the memory locations 101,102,103,104 are 4,6,8,12.Also provide the values of registers AR3,AR1,T and accumulated after completion of each cycle. ADD *AR3+,A LD*AR1+,T MPY*AR3+,B	3	CO3	L3
5(a)	ADD B,A Describe host port interface and explain its signals.	[05]	CO3	L2

Briefly describe the following instructions of TMS320C54XX processors with an

Draw the functional diagram of multiplier/ adder unit of TMS320C54XX processors and

Draw and explain the functional diagram of Barrel shifters of TMS320C54XX processors.

example. i) MAC *AR5, +*AR6+, A, B ii) RPT Smem iii) RPTB iv) BANZ,

v) MAS *AR3-, *AR6+, B, A

6(a)

(b)

explain.

(b)	By means of a figure explain the pipeline operation of the following sequence of instruction if the initial values of AR1,AR3,A are 104,101, 2 and the values stored in the memory locations 101,102,103,104 are 4,6,8,12. Also provide the values of registers AR3,AR1,T and accumulator after completion of each cycle. ADD *AR3+,A LD*AR1+,T MPY*AR3+,B ADD B,A	[05]	CO3	L3
5(a)	Describe host port interface and explain its signals.	[05]	CO3	L2
(b)	Briefly describe the following instructions of TMS320C54XX processors with an example. i) MAC *AR5, +*AR6+, A, B ii) RPT Smem iii) RPTB iv) BANZ, v) MAS *AR3-, *AR6+, B, A	[05]	CO3	L2
6(a)	Draw the functional diagram of multiplier/ adder unit of TMS320C54XX processors and explain.	[05]	CO3	L1
(b)	Draw and explain the functional diagram of Barrel shifters of TMS320C54XX processors.	[05]	CO3	L1

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Sub:	DSP Algorith	nms and Architecture			Sub Code:	15EC751	Branch:	EC	Έ
Date:	17/10/2018	Duration: 90 mins	Max Marks:	50	Sem / Sec:	7/A,B,C		OI	BE.
		Answer any	FIVE FULL Q	uestio	<u>ns</u>		MAR	CO	RBT
							KS		
1	Explain Funct	ional Architecture of T	MS320C54XX	Proce	ssor, with a I	Block Diagram.	[10]	CO3	L1
2 (a)	Discuss briefly	about the Direct and	Indirect addre	ssing n	nodes of TMS	S320C54XX Processo	or. [07]	CO3	L2
(b)	Assuming the	current content of AR	3 to be 220h, v	vhat w	rill be its con	tents after	[03]	CO3	L3
	each of the fol	lowing TMS320C54xx	addressing mo	des is	used? Assum	e that the			
	contents of AF	R0 are 10h.							
	a. *AR3+0	b. *AR3-0	c. *AR3+						
	d. *AR3	e. *AR3 -	f. *+AR3 (4	0h)					
3	Write an asse	mbly language progra	m of TMS3200	C54XX	Processors	to compute the sum	of [10]	CO3	L3
	three product	terms given by the equ	iation,						
	y(n) = h(0)	x(n)+h(1) x(n-1)+h(2)	2) x(n-2) with ι	ısual n	otations. Use	2			
	MAC Instruct	tion and Indirect Addr	essing mode.						
4 (a)	Explain the 6	level pipeline operatio	n of TMS320C	C54XX	.		[05]	CO3	L1