# Integrating Type (DVM) (Voltage to time)

① The dual slope DVM based its operation on the principle of voltage to time conversion.

② At the start of the cycle the counter is reset and the F/F changes its status to '0'.

③ The switch drive now opens $S_2$ and closes $S_1$, here by connecting the i/p voltage, under measurement to the terminals of the integrator ckt.

④ The capacitor starts charging and the o/p $e_o$ crosses '0'. The zero comparator generates a pulse which opens the gate.

⑤ The pulses from the oscillator ckt start reaching the counter which increment on each pulse.

⑥. The i/p in this case is integrated for a constant period of time, which ~~in this case~~ is the time it takes for the counter to reach its full count, with its slope being proportional to the magnitude of the i/p.

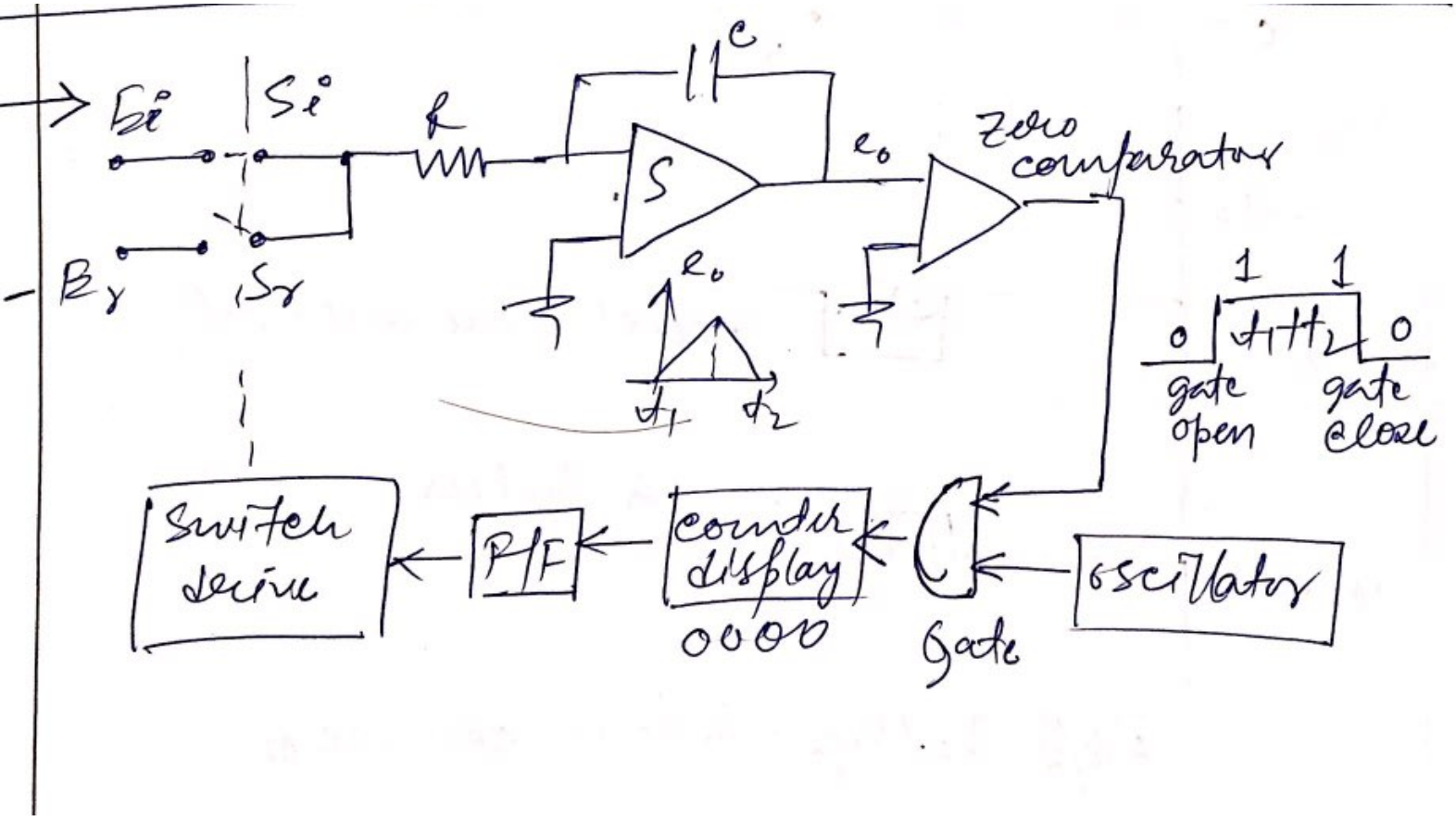
⑦. On the next pulse, the counter overflows and the FF changes its state to '1'.

⑧. The switch drive now opens 'Si' and closes 'Sr'. Thus by connecting a (-ve) reference voltage to the terminals of the integrator.

⑨. The capacitor now starts discharging and it allowed to discharge completely. with a constant slope proportional to the (-ve) reference.

(10). When the capacitor completely discharges ($e_o = 0$), the zero comparator generates a pulse which closes the gate.

(11). The count stored in the counter ckt now represent the time it takes by the capacitor to discharge completely for a given magnitude of the i/p, which is displayed in terms of voltage under measurement.



During charging (=

$$e_0 = -\frac{1}{RC}\int_0^{t_1} e_i\,dt = -\frac{e_i t_1}{RC} \quad \text{— (1)}$$

During discharging (=

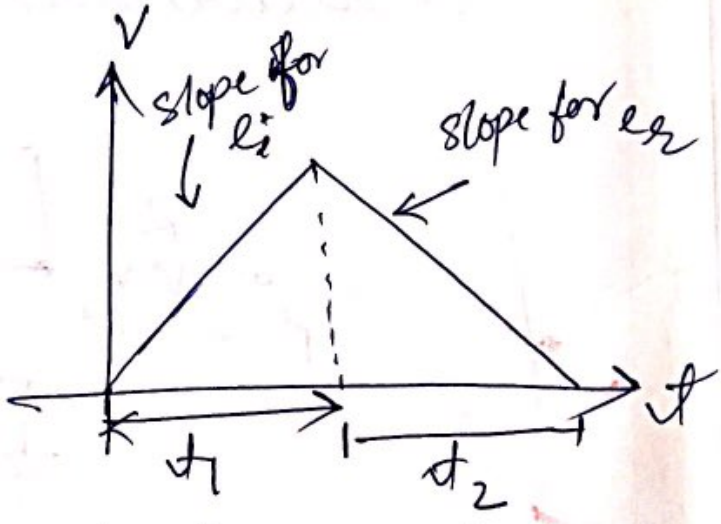
$$e_0 = +\frac{1}{RC}\int_0^{t_2} (-e_R)\,dt = \frac{-e_R t_2}{RC} \quad \text{— (2)}$$

(1) − (2) ⇒

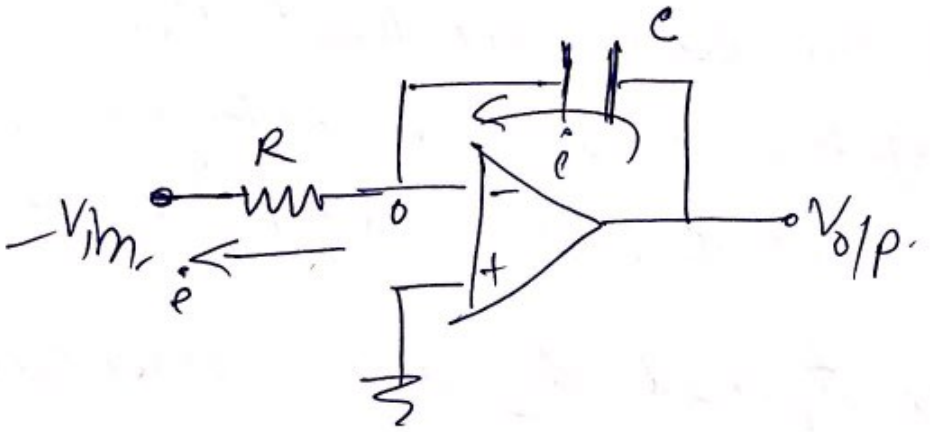
$$0 = \frac{-e_i t_1}{RC} + \frac{e_R t_2}{RC}$$

$$\Rightarrow 0 = e_R t_2 - e_i t_1$$

$$\Rightarrow \boxed{e_i = \frac{e_R t_2}{t_1}} \quad \text{— (3)}$$




If the oscillator time period is 'T' and the digital counter indicates $n_1$ and $n_2$ counts, respectively




$$\frac{0-(-V_{in})}{R} = i$$

$$\Rightarrow \frac{V_{in}}{R} = C\frac{dV_o}{dt}$$

$$\Rightarrow V_o = \frac{1}{RC}\int_0^t V_{in}\,dt$$

$$i = \frac{dQ}{dt}$$

$$Q = CV_c$$

$$i = C\frac{dV_c}{dt}$$

$$= C\frac{dV_o}{dt}$$

$$e_i^\circ = \frac{n_2 T}{n_1 T} e_R$$

$$\Rightarrow e_i^\circ = \frac{n_2}{n_1} e_R$$

But $n_1$ and $e_R$ are constant

$$K_1 = \frac{e_R}{n_1}$$

$$\boxed{e_i^\circ = K_1 n_2} \quad \text{---(1)}$$

$$\boxed{E_i^\circ \propto n_2}$$ no. of count.

From eq³ (3) we can say that the accuracy of the measured voltage is independent of the integrator time constant.

→ Also the time $t_1$ and $t_2$ are measured by the count of the clock given by the numbers $n_1$ and $n_2$ respectively. The clock ~~frequency~~ oscillator period 'T' and $n_1$ and $e_R$ are also constant. Therefore the accuracy of the method is also independent of the oscillator frequency.

# $(3\frac{1}{2})$ Digit.

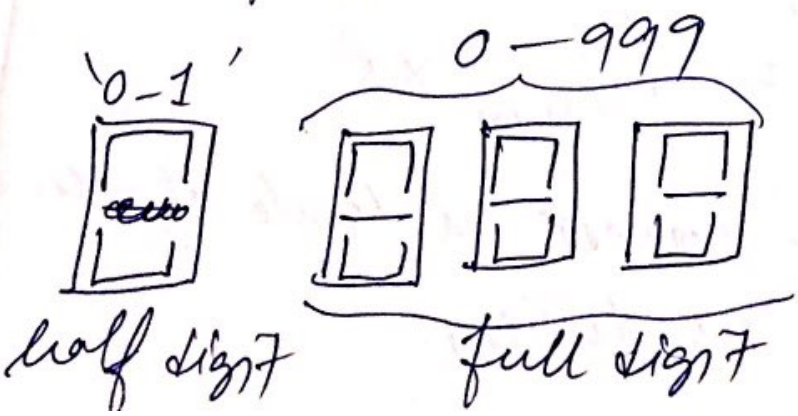
→ The number of digit positions used in a digital meter determines the resolution.

→ In a 3 digit display on a DVM for a (0-1)V range will indicate values from 0-999mV, with a smallest increment of 1mV.

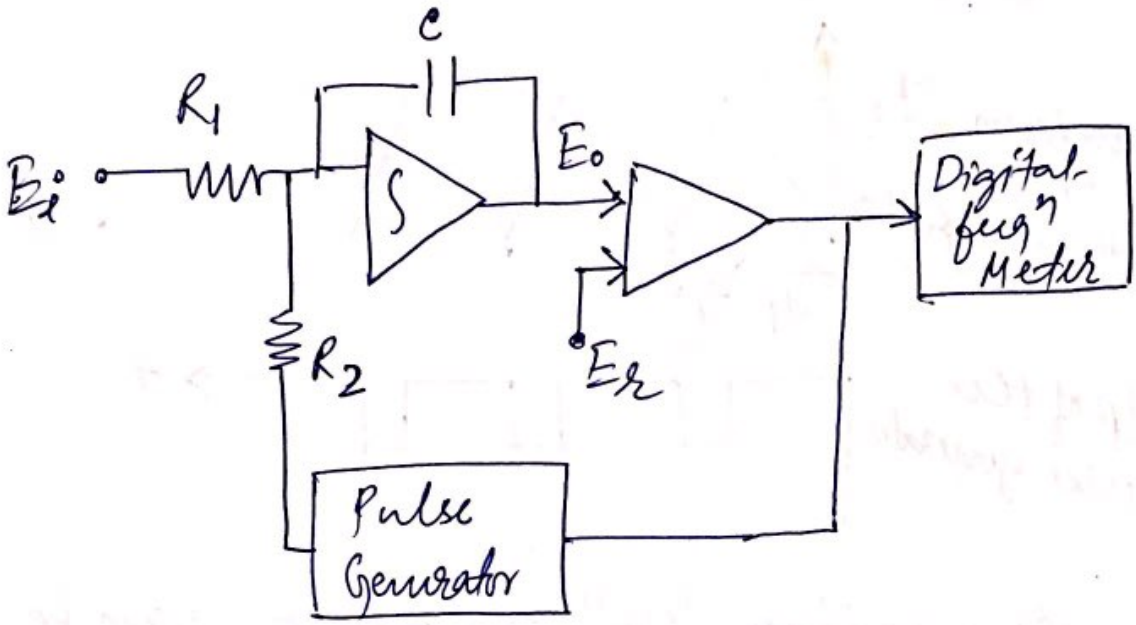
→ Normally a fourth digit capable of indicating '0 or 1' (hence called half digit) is placed to the left.

→ This allows the digital meter to read values above 999 up to 1999, this process is called overranging.

→ This type of display is called a $3\frac{1}{2}$ digit display.



# Integrating Type DVM (Voltage to Frequency Conversion)

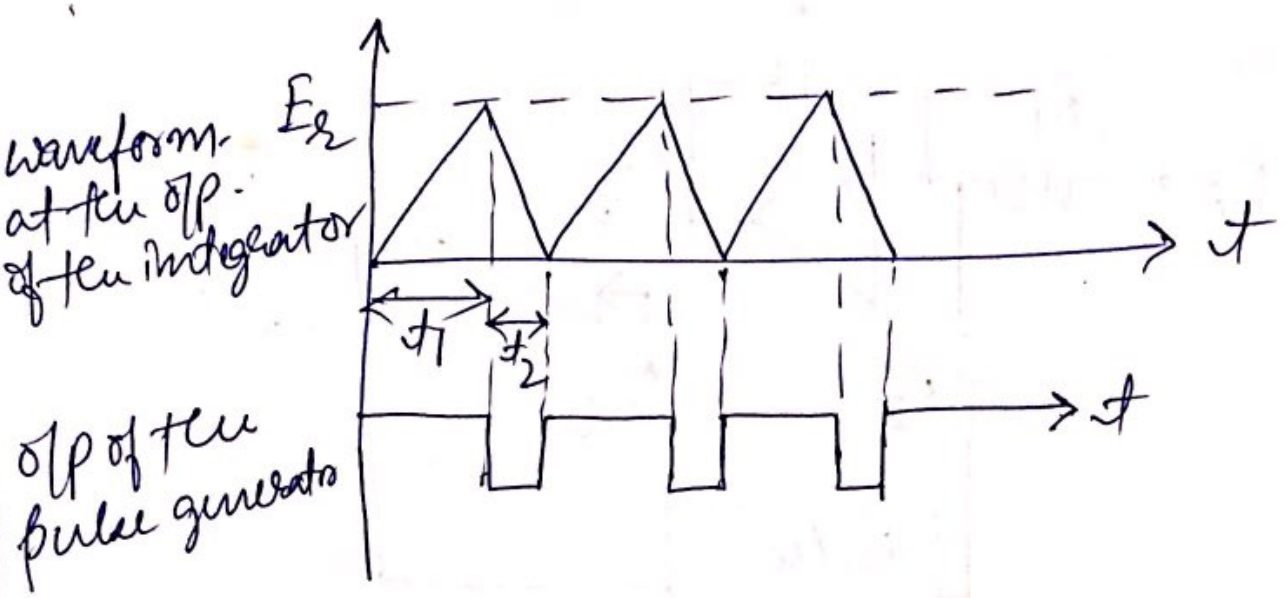



(1) The i/p voltage produces a charging current $E_i/R_1$, that charges the capacitor 'C' to the reference voltage $E_r$.

(2) When $E_r$ is reached, the comparator changes state, so as to trigger the pulse generator.

(3) The pulse generator produces a pulse that rapidly discharges the capacitor.

(4) The rate of charging and discharging (produces a signal freq^n) that is directly proportional to $E_i$.




The voltage freq$^n$ conversion can be considered to be a dual slope method.

$$E_i = \frac{E_R t_2}{t_1}$$

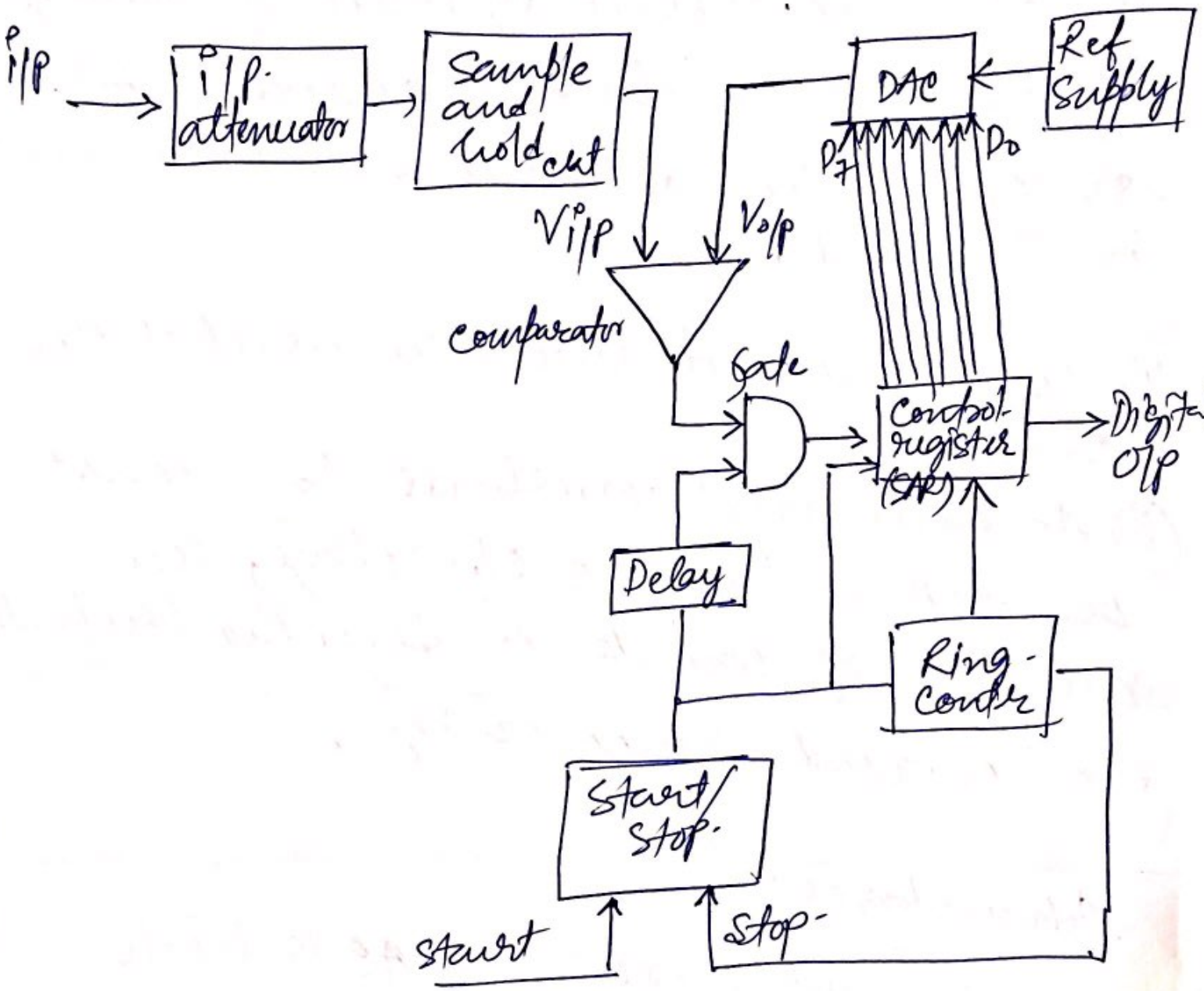
But in this case $E_R$ and $t_2$ are constant

$$K_2 = E_R t_2$$

$$E_i = K_2\left(\frac{1}{t_1}\right) = K_2 f_0 \qquad \boxed{E_i \propto f_0}$$

the o/p freq$^n$ is proportional to the i/p voltage $E_i$.

# (Successive Approximation)



(1) → In SAR type ~~DAC~~ ADC, comparator is used in i/p. to compare i/p. analog voltage with. FB voltage provided by DAC.

(2) → In (SAR) register, in order to successfully approximate ring counter is used.

(3) → Ring counter will set 1 by 1 bit from. MSB to LSB, with each clock.

(4) → Control ckt is used to reset current (or) present bit, in SAR, when. the analog voltage ($V_A$) is. lesser than the FB voltage (No i/p)

(2) When the start pulse signal is activated the control circuit, the successive approximation register (SAR) is cleared. In this case the O/P of the SAR is 00000000 and $V_{op}$ of the D/A converter is '0'.

(6) Now if $V_{in} > V_{o/p}$ the comparator o/p is positive. and the gate opens.

(7) During the set clock pulse the control- ckt sets the $D_7$ to '1', ~~and V_o/p jumps to~~.

(8) if $V_{in} < V_{o/p}$ the comparator o/p is -ve' and the control- circuit resets '$D_7$'.

(9) However if $V_{in} \geq V_{o/p}$ then the comparator o/p is '+ve' and the control- circuits keeps $D_7$ 'set'.

(5) 00110011

| | | |
|---|---|---|
| Start | 1000 \| 0000 → 128 | $V_{in} < V_{o/p} \rightarrow D_7$ reset |
| | 0100 \| 0000 → 64 | $V_{in} < V_{o/p} \rightarrow D_6$ reset |
| | 0010 \| 0000 → 32 | $V_{in} > V_{o/p} \rightarrow D_5$ set |
| | 0011 \| 0000 → 48 | $V_{in} \geq V_{o/p} \rightarrow D_4$ set |
| | 0011 \| 1000 → 56 | $V_{in} < V_{o/p} \rightarrow D_3$ reset |
| | 0011 \| 0100 → 52 | $V_{in} < V_{o/p} \rightarrow D_2$ reset |
| | 0011 \| 0010 → 50 | $V_{in} > V_{o/p} \rightarrow D_1$ set |
| Stop → | 0011 \| 0011 → 51 | $V_{in} > V_{o/p} \rightarrow D_0$ set |

(37)

128 64 32 16 8 4 2 1

0 0 0 0 0 0 0 0

0 0 1 0 1 0 1 0 1

| | | | |
|---|---|---|---|
| Start | 1000 | 0000 → 128 | $V_{in} < V_{o/p}$ |
| | 0100 | 0000 → 64 | $V_{in} < V_{o/p}$ |
| | 0010 | 0000 → 32 | $V_{in} > V_{o/p}$ |
| | 0011 | 0000 → 48 | $V_{in} < V_{o/p}$ |
| | 0010 | 1000 → 40 | $V_{in} < V_{o/p}$ |
| | 0010 | 0100 → 36 | $V_{in} > V_{o/p}$ |
| | 0010 | 0110 → 38 | $V_{in} < V_{o/p}$ |
| Stop | 0010 | 0101 → 37 | $V_{in} > V_{o/p}$ |