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Internal Assesment Test 2 – Nov. 2017

Sub:	COMPUTER ORGANIZATION					Sub Code:	15CS34	Branch:	CSE
Date:	07 / 11 / 2017	Duration:	90 mins	Max Marks:	50	Sem / Sec:	3(A,B,C)		OBE

Answer **FIVE** FULL questions selecting AT LEAST ONE question **FROM EACH PART**

		MARKS	CO	RBT
	PART A			
1 (a)	With a neat diagram, explain general 8-bit serial interface.	[10]	CO2	L2
	OR			
2 (a)	With neat timing diagrams, explain asynchronous bus.	[10]	CO2	L2
	PART B			
3 (a)	Explain USB bus.	[10]	CO2	L2
	OR			
4 (a)	Consider sixteen words and each word having eight bits. Draw internal organization of the specified RAM memory chip.	[10]	CO5	L3
	PART C			
5 (a)	Explain 4-bit carry look-ahead adder.	[10]	CO3	L3
	OR			
6 (a)	Perform multiplication for +23 and -10 using Booth algorithm.	[5]	CO3	L3
(b)	Perform multiplication for +23 and -10 using Bit-pair recoding.	[5]	CO3	L3
	PART D			
7 (a)	Explain hardware arrangement for sequential multiplication	[10]	CO3	L2
	OR			
8 (a)	With a figure, explain circuit arrangement for binary division.	[10]	CO3	L2
	PART E			
9 (a)	Explain Synchronous DRAM with the aid of a block diagram.	[6]	CO2	L2
(b)	With a neat diagram, show connection between memory and processor.	[4]	CO2	L2
	OR			
10 (a)	Explain memory hierarchy with respect to speed, size and cost.	[5]	CO5	L2
(b)	Explain various types of ROM.	[5]	CO2	L2

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Internal Assesment Test 2 – Nov. 2017- Scheme and Solution

Sub:	COMPUTER ORGANIZATION					Sub Code:	15CS34	Branch:	CSE, ISE
Date:	07 / 11 / 2017	Duration:	90 mins	Max Marks:	50	Sem / Sec:	3(A,B,C)		OBE

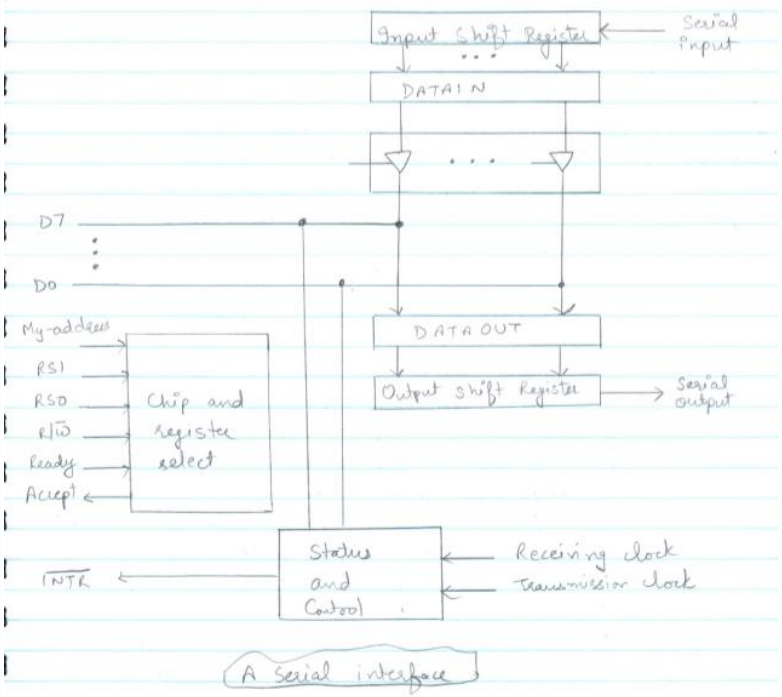
Answer **FIVE** FULL questions selecting AT LEAST ONE question **FROM EACH PART**

	MARKS	CO	RBT

PART A

1 (a) With a neat diagram, explain general 8-bit serial interface. [10] CO2 L2

(diagram -5 explanation-5)



- A serial port is used to connect the processor to I/O devices that require transmission of data one bit at a time.
- Serial port is capable of communicating in a bit-serial fashion on the device side and in a bit-parallel fashion on the bus side. This transformation between parallel and serial formats is achieved with shift registers.
- The input shift register accepts bit-serial input from the I/O device. When all 8 bits of data have been received, the contents of this shift register are loaded in parallel into DATAIN register.
- Similarly, output data in DATAOUT register are loaded into the output shift register, from which bits are shifted out and sent to I/O device serially.

SIN = 1 when data is present in DATAIN, as soon as processor reads it, SIN = 0.

SOUT = 1 when DATAOUT is available (empty) and ready to load. as soon as processor writes in DATAOUT, SOUT becomes 0.

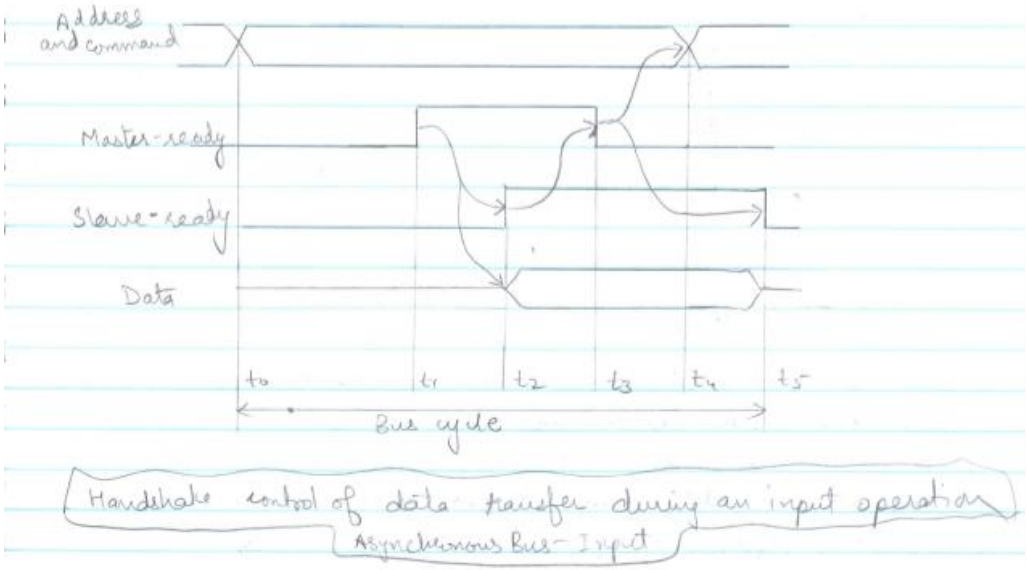
(shift register & DATAIN/DATAOUT)

- If double buffering is not imposed, after receiving one character from the serial line, the device cannot start receiving the next character until the processor reads the contents of DATAIN. Therefore, a pause would be needed between two characters to allow the processor to read the input data. With double buffer, the transfer of the second character can begin as soon as the first character is loaded from shift register into DATAIN register.
- It requires fewer wires, and thus is convenient for connecting devices that are physically far away from the computer.
- The speed of transmission (bit rate) depends on the nature of devices connected. To accommodate a range of devices, a serial interface must be able to use a range of clock speeds. Therfore, given circuit in diagram allows separate clock signals (receiving clock & transmission clock) to be used for input and output operations for increased flexibility.
- Other functionalities of lines / units is similar to ~~operate~~ that given in parallel port functioning (Refer page - 36).
- Eg of serial interface — UART (Universal Asynchronous Receiver Transmitter).

OR

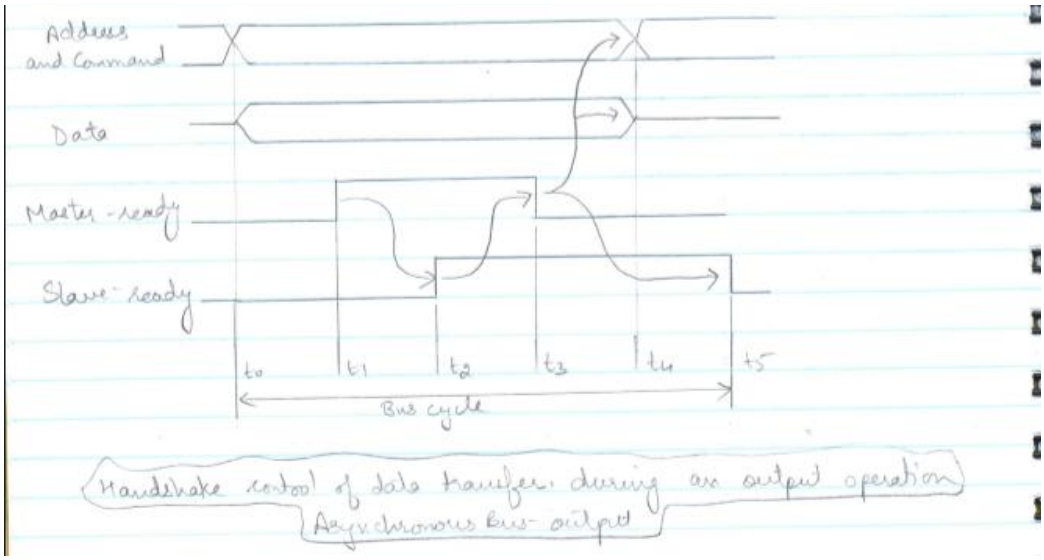
2 (a) With neat timing diagrams, explain asynchronous bus. [10] CO2 L2

(diagram-8 explanation-2)



Handshake control of data transfer during an input operation

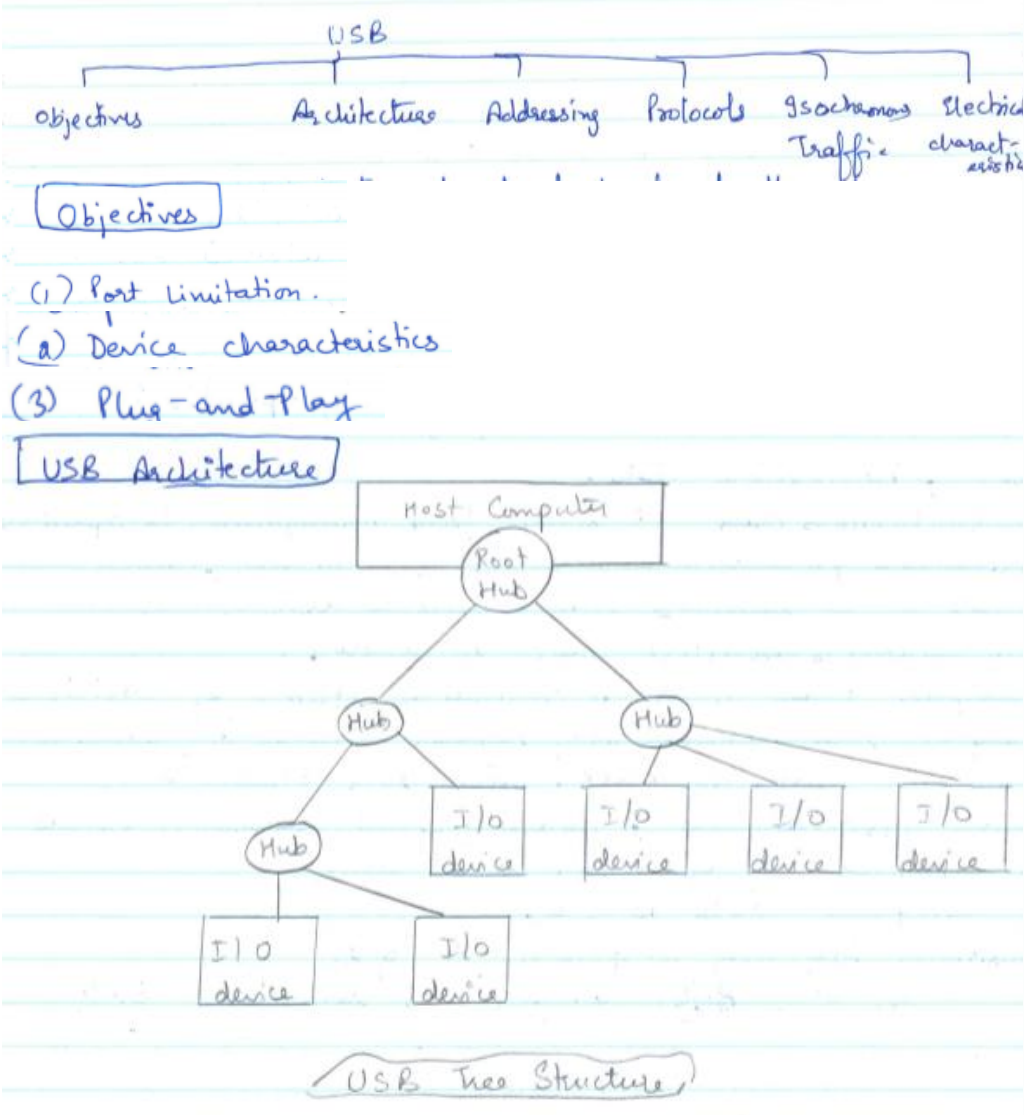
Asynchronous Bus - Input

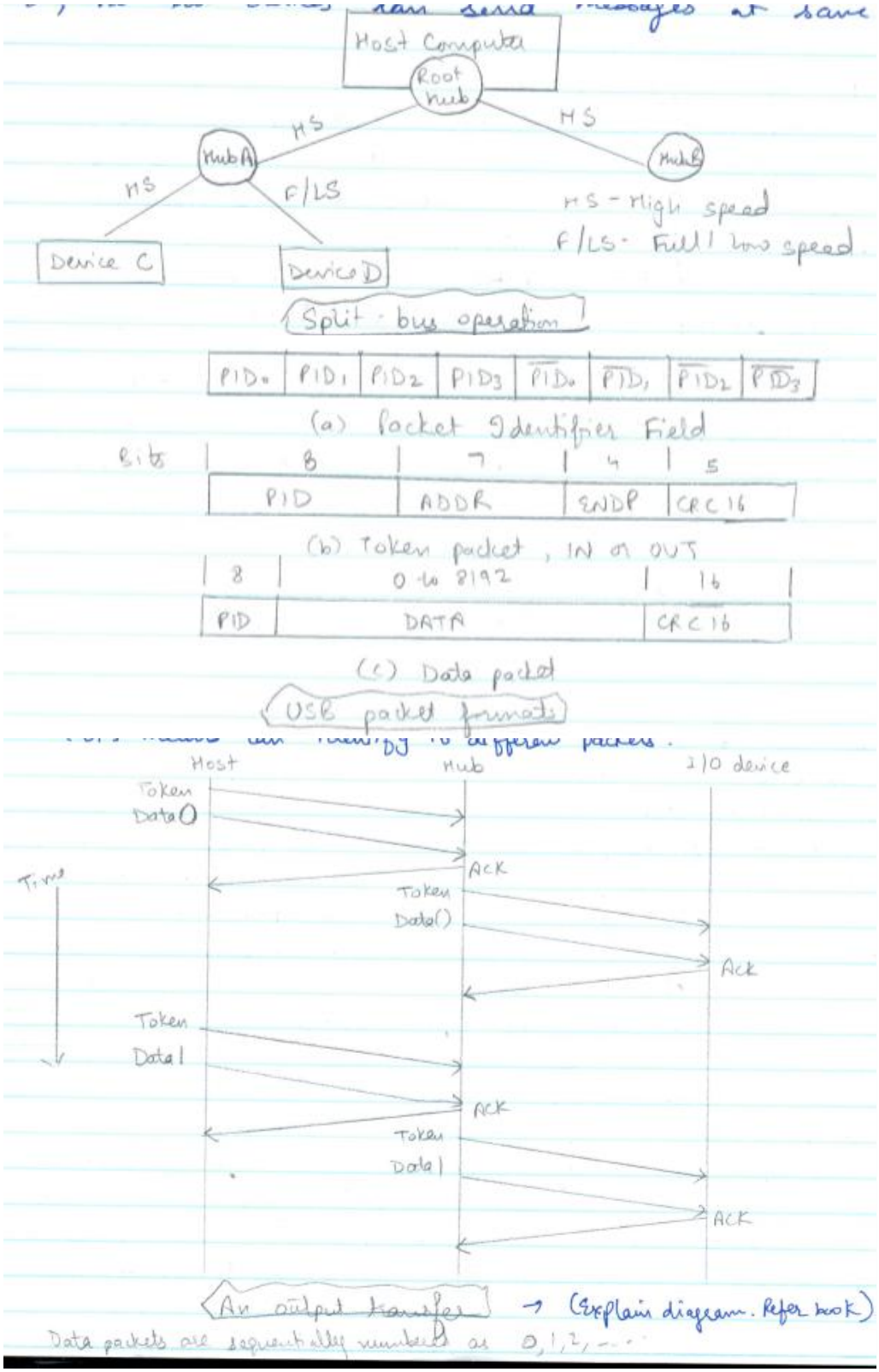


PART B

3 (a) Explain USB bus. [10] CO2 L2

(architecture-4, split bus- 2, packet format-2, output transfer-2)





OR

4 (a)	Consider sixteen words and each word having eight bits. Draw internal organization of the specified RAM memory chip. (diagram-7, explanation-3)	[10]	CO5	L3

- Memory-cells are organized in the form of array (Figure 8.2).
- Each cell is capable of storing 1-bit of information.
- Each row of cells forms a memory-word.
- All cells of a row are connected to a common line called as **Word-Line**.
- The cells in each column are connected to **Sense/Write** circuit by 2-bit-lines.
- The Sense/Write circuits are connected to data-input or output lines of the chip.
- During a write-operation, the sense/write circuit
  → receive input information &
  → store input info in the cells of the selected word.

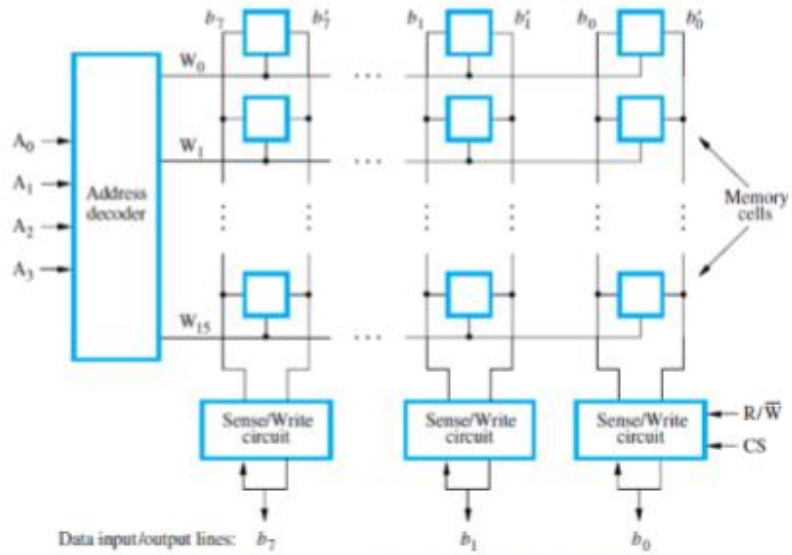


Figure 8.2 Organization of bit cells in a memory chip.

- The data-input and data-output of each Sense/Write circuit are connected to a single bidirectional data-line.
- Data-line can be connected to a data-bus of the computer.
- Following 2 control lines are also used:
  1) R/W' → Specifies the required operation.
  2) CS' → Chip Select input selects a given chip in the multi-chip memory-system.

PART C

5 (a) Explain 4-bit carry look-ahead adder. [10] CO3 L3
(diagram-4, derivation-6)

Carry-Lookahead adder (CLA)

Improving speed of addition will improve speed of all other arithmetic operations.

CLA improves speed by reducing carry propagation delay. It calculates carry signal in advance, based on input signals instead of waiting for them to ripple through the adders.

Recall the equations:

$$s_i = x_i \oplus y_i \oplus c_i$$
$$c_{i+1} = x_i y_i + x_i c_i + y_i c_i$$

Second equation can be written as:

$$c_{i+1} = x_i y_i + (x_i + y_i) c_i$$

We can write:

$$c_{i+1} = G_i + P_i c_i$$
$$where\ G_i = x_i y_i\ and\ P_i = x_i + y_i$$

- G_i is called generate function and P_i is called propagate function
- G_i and P_i are computed only from x_i and y_i and not c_i, thus they can be computed in one gate delay after X and Y are applied to the inputs of an n-bit adder.

$$c_{i+1} = G_i + P_i c_i$$
$$c_i = G_{i-1} + P_{i-1} c_{i-1}$$
$$\Rightarrow c_{i+1} = G_i + P_i (G_{i-1} + P_{i-1} c_{i-1})$$
$$continuing$$
$$\Rightarrow c_{i+1} = G_i + P_i (G_{i-1} + P_{i-1} (G_{i-2} + P_{i-2} c_{i-2}))$$
$$until$$
$$c_{i+1} = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + .. + P_i P_{i-1} .. P_1 G_0 + P_i P_{i-1} ... P_0 c_0$$

c_{i+1} is given in terms of c_0.

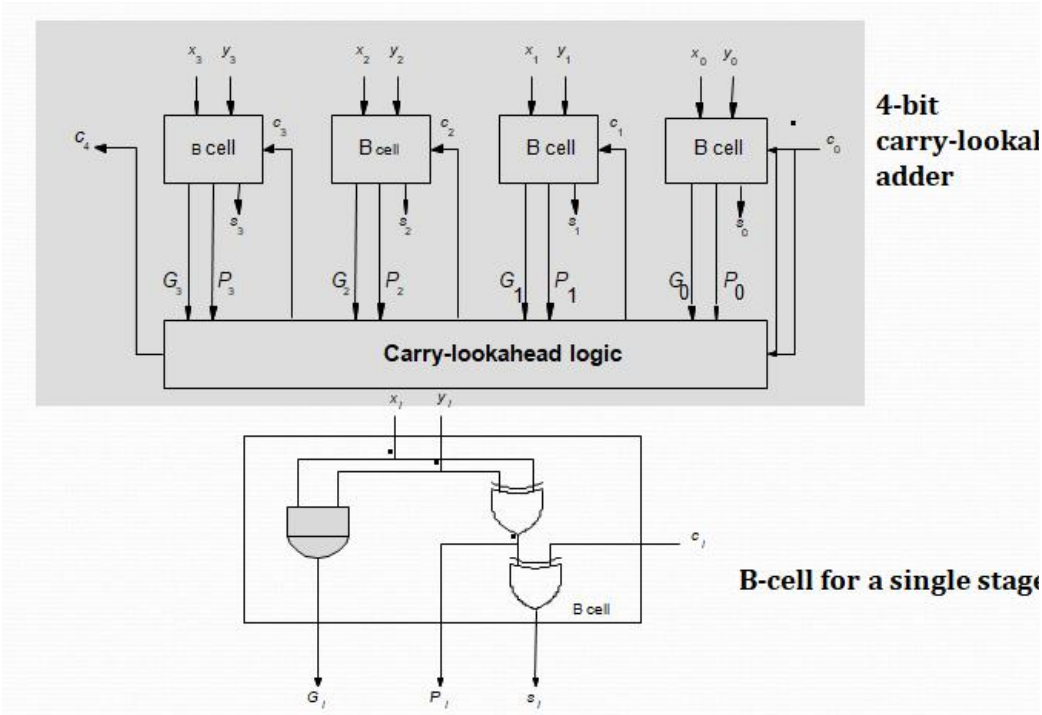
Consider 4-bit CLA:

$c_1 = G_0 + P_0 c_0$

$c_2 = G_1 + P_1 G_0 + P_1 P_0 c_0$

$c_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0$

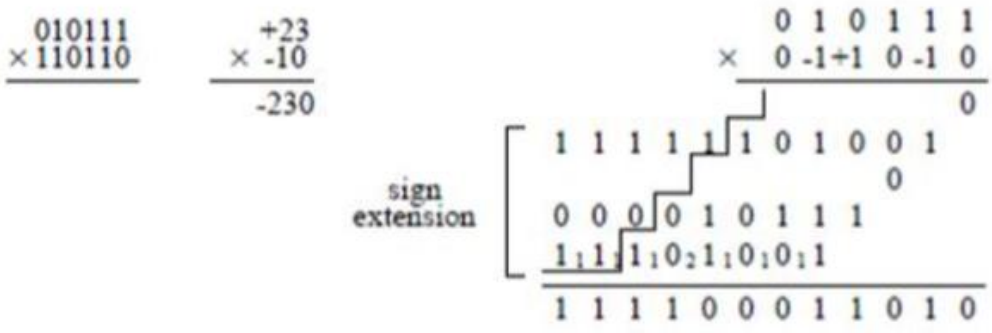
$c_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0$



OR

6 (a) Perform multiplication for +23 and -10 using Booth algorithm. [5] CO3 L3

010111 × 110110 = -230 (+23 × -10)

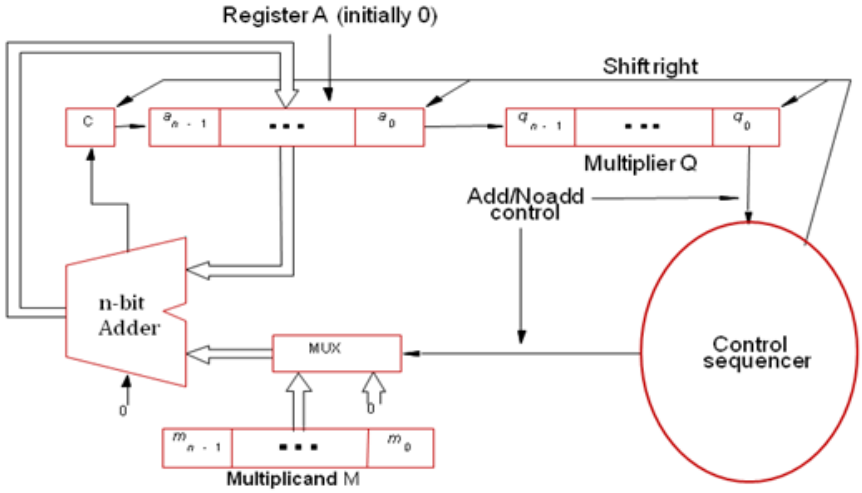


(b) Perform multiplication for +23 and -10 using Bit-pair recoding. [5] CO3 L3

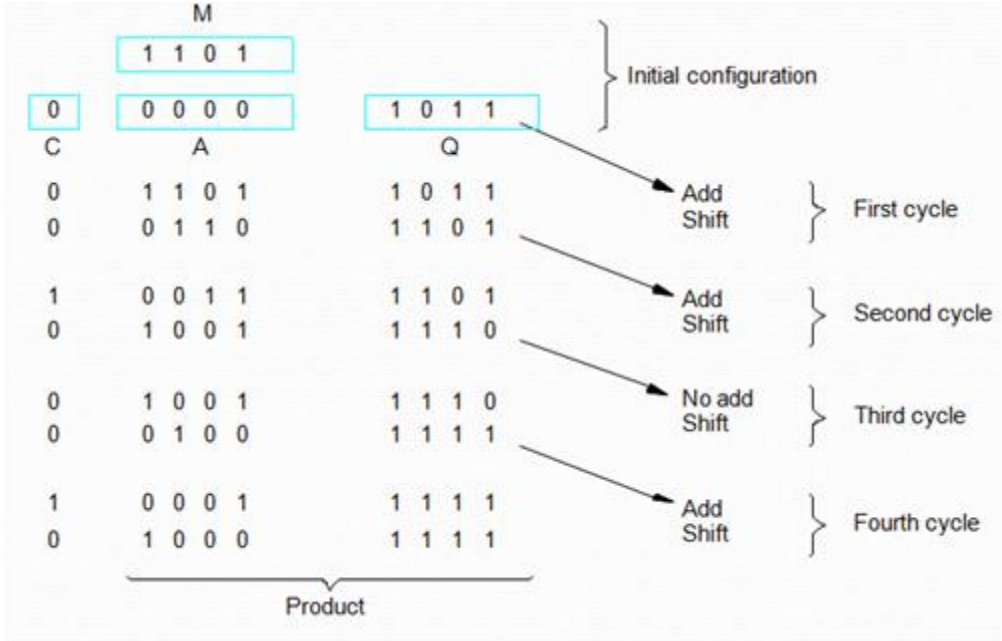
```
  010111                    0 1 0 1 1 1
× 110110                      -1  +2  -2
                  ---------------------
1 1 1 1 1 | 1 0 1 0 0 1 0
0 0 0 | 0 1 0 1 1 1 0
1 1 1 1 0 2 1 1 0 1 0 1
-------------------------
1 1 1 1 0 0 0 1 1 0 1 0
```

PART D

7 (a) Explain hardware arrangement for sequential multiplication (diagram-5, explanation-5) [10] CO3 L2



Sequential circuit binary multiplier/ register configuration for hardware arrangement for sequential multiplication



OR

8 (a) With a figure, explain circuit arrangement for binary division. (Diagram-5, any one algorithm-5) [10] CO3 L2

- An n-bit positive-divisor is loaded into register M.
  An n-bit positive-dividend is loaded into register Q at the start of the operation.
  Register A is set to 0 (Figure 9.21).
- After division operation, the n-bit quotient is in register Q, and
  the remainder is in register A.

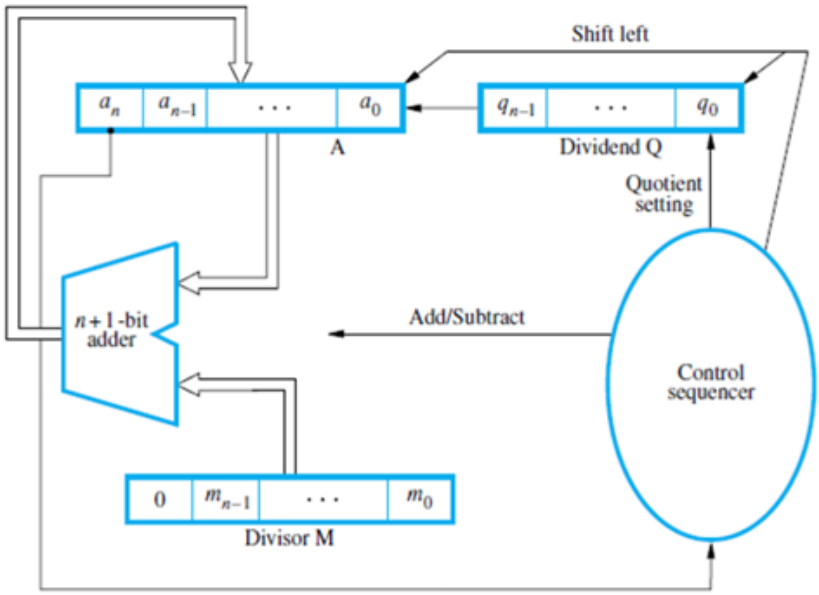


Figure 9.23 Circuit arrangement for binary division.

NON-RESTORING DIVISION

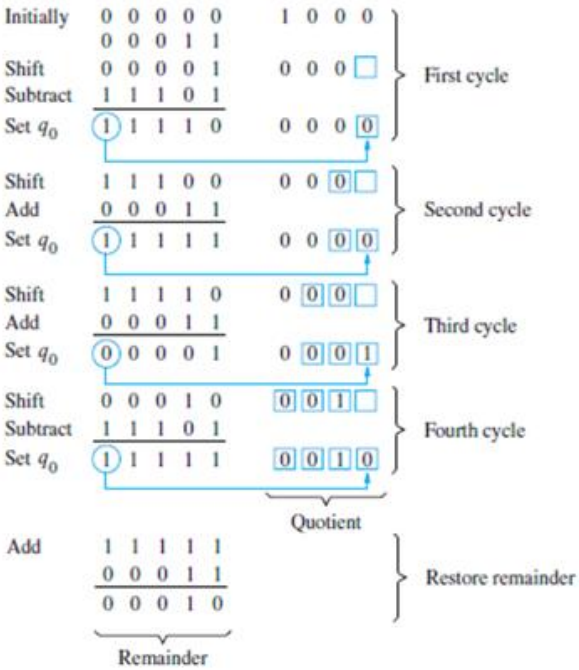
- Procedure:

  Step 1: Do the following n times

  i) If the sign of A is 0, shift A and Q left one bit position and subtract M from otherwise, shift A and Q left and add M to A (Figure 9.23).

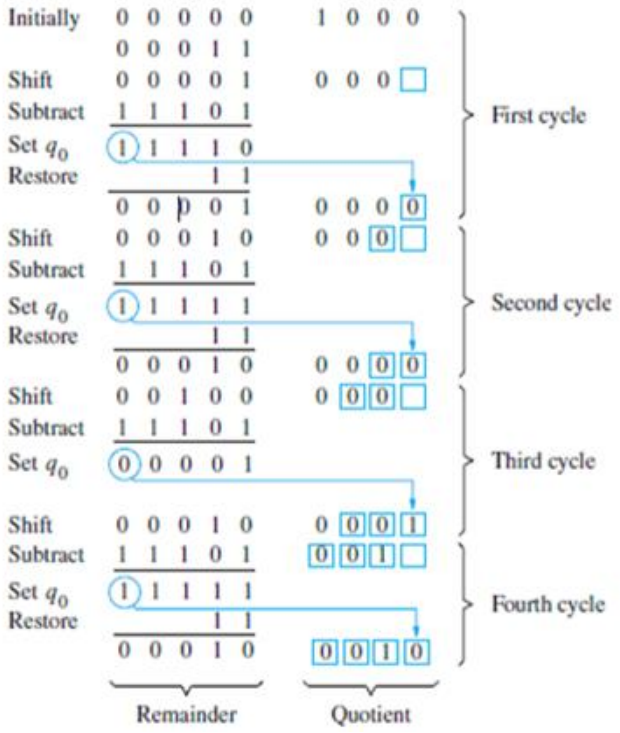
  ii) Now, if the sign of A is 0, set q_0 to 1; otherwise set q_0 to 0.

  Step 2: If the sign of A is 1, add M to A (restore).



RESTORING DIVISION

- Procedure: Do the following n times
  1) Shift A and Q left one binary position (Figure 9.22).
  2) Subtract M from A, and place the answer back in A
  3) If the sign of A is 1, set q_0 to 0 and add M back to A(restore A).
     If the sign of A is 0, set q_0 to 1 and no restoring done.



PART E

9 (a) Explain Synchronous DRAM with the aid of a block diagram. [6] CO2 L2

(diagram- 4, exaplanation-2)

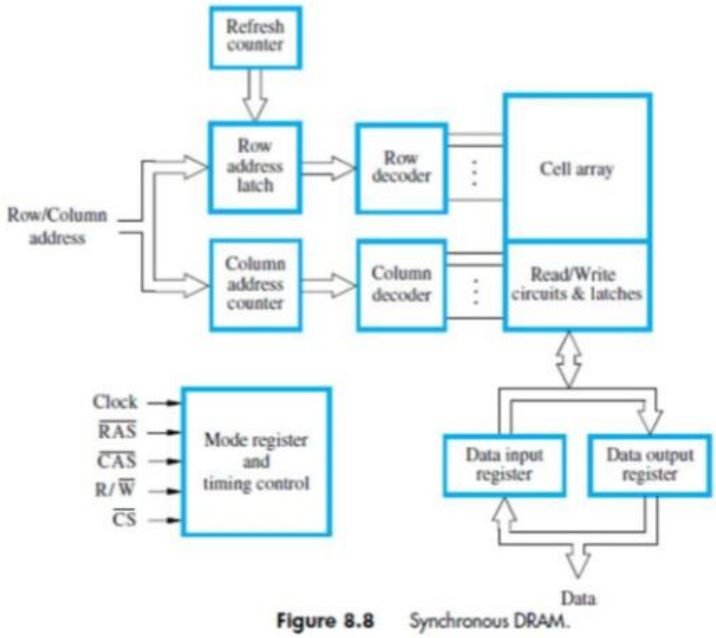
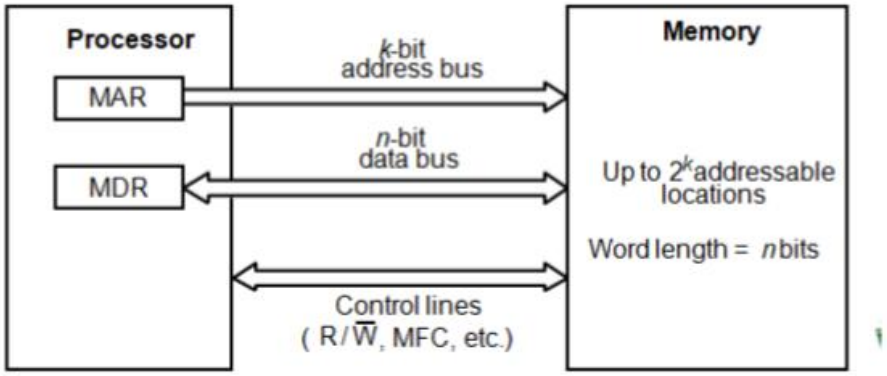


Figure 8.8 Synchronous DRAM.

- The operations are directly synchronized with clock signal
- The address and data connections are buffered by means of registers
- The output of each sense amplifier is connected to a latch.
- During a Read operation, the contents of the cells in a row are loaded onto the latches.
- During a refresh operation, the contents of the cells are refreshed without changing the contents of the latches. Refresh counter provides the address of the rows that are selected for refreshing. (generally, each row must be refreshed at least every 64 ms)
- Data held in latches that correspond to selected columns are transferred into data-output register. Thus, data becoming available on the data-output pins.
- SDRAMs have several different modes of operation, which can be selected by writing control information into a mode register.
- In SDRAMs, it is not necessary to provide externally generated pulses on CAS line to select successive columns, The necessary control signals are provided internally using a column counter and the clock signal.
- New data is placed on the data lines in each clock cycle.
- All actions are triggered during the rising edge of the clock.

(b)	With a neat diagram, show connection between memory and processor. (diagram-3, explanation-1)	[4]	CO2	L2



- If MAR is k-bits long then
  → memory may contain upto 2^K addressable-locations
- If MDR is n-bits long, then
  → n-bits of data are transferred between the memory and processor.
- The data-transfer takes place over the processor-bus (Figure 8.1).
- The processor-bus has
  1) Address-Line
  2) Data-line &
  3) Control-Line (R/W', MFC – Memory Function Completed).
- The Control-Line is used for coordinating data-transfer.
- The processor reads the data from the memory by
  → loading the address of the required memory-location into MAR and
  → setting the R/W' line to 1.
- The memory responds by
  → placing the data from the addressed-location onto the data-lines and
  → confirms this action by asserting MFC signal.
- Upon receipt of MFC signal, the processor loads the data from the data-lines into MDR.
- The processor writes the data into the memory-location by
  → loading the address of this location into MAR &
  → setting the R/W' line to 0.

OR

10 (a)	Explain memory hierarchy with respect to speed, size and cost. (diagram-4, explanation-1)	[5]	CO5	L2

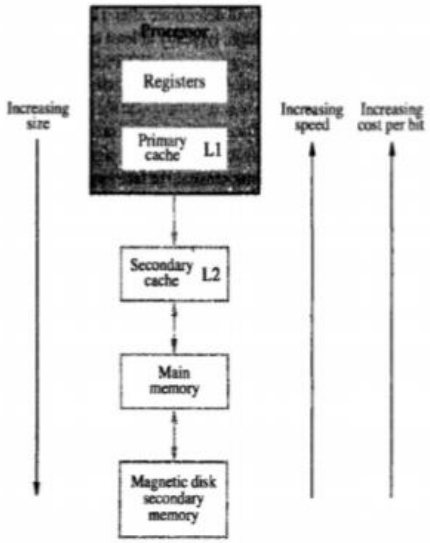


Figure 5.13 Memory hierarchy.

- Fastest access is to the data held in processor registers. Registers are at the top of the memory hierarchy.
- Relatively small amount of memory that can be implemented on the processor chip. This is processor cache. Usually implemented as SRAM.
- Two levels of cache.

Level 1 (L1) cache is on the processor chip. Level 2 (L2) cache is in between main memory and processor.

- Next level is main memory, implemented as DRAM (SIMMs,RIMM,DIMM). Much larger, but much slower than cache memory.
- Next level is magnetic disks. Huge amount of inexepensive storage.
- Speed of memory access is critical, the idea is to bring instructions and data that will be used in the near future as close to the processor as possible.

(b) Explain various types of ROM. [5] CO2 L2
(PROM-1, EPROM-1, EEPROM-1, Flash memory-2)

PROM(Programmable Read Only Memory)

- PROM allows the data to be loaded by the user.
- Programmability is achieved by inserting a 'fuse' at point P in a ROM cell.
- Before PROM is programmed, the memory contains all 0's.
- User can insert 1's at required location by burning-out fuse using high current-pulse.
- This process is irreversible.
- **Advantages:**
  1) It provides flexibility.
  2) It is faster.
  3) It is less expensive because they can be programmed directly by the user.

EPROM (Erasable Reprogrammable Read Only Memory)

- EPROM allows
  → stored data to be erased and
  → new data to be loaded.
- In cell, a connection to ground is always made at 'P' and a special transistor is used.
- The transistor has the ability to function as
  → a normal transistor or
  → a disabled transistor that is always turned 'off'.
- Transistor can be programmed to behave as a permanently open switch, by injecting charge into it.
- Erasure requires dissipating the charges trapped in the transistor of memory-cells.
  This can be done by exposing the chip to ultra-violet light.
- **Advantages:**
  1) It provides flexibility during the development-phase of digital-system.
  2) It is capable of retaining the stored information for a long time.
- **Disadvantages:**
  1) The chip must be physically removed from the circuit for reprogramming.
  2) The entire contents need to be erased by UV light.

A significant disadvantage of EPROMs is that a chip must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultraviolet light. It is possible to implement another version of erasable PROMs that can be both programmed and erased electrically. Such chips, called EEPROMs, do not have to be removed for erasure. Moreover, it is possible to erase the cell contents selectively. The only disadvantage of EEPROMs is that different voltages are needed for erasing, writing, and reading the stored data.

FLASH MEMORY

- Has similar approach to EEPROM.
- Read the contents of a single cell, but need to write the contents of an entire block of cells. Prior to writing, previous contents of the block are erased.
- Flash devices have greater density so have higher capacity and low storage cost per bit.
- Power consumption of flash memory is very low, hence, making it attractive for use in portable equipment that is battery-driven. E.g., MP3 music players, cell phones, digital cameras.
- Single flash chips are not sufficiently large, so larger memory modules are implemented using flash cards and flash drives.

1) Flash Cards

- One way of constructing larger module is to mount flash-chips on a small card.
- Such flash-card have standard interface.
- The card is simply plugged into a conveniently accessible slot.
- Memory-size of the card can be 8, 32 or 64MB.
- Eg: A minute of music can be stored in 1MB of memory. Hence 64MB flash cards can store an hour of music.

2) Flash Drives

- Larger flash memory can be developed by replacing the hard disk-drive.
- The flash drives are designed to fully emulate the hard disk.
- The flash drives are solid state electronic devices that have no movable parts.

Advantages:

1) They have shorter seek & access time which results in faster response.
2) They have low power consumption. .'. they are attractive for battery driven application.
3) They are insensitive to vibration.

Disadvantages:

1) The capacity of flash drive (<1GB) is less than hard disk (>1GB).
2) It leads to higher cost per bit.
3) Flash memory will weaken after it has been written a number of times (typically at least 1 million times).