ANALOG & DIGITAL ELECTRONICS

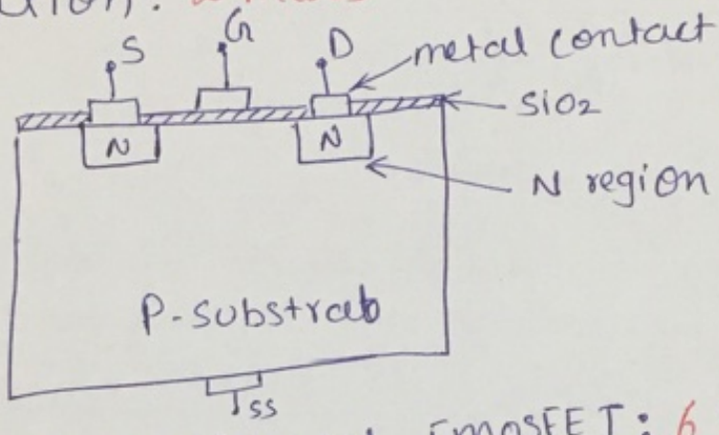
(15CS32)

Improvement Test - NOV. 2017

(Scheme & Solution)

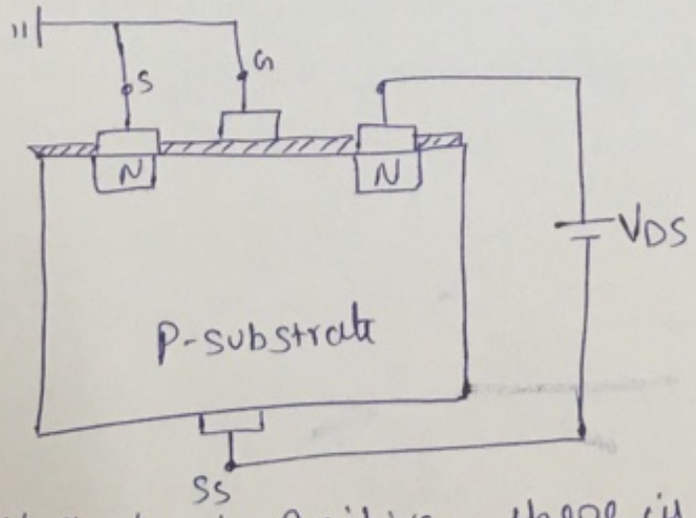
1. Explain the working of an N-channel EMOSFET with neat diagram. Explain with diagram output characteristics of the same. (10)

Sol Construction: 2 marks



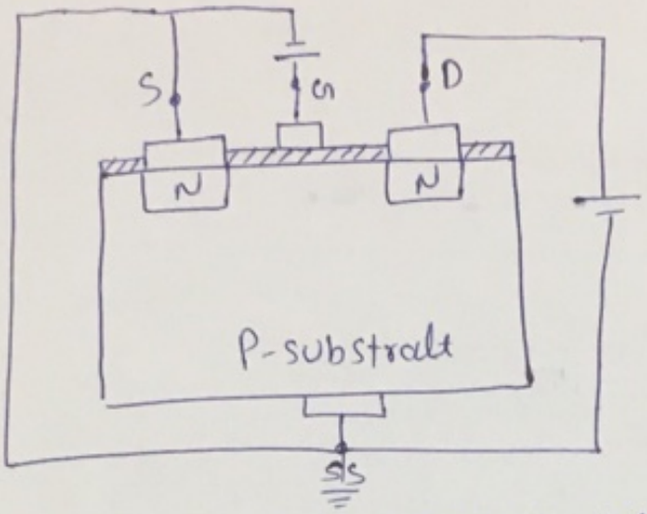
Working of N-channel EMOSFET: 6 marks

Case 1: $V_{GS}=0$, $V_{DS}>0V$



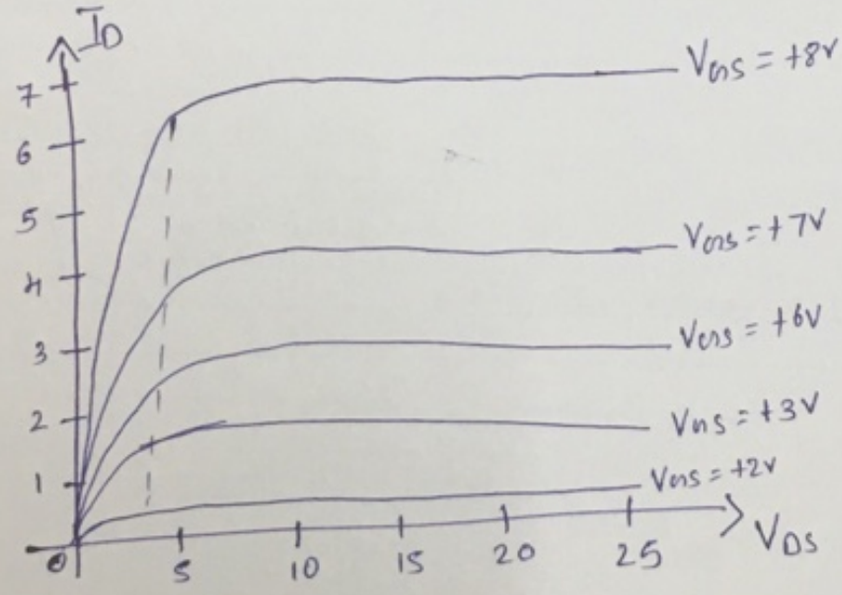
When $V_{GS}=0V$ & V_{DS} is Positive there is no Drain current, as there is no channel available for flow of Drain current. Hence E-MOSFET are also reffered to as OFF-MOSFETs as they do not conduct when $V_{GS}=0V$

Case 2: $V_{GS} > 0V$, $V_{DS} > 0V$



When a positive Gate-Source voltage (V_{GS}) is applied, electrons in the P-type substrate will accumulate near the surface of SiO_2 layer. As the value of V_{GS} is increased more & more electrons accumulate leading to an enhanced flow of Drain current.

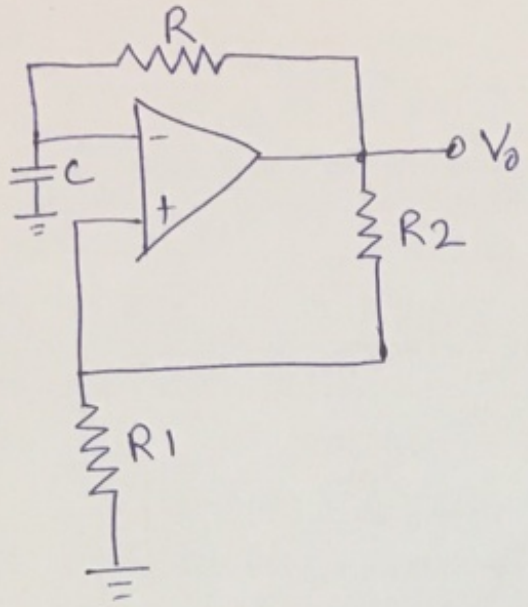
Output characteristics of N-channel EMOSFET: 3 marks



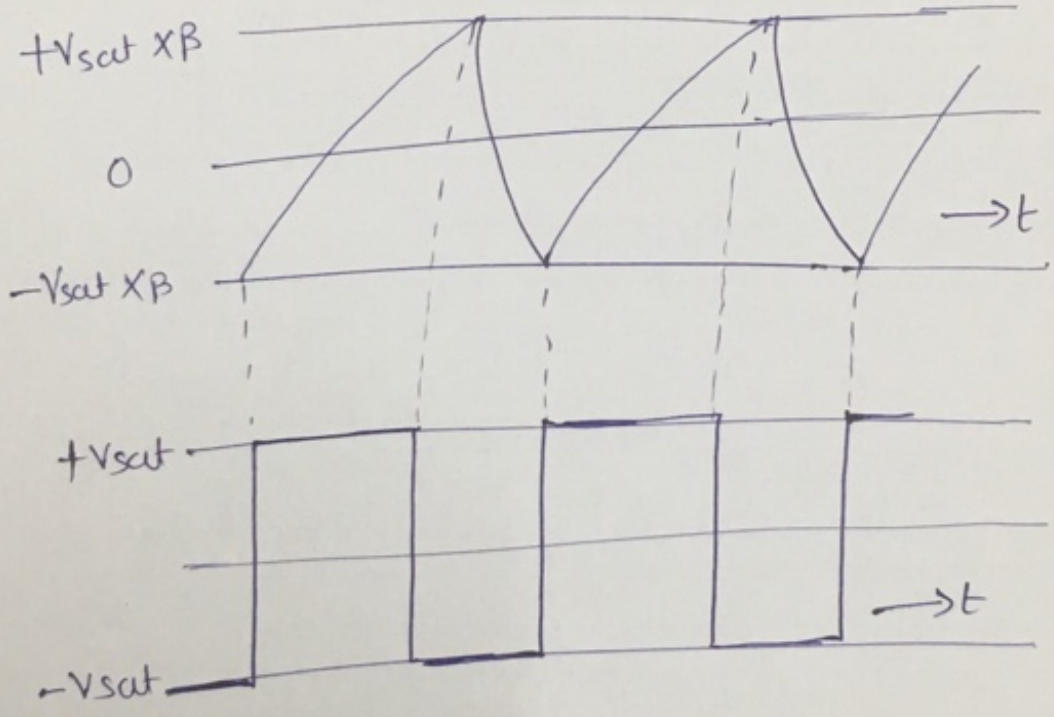
2. (a) Explain OP-amp relaxation oscillator with a neat diagram (5)

Sol: Relaxation oscillator produces a non-sinusoidal output whose time period is dependent on the charging time of the capacitor. Definition: 1 mark (2)

Circuit Diagram: 2 marks



·Waveform



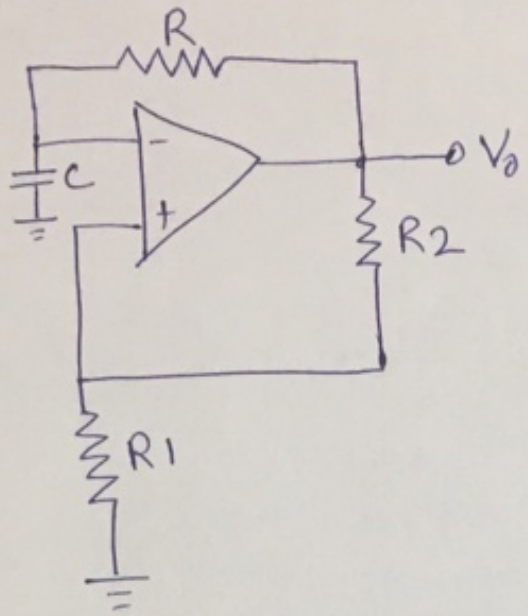
Explanation: 2 marks

The expression for time period of O/P waveform is given by

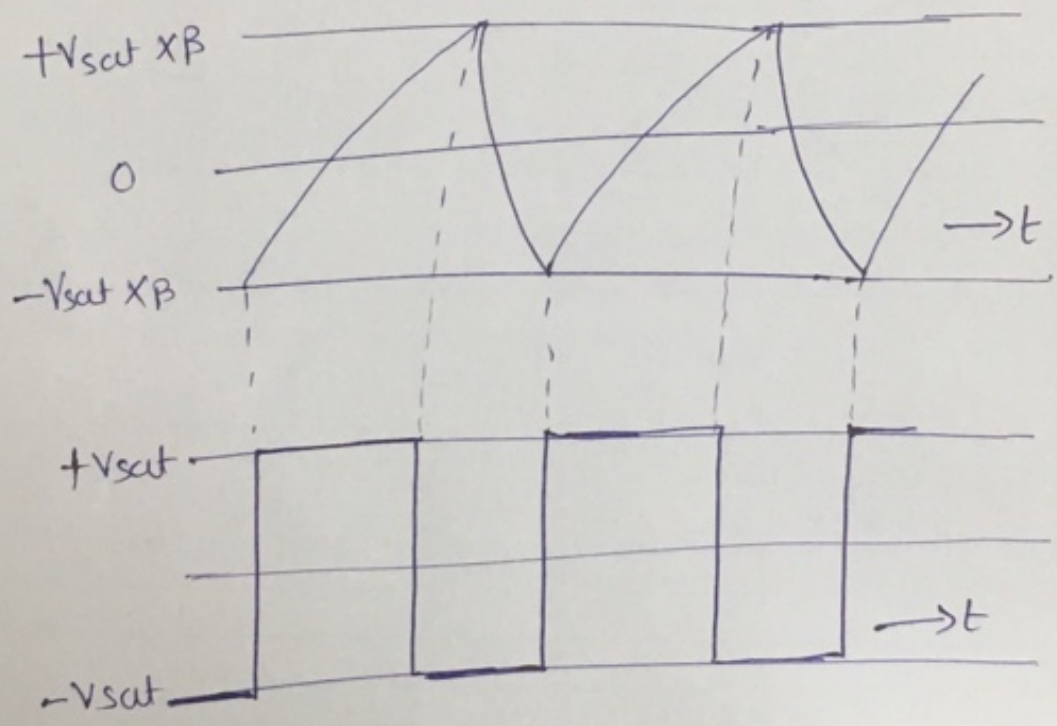
$$T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$$

where $\beta = \frac{R_1}{R_1+R_2}$

Circuit Diagram: 2 marks



Waveform



Explanation: 2 marks

The expression for time period of O/P waveform is given by

$$T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$$

where $\beta = \frac{R_1}{R_1+R_2}$

- The voltage at non inverting i/p of op amp is $+V_{sat} \times \frac{R_1}{(R_1+R_2)}$

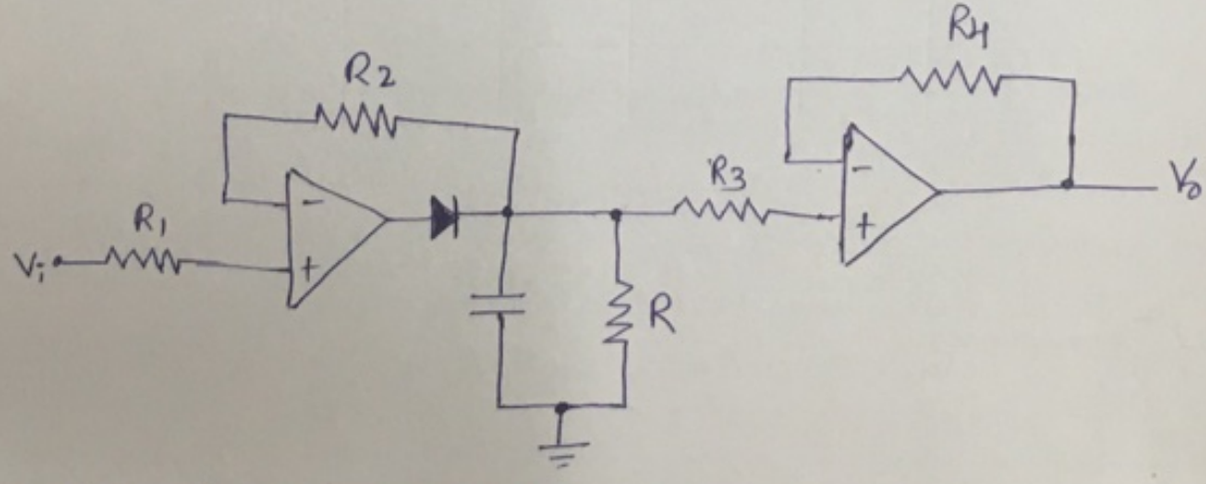
This forces the o/p to stay in positive saturation as the capacitor C is initially in fully discharged state.

- Capacitor C starts charging towards $+V_{sat}$ through R.
- The capacitor starts discharging after reaching zero, it begins to discharge towards $-V_{sat}$.

(b) Explain the working of peak detector circuit with a neat diagram. (5)

Sol: Peak detector circuit produces a voltage at the output equal to peak amplitude of the input signal. Defn: 1 mark

Circuit Diagram: 2 marks



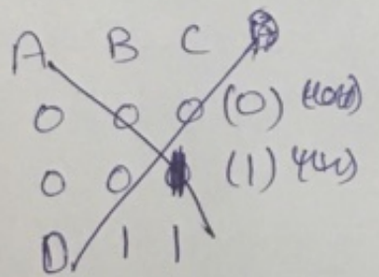
Explanation: 2 marks

- The clipper produces the positive half cycles.
- During this period, the Diode is forward biased.

- The capacitor rapidly charges to the positive peak from the o/p of opamp.
- As the i/p starts decreasing beyond the peak, the diode gets reverse biased, thus isolating the capacitor from the o/p of opamp.
- The capacitor now discharge only thro' the Resistor (R) connected across it.

3. Find Prime Implicants & Essential Prime implicants for the following function using Quine mc-clusky method & write the final SOP expression. The given function is: $\Sigma m(0,1,3,4,5,7)$ (10)

Sol:



Step 1

A	B	C	
0	0	0	(0) ✓
0	0	1	(1) ✓
1	0	0	(4) ✓
0	1	1	(3) ✓
1	0	1	(5) ✓
1	1	1	(7) ✓

Step 2

A	B	C	
0	0	-	(0,1) ✓
-	0	0	(0,4) ✓
0	-	1	(1,3) ✓
-	0	1	(1,5) ✓
1	0	-	(4,5) ✓
-	1	1	(3,7) ✓
1	-	1	(5,7) ✓

Step 3

A	B	C	
-	0	-	(0,1,4,5)
-	0	-	(0,4,1,5)
-	-	1	(1,3,5,7)
-	-	1	(1,5,3,7)

Steps → 6 marks

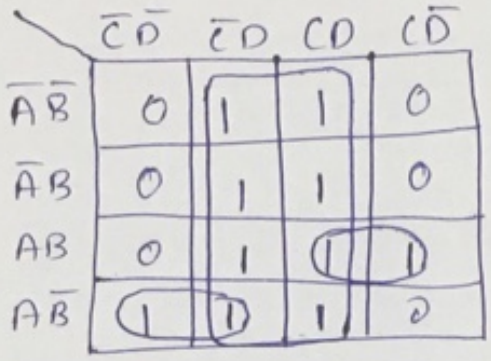
Prime implicants

$\bar{B}, C$ ← 2 marks

$\therefore Y = \bar{B} + C$ ← 2 marks

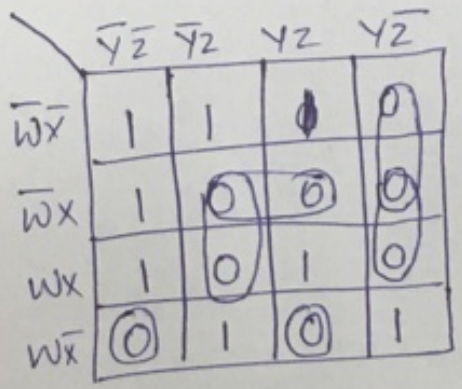
4. Simplify the following logic expression using K-map method and write the SOP/POS expression as applicable (OS+OS)

(a) $f(A,B,C,D) = \Sigma m(1,3,5,7,8,9,11,13,14,15)$ 5 marks



$$Y = D + ABC + A\bar{B}\bar{C}$$

(b) $f(W,X,Y,Z) = \Pi M(2,5,6,7,8,11,13,14)$ 5 marks.

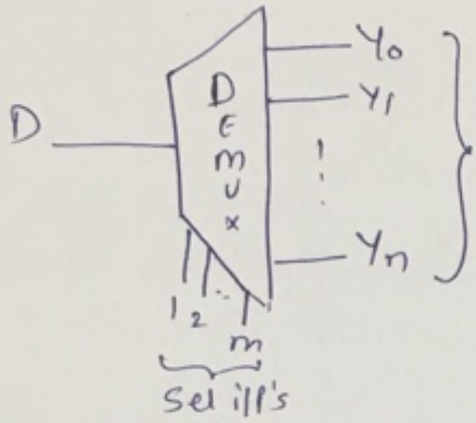


$$Y = (W+\bar{Y}+Z)(\bar{X}+\bar{Y}+Z)(W+\bar{X}+\bar{Z})(\bar{X}+Y+\bar{Z})(\bar{W}+X+Y+Z)$$
$$(\bar{W}+X+\bar{Y}+\bar{Z})$$

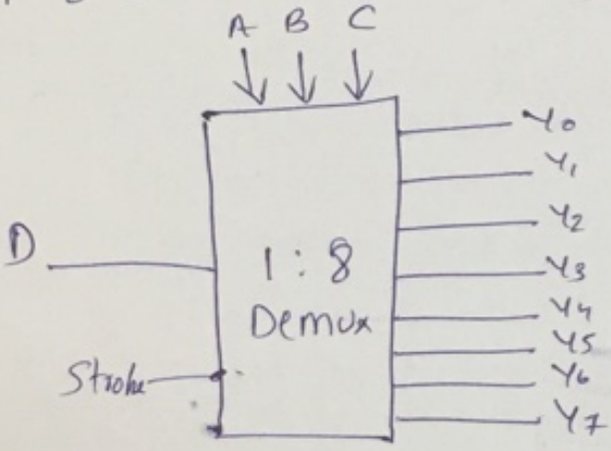
5. What is Demultiplexer? Explain with a neat diagram 1:8 Demux. (OS)

Sol. A Demux is a combinational logic circuit that has one input and n output.

for 2^n outputs there will be 'n' select inputs. (2 marks)



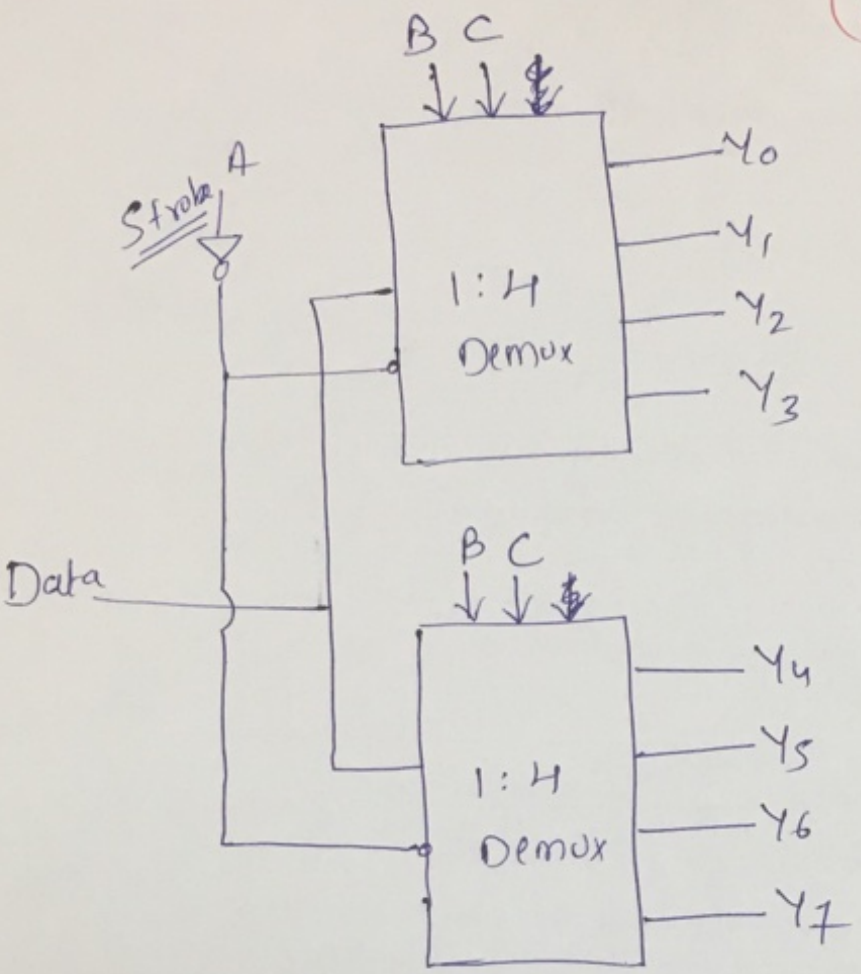
1:8 Demux (3 marks)



- The select inputs can range from 000 to 111.
- Based on the select input, the Data input will be transmitted to one of the o/p lines.
- A Strobe input is given to a Demux inorder to activate it.
  - if Strobe is low - Demux works
  - if Stobe is High - Demux is Deactivated.

(b) Design 1-to-8 Demux using 1-to-4 Demux (cos)

(5 marks)



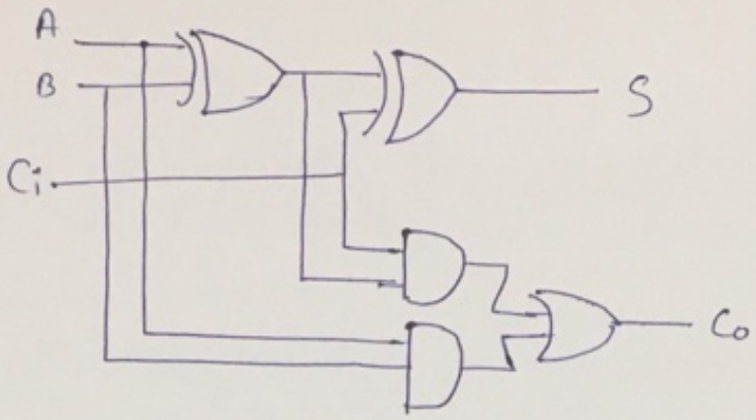
6. (a) write the Verilog Program for the given Boolean expression using dataflow modeling

(i) $Y = (A+B+C)(BC)$ (5 marks)

Sol

```
module ABC(A,B,C,Y);
  input A,B,C;
  Output Y;
  assign Y=((A|B|C)&(B&C));
  endmodule.
```

(ii) 5 marks



Sol:

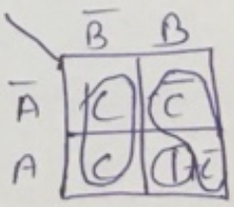
```
module ABCi(A,B,Ci,S,Co);
  input A,B,Ci;
  Output S,Co;
  assign S = (A^B)^Ci;
  assign Co =((A^B)&Ci)|(A&B);
  endmodule.
```

7(a) using EVM Technique Solve the Boolean function $F(A,B,C) = \Sigma m(1,2,5,6,7)$ & write the SOP Expression.

Sol

MEV ← 2 marks

A	B	C	Y	
0	0	0	0	→ C
0	0	1	1	
0	1	0	1	→ $\bar{C}$
0	1	1	0	
1	0	0	0	→ C
1	0	1	1	
1	1	0	1	→ 1
1	1	1	1	



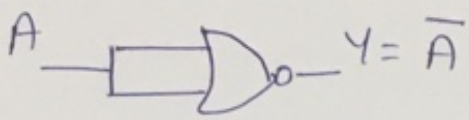
← 2 marks

$Y = \bar{B}C + B\bar{C} + A\bar{B}$ ← 1 mark

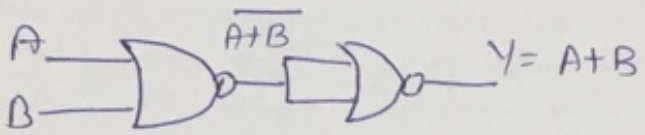
(b) Realize basic gates and NAND gate using NOR gates only (OS)

Sol:

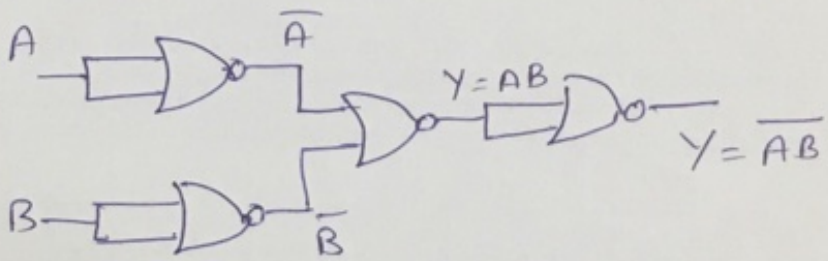
(a) NOT using NOR (1 mark)



(b) OR using NOR (1 mark)



(c) NAND using NOR (2 marks)



(d) AND using NOR (1 mark)