CMR INSTITUTE OF TECHNOLOGY

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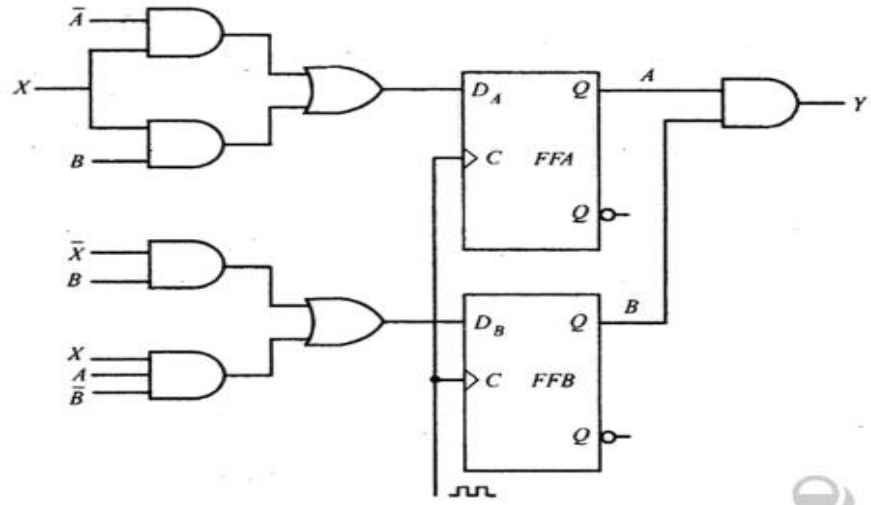
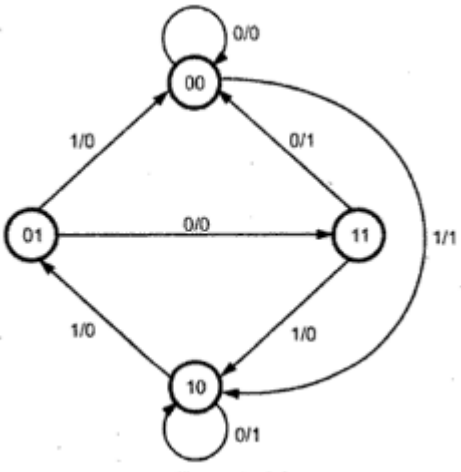
Internal Assesment Test - II

Sub:	DIGITAL SYSTEM DESIGN							Code:	15EE35
Date:	08/ 11/ 2017	Duration:	90 mins	Max Marks:	50	Sem:	3RD	Branch:	EEE

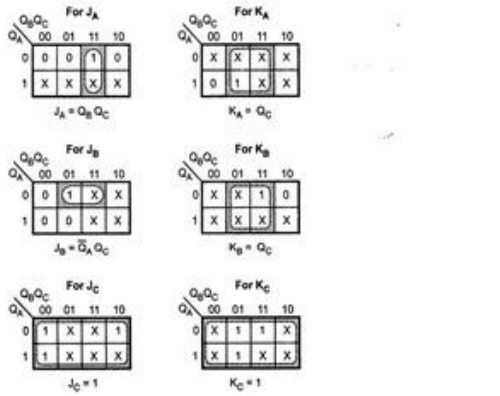
Answer Any FIVE FULL Questions

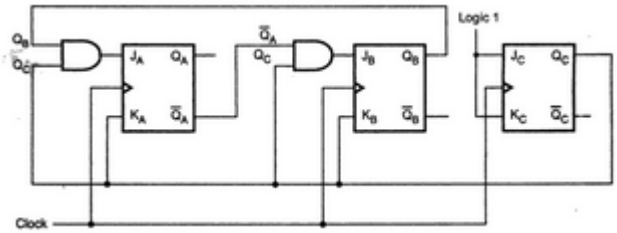
		Marks	OBE	
			CO	RBT
1	Design a synchronous Mod-6 counter using JK flip flop and represent the equations using sequential circuit.	10	CO3	L3
2	Convert JK flip flop in to D and T flip flop.Represnt symbolically.	10	CO3	L2
3	Explain the working of SR flip flop as switch debouncer and obtain the characteristic equations of SR flip flop.	10	CO3	L2
4	Explain the working of Master slave JK flip flop with the help of timing diagram, function table logic diagram and logic symbol.	10	CO3	L2
5	Write short notes on shift registers. Explain how a serial shift register can be transformed into a ring counter and Johnson counter	10	CO4	L2
6	Construct excitation table, transition table, state table and state diagram for the sequential circuit shown in fig 6  Fig 6	10	CO3	L3
7	Design a synchronous counter using JK flip flops to count sequence 0,1,2,4,5,6,0,1,2……..Draw state table and state diagram.	10	CO4	L3
8	Design a sequential circuit using T flip flop for the given state diagram shown in fig 8  Fig 8	10	CO4	L3

1.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Step 4 : K-map simplification for flip-flop inputs.





2.

IK Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in Table 5.10.

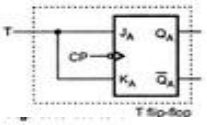
Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Table 5.10

K-map simplification

Fig. 5.44

Logic diagram



5.11.5 JK Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 5.11.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

K-map simplification

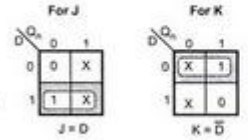


Fig. 5.46

Logic diagram

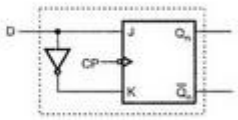
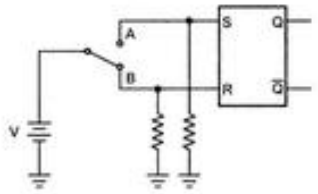


Fig. 5.47 JK to D

3.

One way to avoid key debounce problem is to use SR latch. The circuit used to avoid keybounce with SR latch is called a **switch debouncer**. The Fig. 5.7 shows the switch debouncer circuit and its waveforms. When key is at position A, the output of SR latch is logic 1, and when key is at position B, the output of SR latch is logic 0. It is important to note that, when key is in between A and B, SR inputs are 00 and hence output does not change, preventing debouncing of key output. In other words, we can say that the output does not change during transition period, eliminating key debounce.



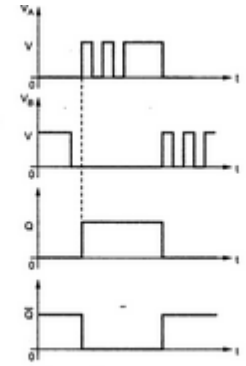
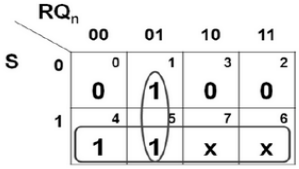


Fig. 5.7 (b) Waveforms of switch debouncer



$Q_{n+1} = S + R'Q_n$

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

4.

The master-slave combination can be constructed for any type of flip-flop. Fig. 5.29 shows one way to build a JK master-slave flip-flop. It consists of clocked JK flip-flop as a

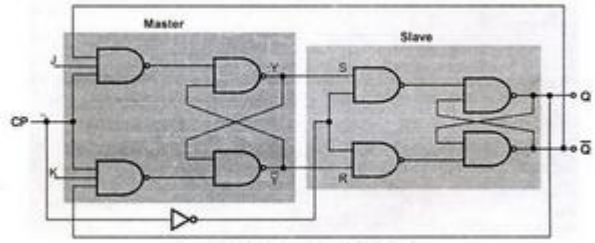


Fig. 5.29 Master-slave JK flip-flop

CP	Q_n	J	K	Y	Q_{n+1}
⌐	0	0	0	0	NC
⌐	0	0	0	NC	0
⌐	0	0	1	0	NC
⌐	0	0	1	NC	0
⌐	0	1	0	1	NC
⌐	0	1	0	NC	1
⌐	0	1	1	1	NC
⌐	0	1	1	NC	1
⌐	1	0	0	1	NC
⌐	1	0	0	NC	1
⌐	1	0	1	0	NC
⌐	1	0	1	NC	0
⌐	1	1	0	1	NC
⌐	1	1	0	NC	1
⌐	1	1	1	0	NC
⌐	1	1	1	NC	0

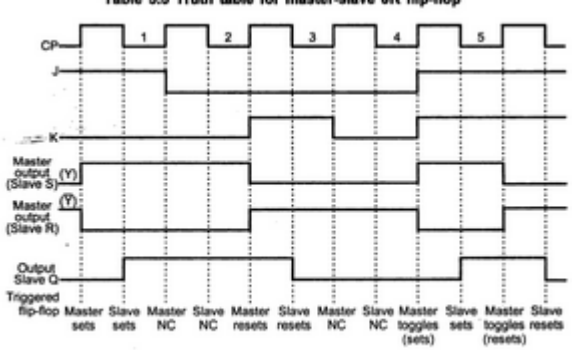
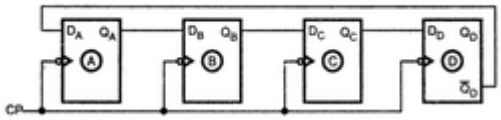


Fig. 5.30 Input and output waveforms of master-slave JK flip-flop

5.*Shift Registers* are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

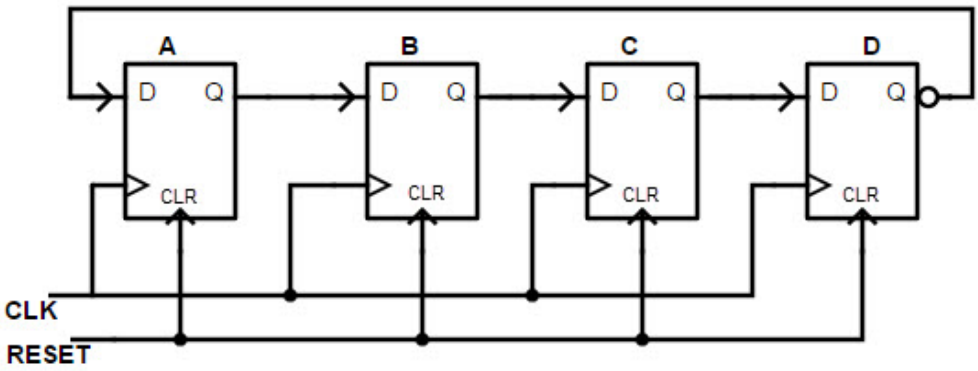
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

Johnson counter can be implemented with SR or JK flip-flops as well.



Clock Pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

The circuit diagram of the ring counter is shown below.



6.

Solution: Let us begin by writing the excitation expressions which are the flip-flop input expressions.

$$D_A = \bar{A}X + B\bar{X}$$

$$T_B = B\bar{X} + A\bar{B}X$$

The output expression is

$$Y = AB$$

This is also a Moore machine since $Y = f(Q)$.
Let us now evaluate the excitation and output expressions as shown in Fig. 7.23.

A	B	X	$\bar{A}$	$\bar{B}$	$\bar{X}$	$\bar{A}X$	$B\bar{X}$	$A\bar{B}$	$A\bar{B}X$	$B\bar{X}$	D_A	T_B	$Y = AB$
0	0	0	1	1	1	0	0	0	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	0	0	1	0	1	0
0	1	1	1	0	0	1	1	0	0	0	1	0	0
1	0	0	0	1	1	0	0	1	0	0	0	0	0
1	0	1	0	1	0	0	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0	0	0	1	0	1	1
1	1	1	0	0	0	0	1	0	0	0	1	0	1

Fig. 7.23 Evaluation of excitation and output expressions

We will now construct the excitation table as shown in Fig. 7.24.

Present state		*Excitation* D_A, T_B		*Output* Y	
		For input		*For input*	
A	B				
0	0	0, 0	1, 0	0	0
0	1	0, 1	1, 0	0	0
1	0	0, 0	0, 1	0	0
1	1	0, 1	1, 0	1	1

Fig. 7.24 Excitation table for Example 7.13

The transition table is constructed from the excitation table as shown in Fig. 7.25.

Present state		*Next state* A^+ B^+		*Output* Y	
		For input		*For input*	
A	B	$X = 0$	$X = 1$	$X = 0$	$X = 1$
0	0	0 0	1 0	0	0
0	1	0 0	1 1	0	0
1	0	0 0	0 1	0	0
1	1	0 0	1 1	1	1

Fig. 7.25 Transition table for Example 7.13

Consider present state $AB = 00$. The next state is $A^+ B^+$. Here, A^+ depends on the D input which is 0 for $X = 0$ and 1 for $X = 1$. Since $A^+ = D$ for a D flip flop, $A^+ = 0$ for $X = 0$ and $A^+ = 1$ for $X = 1$. Now B^+ depends on the T input which is 0 for both $X = 0$ and $X = 1$ and hence $B^+ = B$ (there is no toggle) for both $X = 0$ and $X = 1$. Thus, the next state for present state $AB = 00$ is $A^+ B^+ = 00$ for $X = 0$ and $A^+ B^+ = 10$ for $X = 1$.

The next state for all the other states are similarly filled in table shown in Fig. 7.25.

Let us label the states as $00 = a$, $01 = b$, $10 = c$ and $11 = d$.

By substituting these symbols for the states in the transition table, we can write the state table as shown in Fig. 7.26.

Present state	*Next state*		*Output* Y	
	For input		*For input*	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	c	0	0
b	a	d	0	0
c	a	b	0	0
d	a	d	1	1

Fig. 7.26 State table for Example 7.13

7.

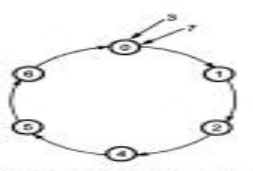


Fig. 6.5.41 (a) State diagram

Present State			Next State			Flip-flop inputs					
A	B	C	A^+	B^+	C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

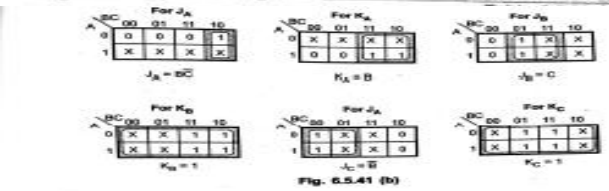


Fig. 6.5.41 (b)

Logic diagram

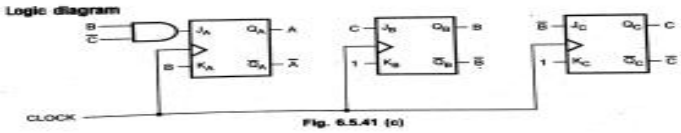


Fig. 6.5.41 (c)

8.

Present state		Input	Next state		Flip-flop inputs		Output
A	B	X	A	B	T_A	T_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0

Table 8.5 Circuit excitation table

The first row of circuit excitation table shows that there is no change in the state for both flip-flops. The transition from 0 → 0 for T flip-flop requires input T to be at logic 0. The second row shows that flip-flop A has transition 0 → 1. It requires the input T_A to be at logic 1. Similarly, we can find inputs for each flip-flop for each row in the table by referring present state, next state and excitation table.

Let us use K-map simplification to determine the flip-flop input functions and circuit output functions.

K-map simplification

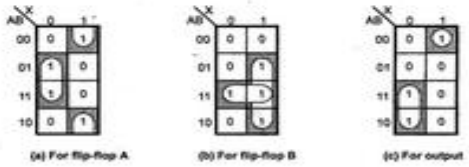


Fig. 8.17

Therefore, input function for $T_A = B\overline{X} + \overline{B}X$,

$T_B = AB + BX + AX$, and

Circuit output function $= A\overline{X} + \overline{A}\,\overline{B}X$