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Internal Assessment Test 1 – Sept. 2017

Sub: DSP Algorithm and Architecture Sub Code: 10TE74/10EC751 Branch: TCE/ECE

Date: 21/09/2017 Duration: 90 mins Max Marks: 50 Sem / Sec: 7/A,B,C,D OBE

Answer any FIVE FULL Questions

		MARKS	CO	RBT
1 (a)	An analog signal is sampled at the rate of 8khz. If 512 samples of this signal are used to compute DFT X(k). Calculate the analog and digital frequency spacing between adjacent X(k) elements. Also, calculate analog and digital frequencies corresponding to k=64.	[04]	CO1	L3
(b)	With a neat diagram explain the scheme of a DSP system.	[06]	CO1	L1
2 (a)	Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagrams.	[06]	CO1	L1
(b)	Let $x(n)$=[0,3,6,9,12] be interpolated with L=3. If the filter coefficients of the filters are $b_k = [1/3, 2/3, 1, 2/3, 1/3]$, Determine the interpolated sequence.	[04]	CO1	L3
3 (a)	For the FIR filter $y(n) = (1/3)[x(n) + x(n-1) + x(n-2)]$. Determine i) System Function ii) Magnitude and phase function iii) impulse response iv) group Delay.	[05]	CO1	L3
(b)	Explain the purpose of program sequencer with block diagram.	[05]	CO2	L1
4 (a)	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier.	[07]	CO1	L1
(b)	Compute the sequence in which the input data should be ordered for a 16 point DIT FFT using bit reversed addressing mode.	[03]	CO2	L3
5(a)	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram.	[6]	CO2	L1
(b)	Draw the schematic diagram of the saturation logic and explain the same	[4]	CO2	L1
6(a)	Explain the pointer updating algorithm for circular addressing mode.	[06]	CO2	L1
(b)	Calculate the memory addresses of the operands in each of the following cases of indirect addressing modes? In each case, what will be the content of the *addreg* after the memory access? Assume that the initial contents of the *addreg* and the *offsetreg* are 0200h and 0010h, respectively. i) ADD **addreg* ii).ADD *+*addreg iii)*ADD *offsetreg+,*addreg* iv) ADD **addreg,offsetreg-*	[04]	CO2	L3

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Internal Assessment Test 1 Key answers– Sept. 2017

Sub: DSP Algorithm and Architecture Sub Code: 10TE74/10EC751 Branch: TCE/ECE

CI: Prof. Pappa M, Mrs. Rashmi K V, Mrs. Reshma P G

1 (a) An analog signal is sampled at the rate of 8khz. If 512 samples of this signal are used to compute DFT X(k). Calculate the analog and digital frequency spacing between adjacent X(k) elements. Also, calculate analog and digital frequencies corresponding to k=64.

Ans: Frequency Spacing $\Delta f = \frac{F_s}{N} = \frac{8khz}{512} = 15.625$ [2M]

Analog Frequency Corresponding to$k = 64$ is $\Delta f \times k = 15.625 * 64 = 1000HZ$ [2M]

(b) With a neat diagram explain the scheme of a DSP system.

Ans: DSP is a technique of performing the mathematical operations on the signals in digital domain. As real time signals are analog in nature we need first convert the analog signal to digital, then we have to process the signal in digital domain and again converting back to analog domain. Thus ADC is required at the input side whereas a DAC is required at the output end. A typical DSP system is as shown in figure 1.1

Fig 1.1: A Typical DSP System

A computer or a processor is used for digital signal processing. Antialiasing filter is a LPF which passes signal with frequency less than or equal to half the sampling frequency in order to avoid Aliasing effect. Similarly at the other end, reconstruction filter is used to reconstruct the samples from the staircase output of the DAC (Figure 1.2). [3 M]

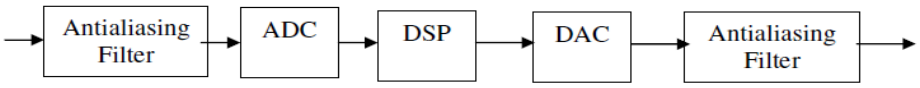


Fig 1.2 The Block Diagram of a DSP System

[3M]

Signals that occur in a typical DSP are as shown in figure 1.3.

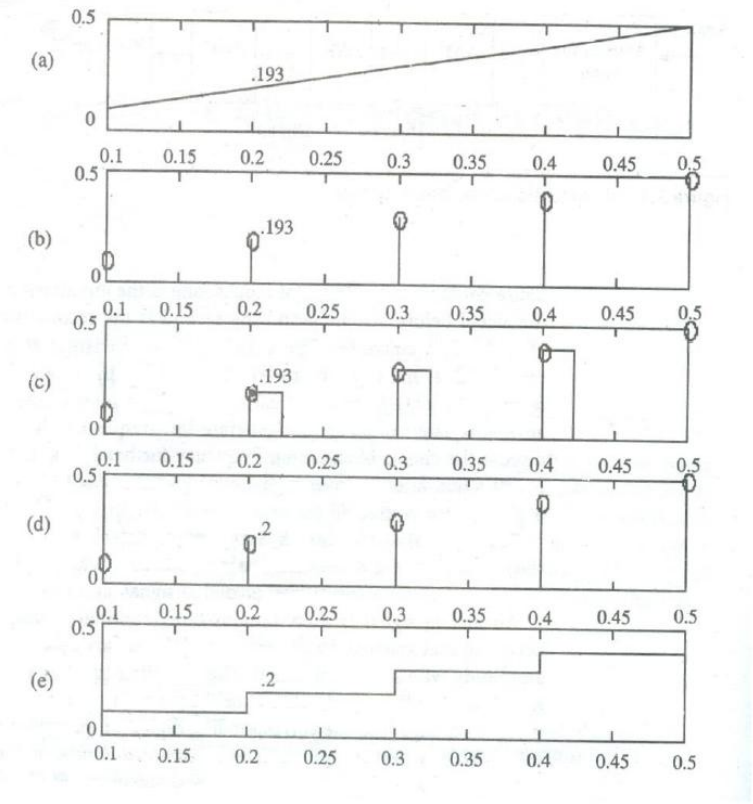


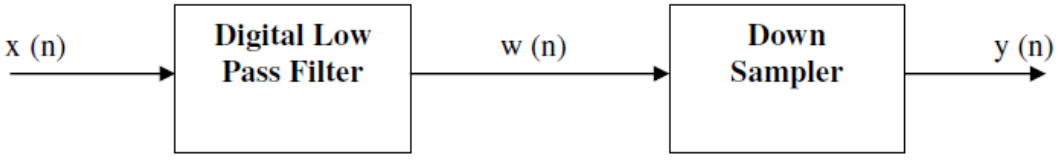
Fig 1.3: (a) Continuous time signal (b) Sampled Signal (c) Sampled Data Signal (d) Quantized Signal (e) DAC Output

2 (a) Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagrams.

Ans: Decimation is a process of dropping the samples without violating sampling theorem. The factor by which the signal is decimated is called as decimation factor and it is denoted by M. It is given by,

$$y(m) = w(mM) = \sum_{k=-\infty}^{\infty} b_k x(mM-k)$$

where $w(n) = \sum_{k=-\infty}^{\infty} b_k x(n-k)$ [2 M]



[1M]

Interpolation is a process of increasing the sampling rate by inserting new samples in between. The input output relation for the interpolation, where the sampling rate is increased by a factor L, is given as, $y(m) = \sum_{k=-\infty}^{\infty} b_k w(m-k)$ where $w(n) = \begin{cases} x\left(\frac{m}{L}\right), m = 0, \pm 1L, \pm 2L, \pm 3L \ldots\ldots \\ 0, otherwise \end{cases}$ [2M]

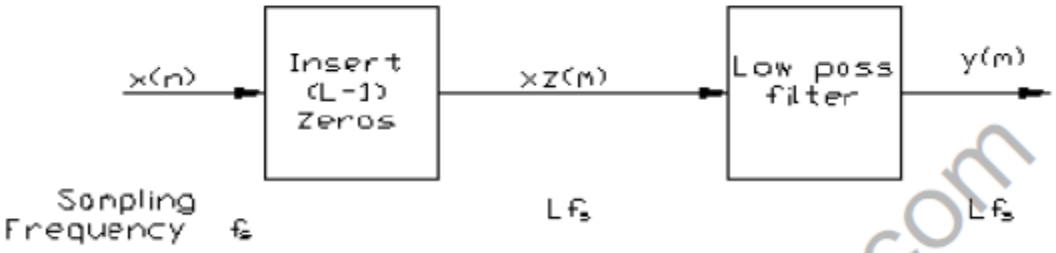
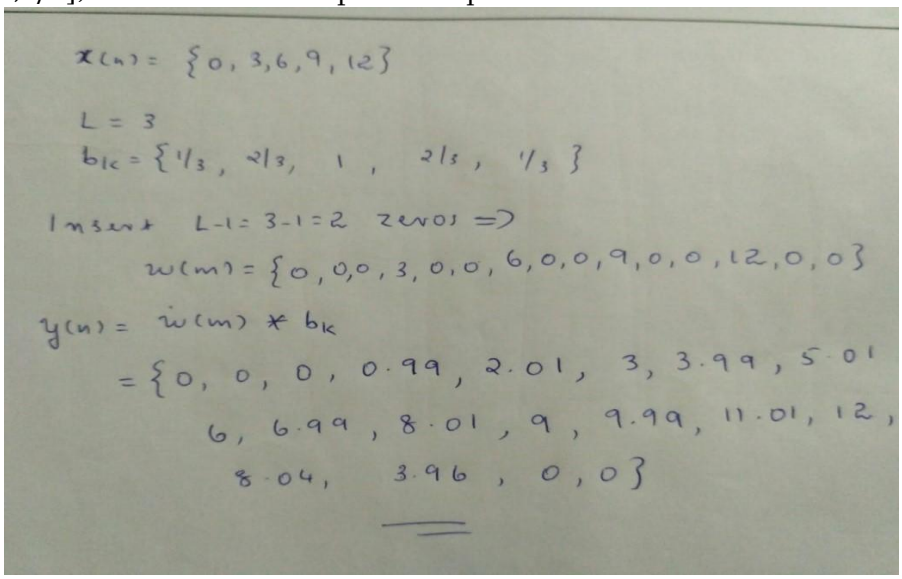


Fig 1.13 Interpolation Process

[1M]

(b) Let $x(n)$=[0,3,6,9,12] be interpolated with L=3. If the filter coefficients of the filters are $b_k = [1/3, 2/3, 1, 2/3, 1/3]$, Determine the interpolated sequence.

Ans:



[2M for convolution]
[2M for y(n)]

3 (a) For the FIR filter $y(n) = (1/3)[x(n) + x(n-1) + x(n-2)]$. Determine i) System Function ii) Magnitude and phase function iii) impulse response iv) group Delay.

Ans:

(a) system function $H(z) = \frac{Y(z)}{X(z)}$

$$y(n) = \frac{1}{3}[x(n) + x(n-1) + x(n-2)].$$

Taking z-transform,

$$Y(z) = \frac{1}{3}[X(z) + z^{-1}X(z) + z^{-2}X(z)]$$

$$\therefore Y(z) = \frac{1}{3}X(z)[1 + z^{-1} + z^{-2}]$$

$$\therefore \boxed{H(z) = \frac{Y(z)}{X(z)} = \frac{1 + z^{-1} + z^{-2}}{3}}$$

(i) Magnitude response function

put $z = e^{j\Omega}$ in $H(z)$

$$\therefore H(z) = \frac{1 + z^{-1} + z^{-2}}{3}$$

$$H(e^{j\Omega}) = \frac{1 + e^{-j\Omega} + e^{-j2\Omega}}{3}$$

$$= \frac{1}{3}\left[\sum_{n=0}^{2} (e^{-j\Omega})^n\right] \longrightarrow (1)$$

using finite geometric series formula

$$\sum_{n=0}^{N-1} a^n = \frac{1-a^N}{1-a}$$ in eqn (1),

$$H(e^{j\Omega}) = \left[\frac{1 - e^{-j3\Omega}}{1 - e^{-j\Omega}}\right] \frac{1}{3}.$$

$$= \frac{1}{3}\left[\frac{e^{j\frac{3\Omega}{2}} e^{-j\frac{3\Omega}{2}} - e^{-j\frac{3\Omega}{2}} e^{-j\frac{3\Omega}{2}}}{e^{j\frac{\Omega}{2}} e^{-j\frac{\Omega}{2}} - e^{-j\frac{\Omega}{2}} e^{-j\frac{\Omega}{2}}}\right]$$

$$= \frac{1}{3}\left[\frac{e^{-j\frac{3\Omega}{2}}\left[e^{j\frac{3\Omega}{2}} - e^{-j\frac{3\Omega}{2}}\right]}{e^{-j\frac{\Omega}{2}}\left[e^{j\frac{\Omega}{2}} - e^{-j\frac{\Omega}{2}}\right]}\right]$$

$$= \frac{1}{3} e^{-j\Omega}\left[\frac{\sin\left(\frac{3\Omega}{2}\right)}{\sin\left(\frac{\Omega}{2}\right)}\right]$$

$$\therefore |H(e^{j\Omega})| = \frac{1}{3}|e^{-j\Omega}| \left|\frac{\sin\left(\frac{3\Omega}{2}\right)}{\sin\left(\frac{\Omega}{2}\right)}\right|$$

$$\boxed{|H(e^{j\Omega})| = \frac{1}{3}\left|\frac{\sin\left(\frac{3\Omega}{2}\right)}{\sin\left(\frac{\Omega}{2}\right)}\right|}$$

(c) Phase response

$$\angle H(e^{j\omega}) = \angle \frac{1}{3} + \angle e^{-j\omega} + \angle \sin(\omega)$$

$$= 0 + (-\omega) + 0$$

$$\therefore \angle H(e^{j\omega}) = -\omega$$

It is a linear response.

(d) Impulse response $h(n)$ is obtained by taking inverse z transform of $H(z)$

$$\therefore H(z) = \frac{1}{3} + \frac{1}{3}z^{-1} + \frac{1}{3}z^{-2}$$

$$\therefore h(n) = \frac{1}{3}\delta(n) + \frac{1}{3}\delta(n-1) + \frac{1}{3}\delta(n-2)$$

$$\therefore h(n) = \left\{\frac{1}{3}, \frac{1}{3}, \frac{1}{3}\right\}.$$

(f) group delay is obtained by differentiating negating the Phase response.

$$\text{Group delay} = -\frac{d}{d\omega}\left(\angle H(e^{j\omega})\right)$$

$$= -\frac{d}{d\omega}(-\omega) = +1$$

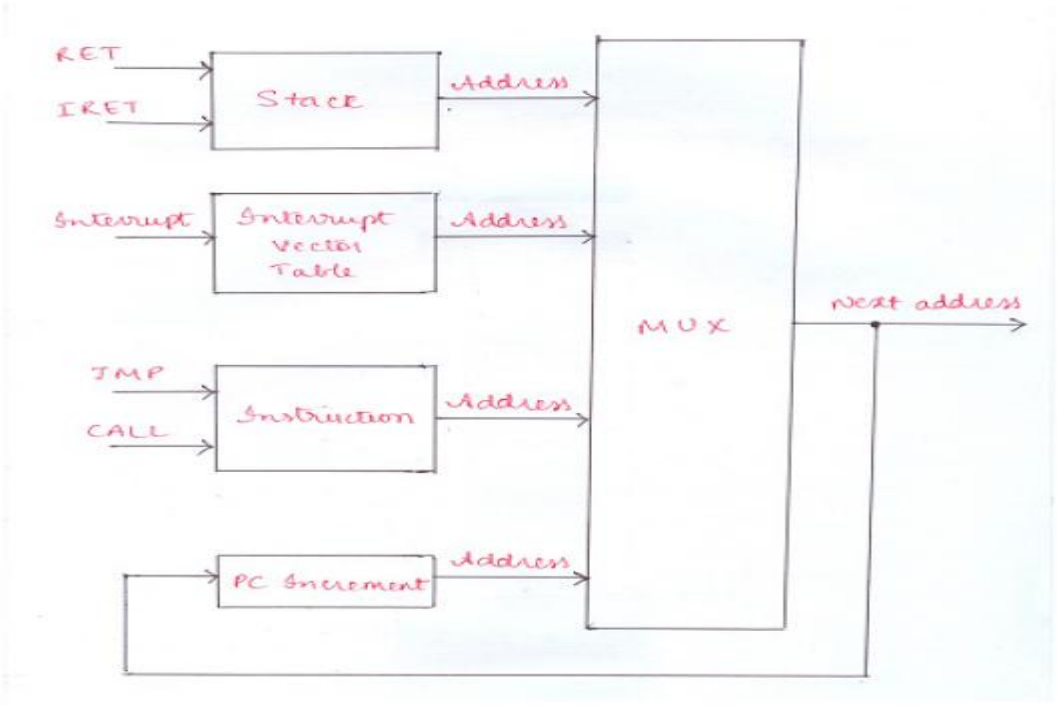
[1M for each]

(b) Explain the purpose of program sequencer with block diagram.

Ans: It is a part of the control unit used to generate instruction addresses in sequence needed to access instructions. It calculates the address of the next instruction to be fetched. The next address can be from one of the following sources.

a. Program Counter
b. Instruction register in case of branching, looping and subroutine calls
c. Interrupt Vector table
d. Stack which holds the return address

The block diagram of a program sequencer is as shown [2M]



[2M]

4 (a) Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier.

Ans: The advent of single chip multipliers paved the way for implementing DSP functions on a VLSI chip. Parallel multipliers replaced the traditional shift and add multipliers now a days. Parallel multipliers take a single processor cycle to fetch and execute the instruction and to store the result. They are also called as Array multipliers.

The key features to be considered for a multiplier are:

a. Accuracy

b. Dynamic range

c. Speed

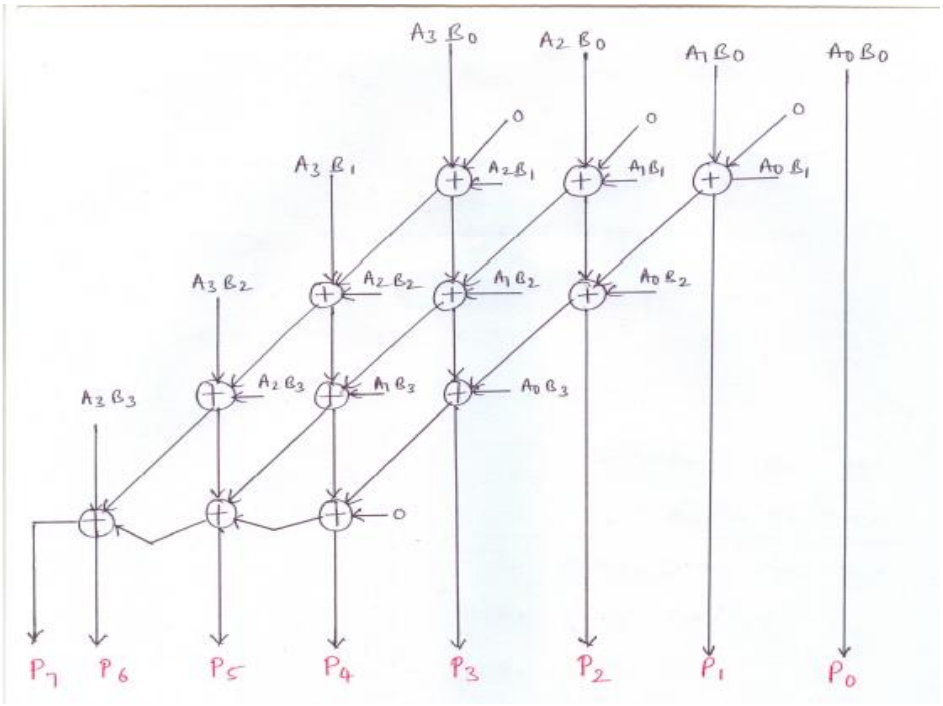
The number of bits used to represent the operands decide the accuracy and the dynamic range of the multiplier. Whereas speed is decided by the architecture employed. If the multipliers are implemented using hardware, the speed of execution will be very high but the circuit complexity will also increases considerably. Thus there should be a tradeoff between the speed of execution and the circuit complexity. Hence the choice of the architecture normally depends on the application.

Parallel Multipliers

Consider the multiplication of two unsigned numbers A and B. Let A be represented using m bits as (Am-1 Am-2 …….. A1 A0) and B be represented using n bits as (Bn-1 Bn-2 …….. B1 B0). Then the product of these two numbers is given by, [2M]

					A_3	A_2	A_1	A_0
					B_3	B_2	B_1	B_0
				A_3B_0	A_2B_0	A_1B_0		A_0B_0
			A_3B_1	A_2B_1	A_1B_1	A_0B_1		
		A_3B_2	A_2B_2	A_1B_2	A_0B_2			
	A_3B_3	A_2B_3	A_1B_3	A_0B_3				
P7	P6	P5	P4	P3	P2	P1		P0

This operation can be implemented paralleling using Braun multiplier whose hardware structure is as shown in the figure



[3M]

Multipliers for Signed Numbers

In the Braun multiplier the sign of the numbers are not considered into account. In order to implement a multiplier for signed numbers, additional hardware is required to modify the Braun multiplier. The modified multiplier is called as Baugh-Wooley multiplier.

Consider two signed numbers A and B,

$$A = -A_{m-1}2^{m-1} + \sum_{i=0}^{m-2} A_i 2^i$$

$$B = -B_{n-1}2^{n-1} + \sum_{j=0}^{n-2} B_j 2^j$$

[2M]

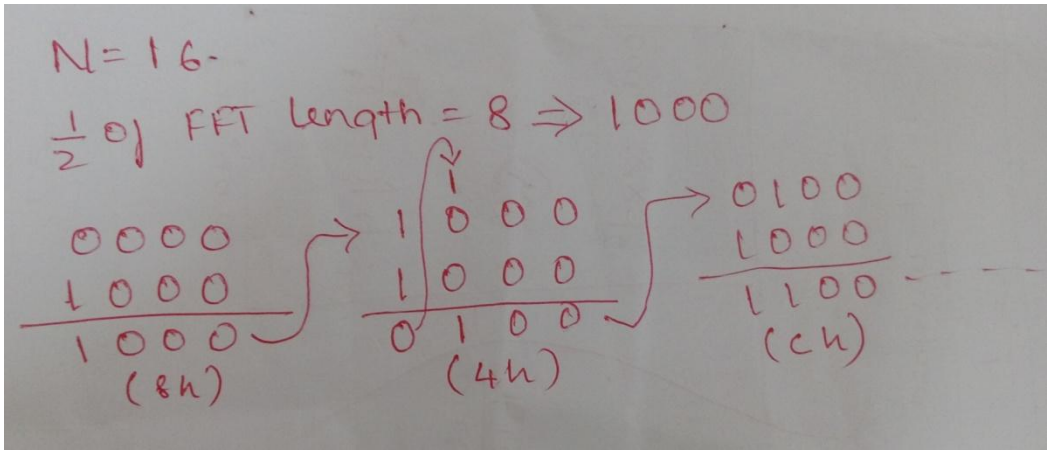
$$\text{Product } P = P_{m+n-1} \ldots\ldots P_1 P_0$$

$$P = A_{m-1}B_{n-1}2^{m+n-2} + \sum_{i=0}^{m-2}\sum_{j=0}^{n-2} A_i B_j 2^{i+j} - \sum_{i=0}^{m-2} A_i B_{n-1} 2^{n-1+I} - \sum_{j=0}^{n-2} A_{m-1} B_j 2^{m-1+j}$$

Speed: Conventional Shift and Add technique of multiplication requires n cycles to perform the multiplication of two n bit numbers. Whereas in parallel multipliers the time required will be the longest path delay in the combinational circuit used. As DSP applications generally require very high speed, it is desirable to have multipliers operating at the highest possible speed by having parallel implementation.

(b) Compute the sequence in which the input data should be ordered for a 16 point DIT FFT using bit reversed addressing mode.

Ans:

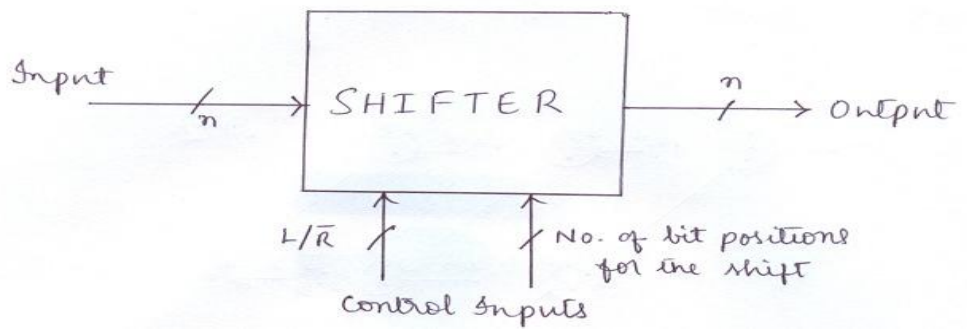


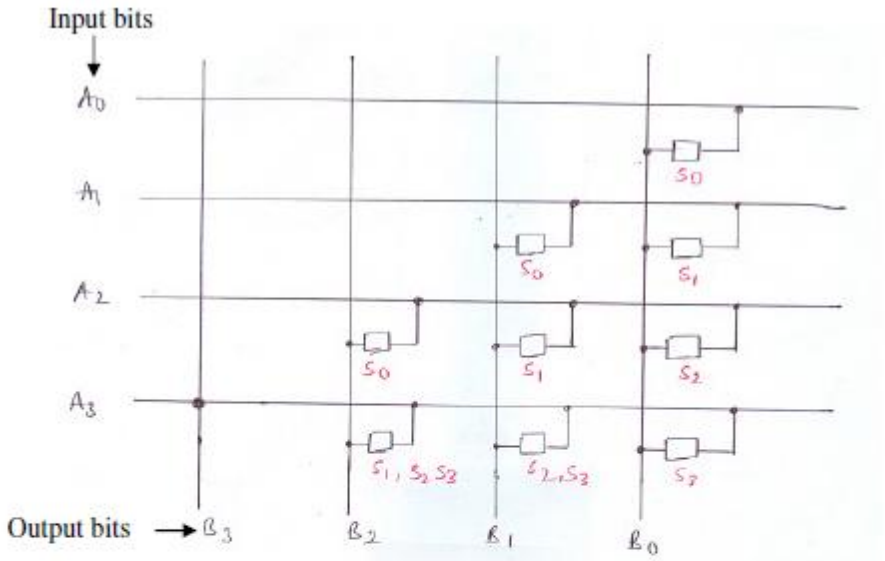
Index in Binary	BCD Value	Bit reversed Index	Value in h
0000	0	0000	0
0001	1	1000	8
0010	2	0100	4
0011	3	1100	C
0100	4	0010	2
0101	5	1010	A
0110	6	0110	6
0111	7	1110	E
1000	8	0001	1
1001	9	1001	9
1010	10	0101	5
1011	11	1101	D
1100	12	0011	3
1101	13	1011	B
1110	14	0111	7
1111	15	1111	F

[3M]

5(a) What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram.

In conventional microprocessors, normal shift registers are used for shift operation. As it requires one clock cycle for each shift, it is not desirable for DSP applications, which generally involves more shifts. In other words, for DSP applications as speed is the crucial issue, several shifts are to be accomplished in a single execution cycle. This can be accomplished using a barrel shifter, which connects the input lines representing a word to a group of output lines with the required shifts determined by its control inputs. For an input of length n, $\log_2 n$ control lines are required. And an additional control line is required to indicate the direction of the shift. The block diagram of a typical barrel shifter is as shown in figure [3M]





INPUT				SHIFT (SWITCH)	OUTPUT (B_3 B_2 B_1 B_0)			
A_3	A_2	A_1	A_0	0 (S_0)	A_3	A_2	A_1	A_0
A_3	A_2	A_1	A_0	1 (S_1)	A_3	A_3	A_2	A_1
A_3	A_2	A_1	A_0	2 (S_2)	A_3	A_3	A_3	A_2
A_3	A_2	A_1	A_0	3 (S_3)	A_3	A_3	A_3	A_3

Fig 2.4 Implementation of a 4 bit Shift Right Barrel Shifter

[3M]

Figure 2.4 depicts the implementation of a 4 bit shift right barrel shifter. Shift to right by 0, 1, 2 or 3 bit positions can be controlled by setting the control inputs appropriately.

(b) Draw the schematic diagram of the saturation logic and explain the same

Ans: Overflow/ underflow will occur if the result goes beyond the most positive number or below the least negative number the accumulator can handle. Thus the overflow/underflow error can be resolved by loading the accumulator with the most positive number which it can handle at the time of overflow and the least negative number that it can handle at the time of underflow. This method is called as saturation logic. A schematic diagram of saturation logic is as shown in figure 2.7. In saturation logic, as soon as an overflow or underflow condition is satisfied the accumulator will be loaded with the most positive or least negative number overriding the result computed by the MAC unit.[2M]

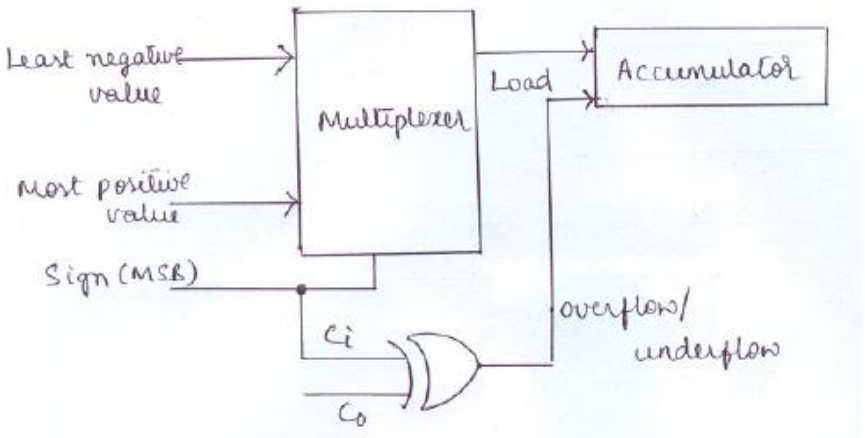


Fig 2.7 A Schematic Diagram of the Saturation Logic

[2M]

6(a) Explain the pointer updating algorithm for circular addressing mode.

Ans: While processing the data samples coming continuously in a sequential manner, circular buffers are used. In a circular buffer the data samples are stored sequentially from the initial location till the buffer gets filled up. Once the buffer gets filled up, the next data samples will get stored once again from the initial location. This process can go forever as long as the data samples are processed in a rate faster than the incoming data rate.

Circular Addressing mode requires three registers viz

a. Pointer register to hold the current location (PNTR)

b. Start Address Register to hold the starting address of the buffer (SAR)

c. End Address Register to hold the ending address of the buffer (EAR)

There are four special cases in this addressing mode. They are

a. SAR < EAR & updated PNTR > EAR

b. SAR < EAR & updated PNTR < SAR

c. SAR >EAR & updated PNTR > SAR

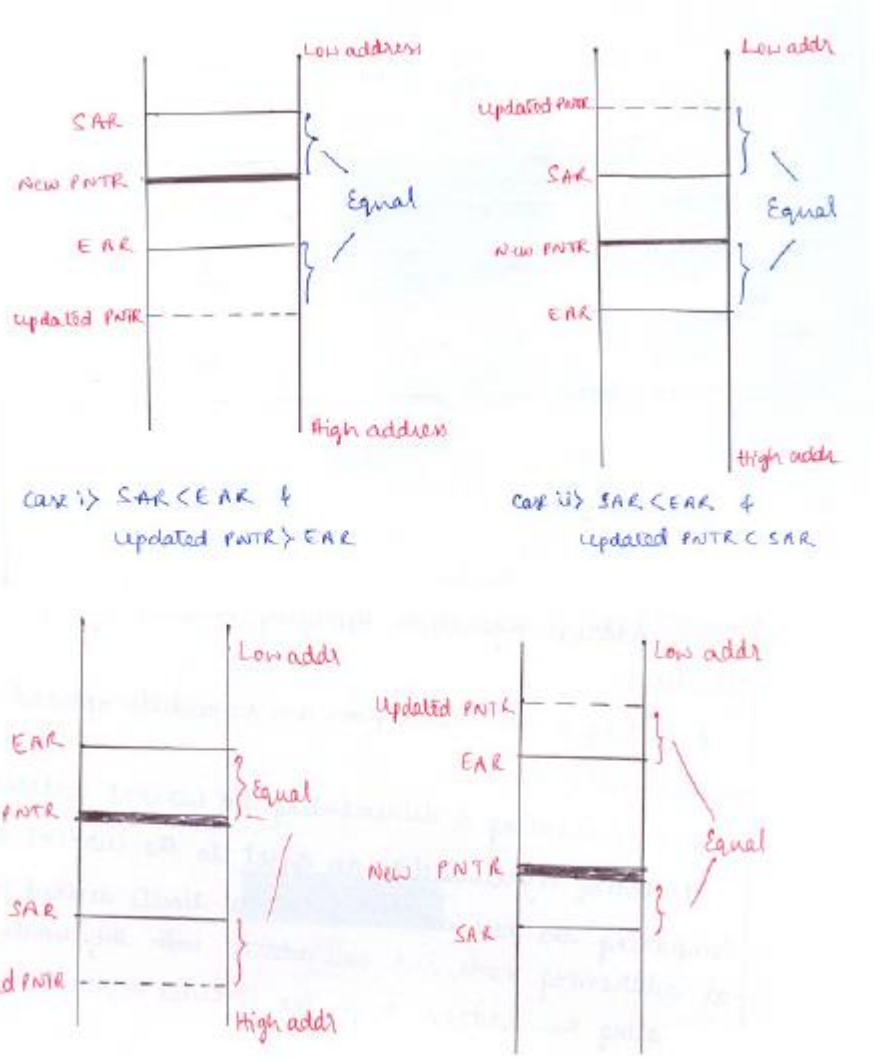
d. SAR > EAR & updated PNTR < EAR

The buffer length in the first two case will be (EAR-SAR+1) whereas for the next tow cases (SAR-EAR+1)

The pointer updating algorithm for the circular addressing mode is as shown below.

```
; Pointer Updating Algorithm

Updated PNTR ◄——— PNTR ± increment

If SAR < EAR
        And if Updated PNTR > EAR then
                New PNTR ◄——— Updated PNTR – Buffer size
        And if Updated PNTR < SAR then
                New PNTR          Updated PNTR + Buffer size

If SAR > EAR
        And if Updated PNTR > SAR then
                New PNTR ◄——— Updated PNTR – Buffer size
        And if Updated PNTR < EAR then
                New PNTR ◄——— Updated PNTR + Buffer size

Else
        New PNTR ◄——— Updated PNTR
```

[2M]



[4M]

(b) Calculate the memory addresses of the operands in each of the following cases of indirect addressing modes? In each case, what will be the content of the *addreg* after the memory access? Assume that the initial contents of the *addreg* and the *offsetreg* are 0200h and 0010h, respectively. i) ADD **addreg* ii).ADD *+*addreg* *iii)*ADD *offsetreg+,*addreg* iv) ADD **addreg,offsetreg-*

Instruction	Addressing Mode	Operand Address	addreg Content after Access
ADD **addreg-*	Post Decrement	0200h	0200-01=01FFh
ADD *+*addreg*	Pre Increment	0200+01=0201h	0201h
ADD *offsetreg+,*addreg*	Pre_Add_Offset	0200+0010=0210h	0210h
ADD **addreg,offsetreg-*	Post_Sub_Offset	0200h	0200-0010=01F0h

[1M for each]