CMR
INSTITUTE OF
TECHNOLOGY

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Internal Assesment Test - II

Sub:	BASIC ELECTRONICS							Code:	15ELN15
Date:	02/10/2016	Duration:	90 mins	Max Marks:	50	Sem:	I	Section:	L, M, N, O

Answer Any FIVE FULL Questions

		Marks	OBE CO	OBE RBT
1.(a)	Design a fixed Current bias circuit with V_{CE}=5V and I_C=3mA when supply voltage is 12V. Assume Si transistor with β=60.	[6]	CO3	L3
(b)	Calculate the DC Load line and determine the Q-point values for the base bias circuit with V_{CC}=20V, R_B=430 kΩ and R_C=2 kΩ and β=100.	[4]	CO3	L3
2.	For the voltage divider bias circuit shown in Fig. 1, find the value of V_E, I_C, V_{CE} and V_C using approximate method(Assume Si transistor)	[10]	CO3	L3,L4

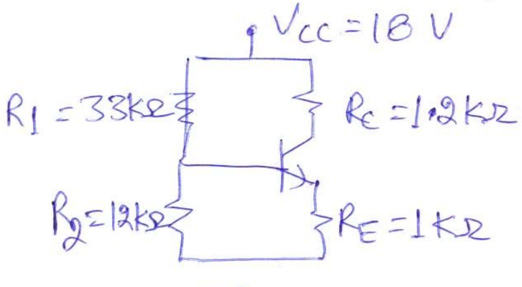
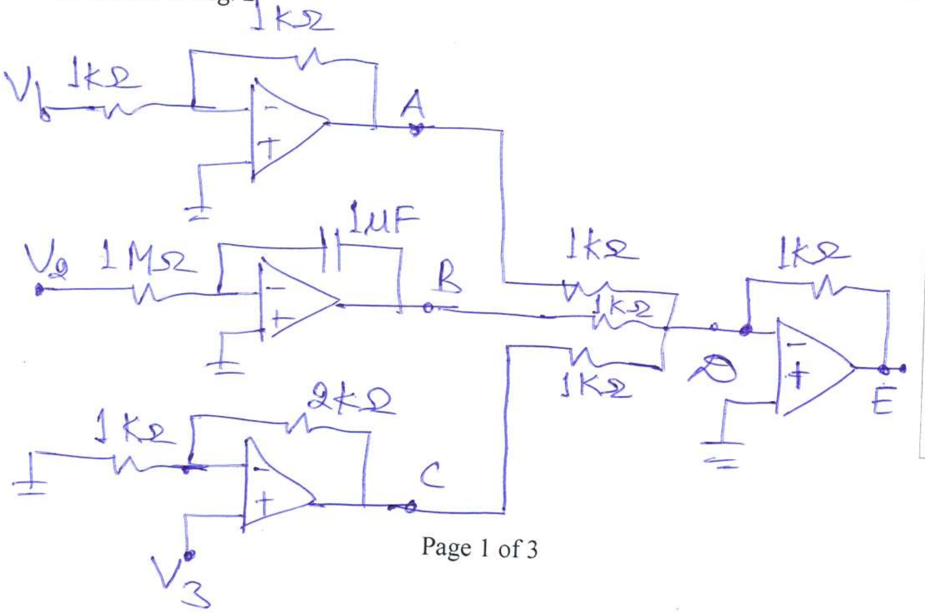


Fig:-1

		Marks	OBE CO	OBE RBT
3(a)	List and explain all Ideal Characteristics of Operational Amplifier.	[5]	CO3	L1,L2
(b)	Write Short note on any one :- (i) Integrator (ii) Inverting Adder	[5]	CO3	L1, L2
4.	Write expressions for output voltage at points A, B, C, D and E from the circuit shown in Fig. 2	[10]	CO3	L3



5.	Convert one number system to other as stated below :- (a) $(11101010)_2 = (\quad)_{10}$ (b) $(01010011)_2 = (\quad)_8$ (c) $(5E)_{16} = (\quad)_{10}$ (d) $(4D)_{16} = (\quad)_2$ (e) $(12.23)_{10} = (\quad)_2$	[10]	CO4	L3
6(a)	Simplify the given expression and Implement using NAND Gate only $ABC + BC + ACD + \bar{A}CD + CD$	[5]	CO4	L3
(b)	What is Half Adder. Explain it with the help of Truth Table and Logic Diagram	[5]	CO4	L1
7.	What is a Flip-Flop. Explain the operation of S-R Flip Flop using Truth Table and Circuit Diagram	[10]	CO4	L1
8.	Write Short note (any two) (i) Latch (ii) De-Morgan's Theorem (iii) Full Adder	[10]	CO4	L1,L2

Course Outcomes		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1:	Appreciate the significance of electronics in different applications.	1	0	0	0	0	0	0	0	0	0	1	0
CO2:	Understand the working principle of diode and apply them to design rectifiers, filter circuits and wave shaping circuits	3	0	2	0	0	0	0	0	0	1	0	0
CO3:	Design simple circuits like amplifiers (inverting and non inverting), adders, integrators and differentiator using OPAMPs	3	0	2	0	0	0	0	0	0	1	0	0
CO4:	Compile the different building blocks in digital electronics using logic gates and implement simple logic function using basic universal gates	2	0	0	0	0	0	0	0	0	1	0	0
CO5:	understand the functioning of a communication system and different modulation techniques	0	0	0	0	0	0	0	0	0	1	0	0
CO6:	understand the basic principles of different types of transducers	0	0	0	0	0	0	0	0	0	1	0	0

Cognitive level	KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PO1 - *Engineering knowledge*; PO2 - *Problem analysis*; PO3 - *Design/development of solutions*; PO4 - *Conduct investigations of complex problems*; PO5 - *Modern tool usage*; PO6 - *The Engineer and society*; PO7- *Environment and sustainability*; PO8 – *Ethics*; PO9 - *Individual and team work*; PO10 - *Communication*; PO11 - *Project management and finance*; PO12 - *Life-long learning*

①

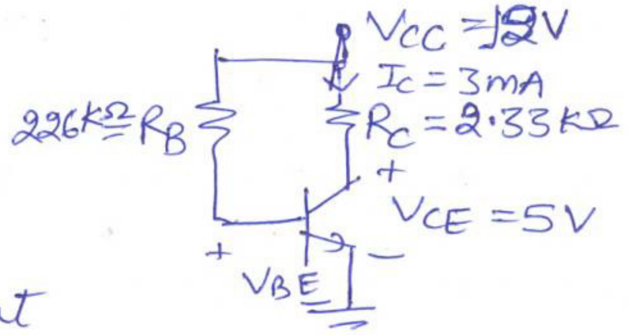
JAGRATI GUPT
ECE. DEPT.

Basic Electronics IAT- 2 Solutions

Q.1 Answer

1.(a) $\beta = 60$

$R_B = ?$, $R_C = ?$



$V_{CC} = 12V$
$I_C = 3mA$
$R_C = 2.33k\Omega$
+
$V_{CE} = 5V$
−
$226k\Omega = R_B$
+
V_{BE}

Applying KVL at input side of opam transistor

$$\Rightarrow \quad R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_B = \frac{12 - .7}{I_B} \qquad \boxed{I_B = \frac{3mA}{60}}$$

$$R_B = \frac{11.3}{3} \times 60 \times 10^3$$

$$\boxed{R_B = 226k\Omega}$$

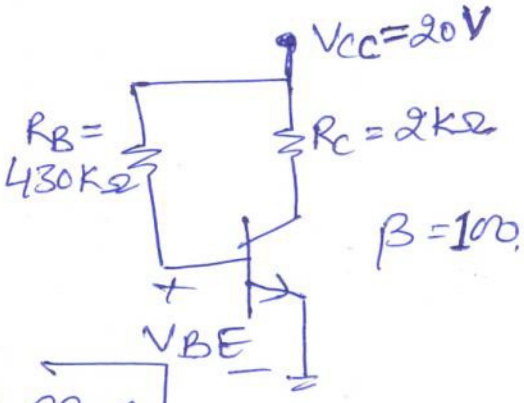
Also,

$$V_{CC} = I_C R_C + V_{CE}$$

$$12 = 3 \times 10^{-3} \times R_C + 5$$

$$\boxed{R_C = 2.33k\Omega}$$

1.(B)



$V_{CC} = 20V$
$R_B = 430k\Omega$
$R_C = 2k\Omega$
$\beta = 100$
+
V_{BE}

We have,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\boxed{I_B = \frac{20 - .7}{430k\Omega} = 44.88\mu A}$$

$I_C = \beta I_B$

$I_C = 100 \times 44.88\,\mu A = 4.48\,mA$

Applying KVL, we have,

$V_{CC} = I_C R_C + V_{CE}$

$20 = 4.48 \times 10^{-3} \times 2 \times 10^{3} + V_{CE}$

$\boxed{V_{CE} = 11.04\,V}$

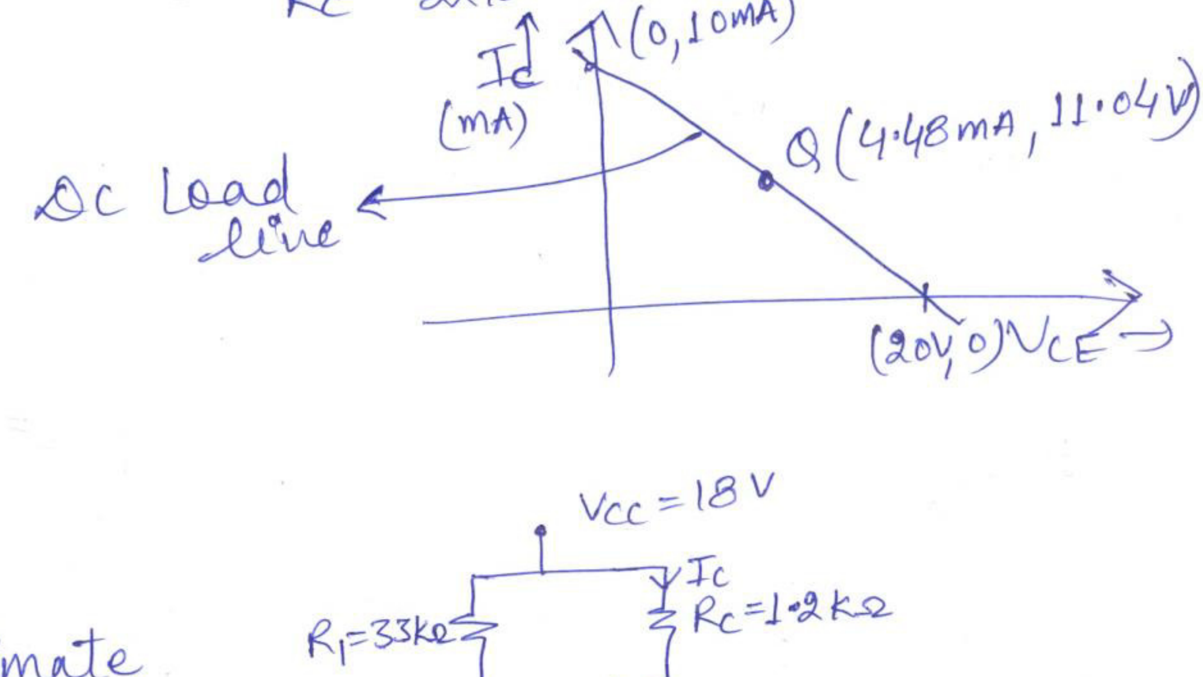
So, Q Point $(I_c, V_{CE}) = Q(4.48mA, 11.04V)$

Load Line

$V_{CC} = I_C R_C + V_{CE}$

At $I_C = 0 \Rightarrow V_{CE} = V_{CC} = 20V$

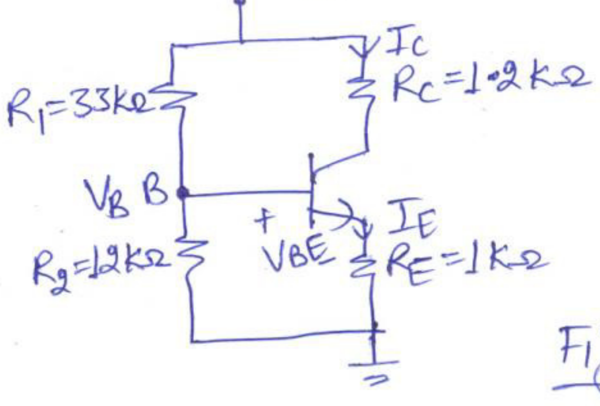
At $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{20}{2 \times 10^3} = 10mA$



Ans. 2

By Approximate method

$V_B = \left(\frac{R_2}{R_2 + R_1}\right) V_{CC}$



$V_{CC} = 18V$
I_C
$R_C = 1.2k\Omega$
$R_1 = 33k\Omega$
V_B B
+
V_{BE}
I_E
$R_2 = 12k\Omega$
$R_E = 1k\Omega$

Fig. 1

$V_B = \left(\frac{12}{12+33}\right) 18 = 4.8\,V$

$\Rightarrow V_B = V_{BE} + V_E$

$\Rightarrow \boxed{V_E = 4.8 - .7 = 4.1\,V}$

$\Rightarrow V_E = I_E R_E$

$\Rightarrow \boxed{I_E = \frac{4.1}{1\,k\Omega} = 4.1\,mA}$

$\Rightarrow \boxed{I_C \approx I_E = 4.1\,mA}$ → since Approximate Analysis.

KVL :-

$\Rightarrow V_{CC} = I_C R_C + V_C$

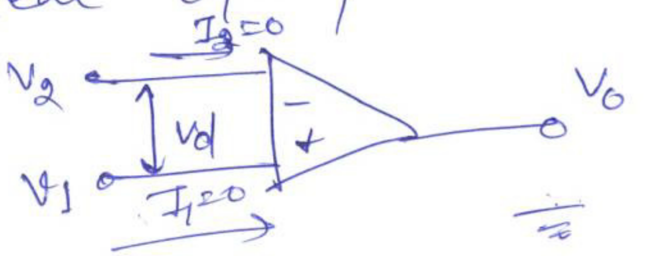
$\Rightarrow V_C = 18 - 4.1\times10^{-3} \times 1.2\times10^{3}$

$\longrightarrow \boxed{V_C = 13.1\,V}$

$\rightarrow \boxed{V_{CE} = V_C - V_E = 13.1 - 4.1 = 9\,V}$

So, $V_E = 4.1\,V$, $I_C = 4.1\,mA$, $V_C = 13.1\,V$, $V_{CE} = 9$

Ans-3 Ideal opamp characteristics



$\boxed{A_{OL} = \infty}$

$I_1 = I_2 = 0$

① Infinite Voltage Gain :- (A_{OL})

$$A_{OL} = \infty$$

$$A_{OL} = \frac{v_o}{v_d} = \frac{v_o}{V_1 - V_2} = \infty.$$

It is differential open loop gain and is infinite for an ideal opamp.
Open loop gain is the gain of the opamp in the absence of feedback from output to the inverting pin of i/p.

② Infinite input Impedance :- ($R_{in} = \infty$)

Infinite Input Impedance ensures that no current can flow into an ideal op-amp. The input Impedance is denoted as Rin. It is the impedance that is offered at the input stage of the opamp circuit.

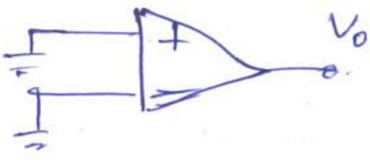
③ Zero output Impedance :- ($R_0 = 0$)

This ensures that the output voltage of the op-amp remains same irrespective of the value of the load resistance connected.
It is zero for an ideal opamp. and is denoted by Ro

④ Zero offset Voltage :- ($V_{ios} = 0$).

Whenever both the i/p terminals of the op-amp are grounded, ideally, the output voltage should be zero. However, in this condition, the practical opamp shows a small non-zero output voltage.
→ To make this output voltage zero, a small voltage in mV is required to be applied to one

of the input terminals. Such a voltage makes output exactly zero. This d.c voltage which makes the output voltage zero, when the other terminal is grounded is called as input offset voltage (V_{ios}).



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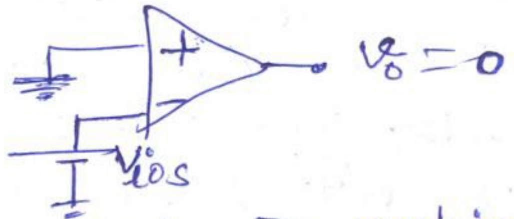


Fig (a) $V_o = V_{ios}$ although I/P voltages $= 0$

Fig (b) → For making $V_o = 0$ V_{ios} is applied at input Pin.

Infinite Bandwidth :-

The range of frequency over which the amplifier performance is satisfactory is called Bandwidth. For ideal opamp, Bandwidth should be infinite.

Infinite CMRR :-

CMRR is called Common Mode Rejection Ratio i.e the ratio of differential Gain and Common mode gain. Thus, infinite CMRR of an ideal opamp ensures zero common mode gain.

→ It is the ability of an op-amp to reject a common mode signal..

$$CMRR = \left|\frac{A_d}{A_{cm}}\right|$$

or $\left[CMRR(dB) = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right| dB \right]$

For Ideal OPAMP :- $\boxed{CMRR = \infty}$ as $[A_{cm} = 0]$

Infinite Slew Rate :- (S=∞)

→ This ensures that the changes in the output voltage occur simultaneously with the changes in the input voltages.

→ When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes. If output does not change with the same rate as input then there occurs distortion in the output. Such distortions are undesirable.

$$\text{Slew Rate}(S) = \left.\frac{dV_o}{dt}\right|_{\text{maximum}}$$

It is expressed in V/usec.

Ideal value of S is ∞ (Infinite).

Power Supply Rejection Ratio (PSRR=0)

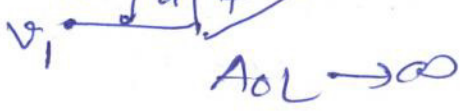
It is defined as the ratio of change in input offset voltage due to the change in supply voltage producing it keeping other power supply voltage constant. It is called as power supply sensitivity

→ Expressed in mV/V or uV/V

→ Ideal value of PSRR = 0.

Voltage Transfer Characteristics of Opamp :-

A_{OL} is ∞ for an opamp.

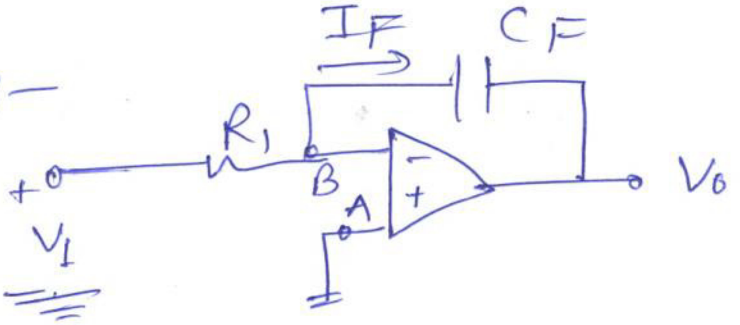


→ But because of saturation property of

Ans-3

(B)

(i) Integrator :-



The O/P voltage is the integration of input voltage.

→ $V_A = 0 = V_B = 0$ (Virtual ground concept)

KCL at node B, we have,

$I_1 = I_F$

$$\frac{v_1 - 0}{R_1} = C_F \frac{d}{dt}(0 - v_0)$$

$$\Rightarrow -\frac{d}{dt}v_0 = \frac{1}{R_1 C_F} v_I$$

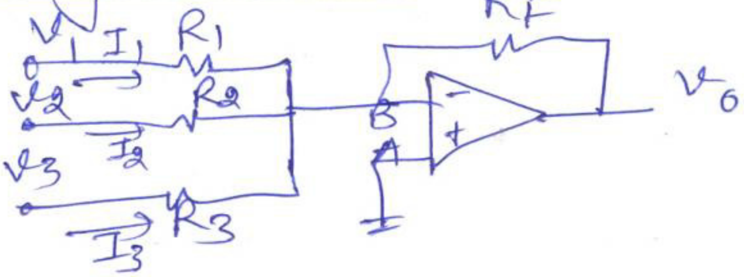
Integrating it,

$$\boxed{v_0 = \frac{-1}{R_1 C_F}\int_0^t v_1 \, dt + c}$$

So, output is integration of the input v_1.

Ans-3 ⓑ

(ii) Inverting Adder



v_1, v_2, v_3 → inputs.

v_0 → o/p of opamp.

$V_A = V_B = 0$

KCL

$$I_1 + I_2 + I_3 = I_F$$

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_0}{R_F}$$

$$\boxed{v_0 = \frac{-R_F}{R_1} v_1 - \frac{R_F}{R_2} v_2 - \frac{R_F}{R_3} V_3}$$

When $R_1 = R_2 = R_3 = R_F = R$

$$\boxed{v_0 = -(v_1 + v_2 + v_3)}$$

Ans-4 $V_A = -\frac{1K}{1K\Omega} V_1 = -V_1$ [Inverting Amplifier ck

$V_B = \frac{-1}{10^{-6} \times 10^{6}} \int_0^t v_2\,dt = -\int_0^t v_2\,dt$ [Integrator]

→ $V_C = \left(1+\frac{2k\Omega}{1k\Omega}\right)V_3 = 3V_3$ [Non-Inverting Amplifier]

→ $V_{\ominus} = 0$ [Virtual Ground concept]

→ $V_E = -\frac{1k\Omega}{1k\Omega}(-V_1) - \frac{1k\Omega}{1k\Omega}\int_0^t -V_1\,dt - 3V_3$

$$\boxed{V_E = V_1 + \int_0^t V_1\,dt - 3V_3}$$

Ans-5

(a) $(\underset{2^7}{1}\underset{2^6}{1}\underset{2^5}{1}\underset{2^4}{0}\underset{2^3}{1}\underset{2^2}{0}\underset{2^1}{1}\underset{2^0}{0})_2 \longrightarrow (\quad)_{10}$

$2^7\times1 + 2^6\times1 + 2^5\times1 + 2^3\times1 + 2^1\times1$

$= (234)_{10}$

(b) $(\underbrace{001}_{\downarrow\atop 1}\,\underbrace{010}_{\downarrow\atop 2}\,\underbrace{011}_{\downarrow\atop 3})_2 \longrightarrow (\quad)_8$

$(123)_8$

(c) $(\underset{16^1}{5}\underset{16^0}{E})_{16} \longrightarrow (\quad)_{10}$

$16^1\times5 + 14\times16^0 = (94)_{10}$

(d) $(4D)_{16} \rightarrow (\quad)_2$

0100 1101

$\Rightarrow (01001101)_2$

(e) $(12.23)_{10} \rightarrow (\quad)_2$

$$\begin{array}{r|ll} 2 & 12 & 0 \\ 2 & 6 & 0 \\ 2 & 3 & 1 \\ & 1 & \end{array}$$

$.23 \times 2 = 0.46$ 0

$.46 \times 2 = 0.92$ 0

$.92 \times 2 = 1.84$ 1

$.84 \times 2 = 1.68$ 1

$\Rightarrow (1100.0011)_2$

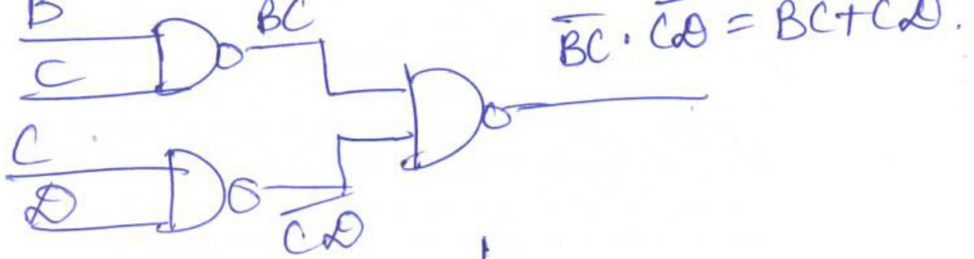
Ans-6

(a) $ABC + BC + ACD + \bar{A}CD + CD$

$BC(1+A) + CD(A+1) + \bar{A}CD$

$= BC + CD + \bar{A}CD = BC + CD(1+\bar{A})$

$= BC + CD$


B
C
C
D
$\overline{BC}$
$\overline{CD}$
$\overline{\overline{BC}\cdot\overline{CD}} = BC+CD.$

↓

NAND Implementation.

Ans-6 (b)

Half Adder is a combinational circuit which adds two inputs and output are Sum and Carry.

Truth Table

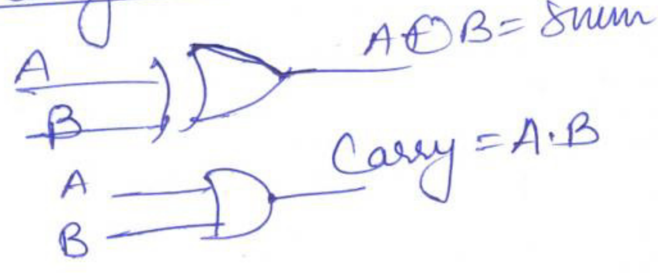
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Equations

$Sum = \bar{A}B + \bar{B}\cdot A = A \oplus B$

$Carry = A \cdot B.$

Logic Diagram



Ans-7 A Flip Flop is a Bistable sequential Circ
that has two stable states that can
be used to store state information.

→ It stores a single bit of data.

→ One of its two states represent a '1' and other a '0'.

Logic Diagram

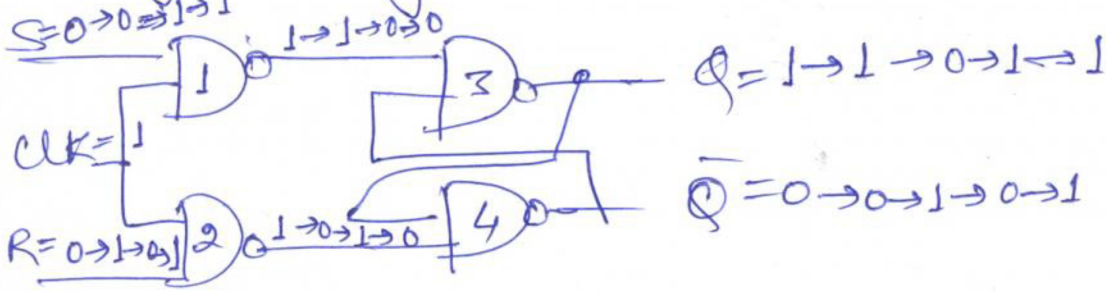

S=0→0→1→1
Clk=1
R=0→1→0→1
1
2
3
4
1→1→0→0
1→0→1→0
Q=1→1→0→1→1
Q̄=0→0→1→0→1

Fig - Flip (S-R) using NAND Gate.

Case-1

Truth Table

Clk	S	R	Q_n	$\bar{Q}_n$	
0	×	×	×	×	
1	0	0	Q_n	$\bar{Q}_n$	→ Hold
1	0	1	0	1	→ Reset
1	1	0	1	0	→ Set
1	1	1	[illegible]	[illegible]	→ Indeterminate State

Operation

Case-1 Let say $Q=1$, $\bar{Q}=0$ and $S=0$, $R=0$.

Thus $Clk=1$,

So, O/P of NAND Gate 1 = 1
" " " 2 = 1
" " " 3 = 1
" " " 4 = 0

So, it is in hold state.

Case-2 clk = 1, S = 0, R = 1

O/P of Gate 1 = 1
2 = 0
3 = 0
4 = 1

So, output Q is at Reset State.

Case-3 Clk = 1, S = 1, R = 0.

O/P of Gate 1 = 0
2 = 1
3 = 1
4 = 0

So, output Q is [illegible] ie Set state.

Case-4 clk = 1, S = 1, R = 1

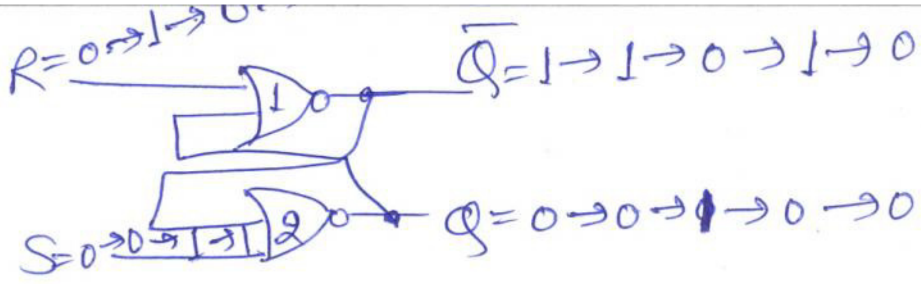
O/P of Gate 1 = 0
2 = 0
3 = 1
4 = 1

O/P Q = 1 and $\bar{Q}$ = 1, Not allowed conditio

Ans-8

(i) Latch:—

Latch stores one bit of information.
It doesn't contain any clock signal (a control signal).
It has two stable states,


R=0→1→0
$\bar{Q}$=1→1→0→1→0
1
2
S=0→0→1→1→1
Q=0→0→1→0→0

S	R	Q_n	$\bar{Q}_n$	
0	0	Q_n	$\bar{Q}_n$	→ Hold state
0	1	0	1	→ Reset "
1	0	1	0	→ set "
1	1	0	0	→ N.A (Invalid)

Case-I S = 0, R = 0,
O/P of Gate 1 = 1
" " " 2 = 0
So, Hold state.

Case-II S = 0, R = 1
O/P of Gate 1 = 0
" " " 2 = 1
So, Reset state

Case-III S = 1, R = 0
O/P of Gate 1 = 1
" " 2 = 0
So, set state

Case-IV S = 1, R = 1
O/P of Gate 1 = 0
" " 2 = 0
So, Invalid state.

Ans-8 (ii) De Morgan's Theorem.

(i) $\overline{A+B} = \bar{A}\cdot\bar{B}$

Complement of the sum of inputs is equal to the product of complemented inputs.

A	B	$\overline{A+B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

(ii) $\overline{A\cdot B} = \bar{A}+\bar{B}$

Complement of the products of inputs variable is equal to the sum of the complemented inpu

A	B	$\overline{A\cdot B}$	$\bar{A}+\bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Ans-8 (iii) Full Adder

→ It has 3 inputs and two outputs i.e sum and Carry.

→ It is a combinational circuit.

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum $= \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\bar{B}\overline{C_{in}} + ABC_{in}$

= ~~Cin(ĀB̄+~~

$= \bar{A}(\bar{B}C_{in} + B\overline{C_{in}}) + A(\bar{B}\overline{C_{in}} + BC_{in})$

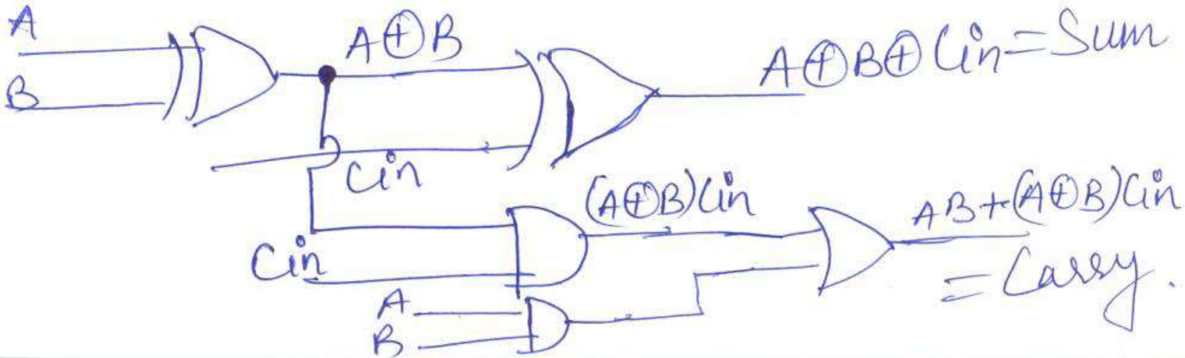
$= \bar{A}(B \oplus C_{in}) + A(\overline{B \oplus C_{in}})$

$= A \oplus B \oplus C_{in}$

Carry $= \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$

$= C_{in}(A \oplus B) + AB(C_{in} + \overline{C_{in}})$

$= (A \oplus B)C_{in} + A \cdot B$


A
B
A⊕B
A⊕B⊕Cin = Sum
Cin
(A⊕B)Cin
Cin
A
B
AB+(A⊕B)Cin
= Carry.