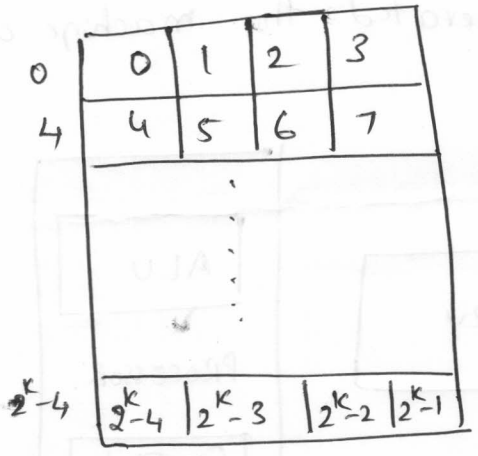
Scheme & Solution [15CS34]

Co-Ist Internals - Sept 2016

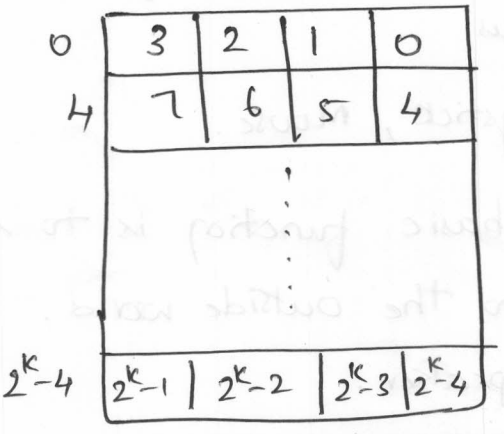
1a) Discuss two ways in which byte addresses are assigned ?

a) Big endian b) Little endian.

→ Big endian :- When lower byte addresses are used for the more significant bytes of the word addressing is called big endian (2M)



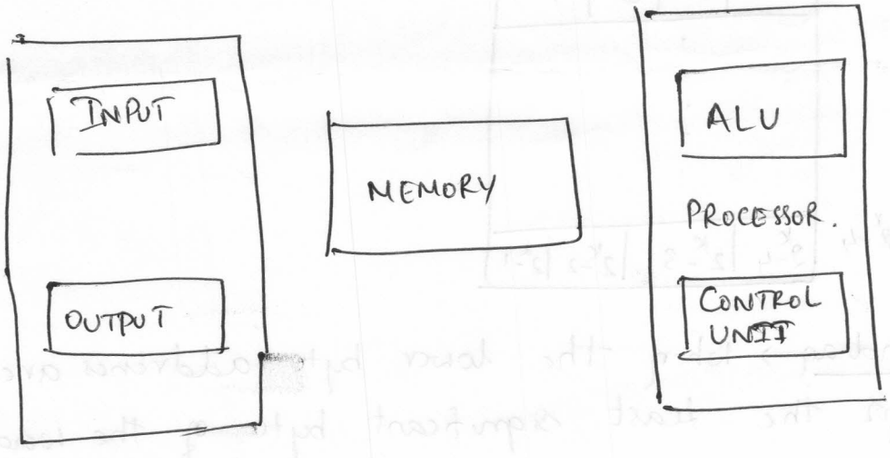
→ Little endian → When the lower byte addresses are used for the least significant byte of the word, addressing is called little endian (2M)



16) What is stored program concept? Explain the functional units of Stored program digital computer with block diagram?

→ The Basic function of computer is to execute program, sequence of instructions, these instructions are stored in the computer memory, these procen is called Stored program concept. (1M)

(ie) According to stored program concept, memory contains the program (source code), the corresponding compiler machine code, editor program and even the compiler that generated the machine code (1M)



(1M)

Input Unit :- Data / Program is fed to a computer through input devices (1M)

Ex :- Joystick, Mouse.

OUTput unit :- Its basic function is to send the Procesed result to the outside world. (1M)

Ex :- printer, speaker.

Memory :- Its function is to store programs and data (1M)

→ Basically two types:
a) Primary memory b) Secondary memory

→ Primary memory → RAM

→ Secondary Memory → Magnetic disk & tapes.

(1M)

ALU & control unit

→ Most of the computer operations are executed in ALU of the processor like addition, subtraction, division, multiplication etc, the operands are brought in to the ALU from memory & stored in registers.

Control unit acts as nerve center that sends signal to other units and senses their states.

→ Actual timing signal that govern the transfer of data between input unit, processor, memory and output are generated by control unit

(2) Consider the following possibilities for saving the return address of a subroutine. (3M)

(a) In a processor register

→ The data to be passed is stored in the registers, and these registers are accessed in the subroutine to process the data

→ In this technique, the main program loads internal registers with appropriate values before calling the subroutine and subroutine then obtains these values by referring pre-defined registers.

Main Program.

```
    :
MOV   R1, 05H
CALL  SUB1
MOV   R2, R3
```

Subroutine

```
SUB1 : MOV  R0, R1
    :
MOV  R3, R2
RET
```

Passing Parameters Using Memory

→ For the cases, where we have to pass few parameters to and from a subroutine registers are a convenient way to do it.

→ However in cases where we need to pass a large number of parameters to subroutine we use memory.

Main Program

```
    :
MOV [LOC], 50H
    :
CALL  SUB1
MOV   R1, [LOC1]
```

Subroutine

```
SUB1: MOV  R1,[LOC]
      :
      MOV [LOC1] ,R1
      RET
```

Passing Parameters Using Pointers.

→ In this technique, the main Program stores the Parameters to be paned in the memory, usually in the consecutive memory locations. Then it loads the internal register pair or pre-defined memory locations with the starting addren of the Parameter list.

```
Main Program
      :
      MOV   R1, 2000H
      :
      Call  Sub1
```

Subroutine

```
Sub1: MOV  R2,[R1]
      :
      RET
```

Passing Paramaters Using stack

→ Stack can be used to pass parameters, to pass parameters to the subroutine using stack, it is necenary to push them on the stack before the call for the subroutine in the main program.

Main Program

```
:
Mov  R0, 1020H
Push R0
Call Sub1
```

Subroutine

```
Sub1
Add  SP, 2
Pop  R1
```

7) Registers R_1 and R_2 of a computer contain the decimal values 1400 and 5000. What is the effective address of the ~~operand~~ Source & destination operand in each of the following instructions. (2M)

i) Load 20(R_1), R_5.

Effective Source Addren: 20 + 1400 = 1420.

Effective destination Addren: R_5.

ii) Mov # 3000, R_5. (2M)

Effective Source Addren: Immediate date: 3000

Effective dustination addren: R5.

(iii) Store 30(R_1, R_2), R_5 (2M)

Effective Source addren: 30 + 1400 + 5000 = 6430

Effective dustination addren: R_5

Add (R2)+, R5

(iv) Effective Source addren: 5000 (2M)

Effective distination addren: R5.

(v) Subtract -(R1), R5. (2M)

Effective Source addren: 1400-1 = 1399

Effective Source addren: R5

6) Write a Program to evaluate the arithmetic Statement Y = (A+B) * (C+D) using three addren, two addren, one address and Zero addren instructions.

Using three addren instructions.

```
ADD  A, B, R1
ADD  C, D, R2
MUL  R1, R2, Y
```

2M

Using two addren instructions

```
MOV  A, R1
ADD  B, R1
MOV  C, R2
MUL  R2, R1
MOV  R1, Y
```

3M

Using one addren instruction.

```
LOAD  A
ADD   B
Store t
LOAD  C
ADD   D
MUL   T
STORE Y
```

3M

Using Zero addren instruction.

```
Push  A
Push  B
ADD
Push  C
Push  D
ADD
MUL
POP   Y
```

2M

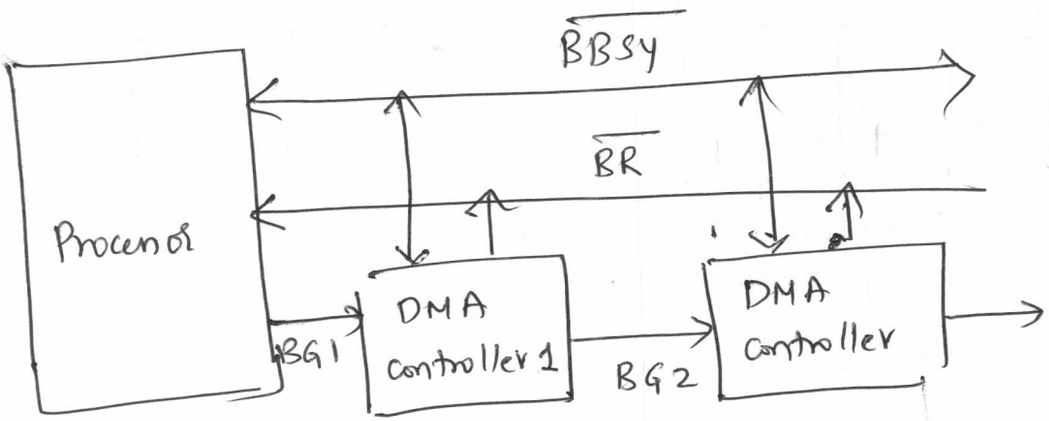
3) What is the necenisity of bus arbitration, Explain the different Methods of bus arbitration?

→ A conflict May arise if both the procenor and a DMA controller try to use the bus at the same time to acces the main memory. Also two or more controllers serving different I/O devica may also attempt to use bus simutaneously. (2M)

to resolve these conflicts, a special circuit called the bus arbiter is provided to co-ordinate the activities of all devices requesting memory transfer.

→ Bus arbitration is process of selecting which device becomes Bus master.

Centralized Arbitration



(2M)

→ DMA controller indicates that it needs to become bus master by activating Bus_request line $\overline{BR}$. The signal on the Bus request line is the logical OR of the bus request from all the devices connected to it.

→ When bus request is activated, the processor activates the Bus Grant signal BG1, indicating to DMA controllers that they may use the bus when bus becomes free.

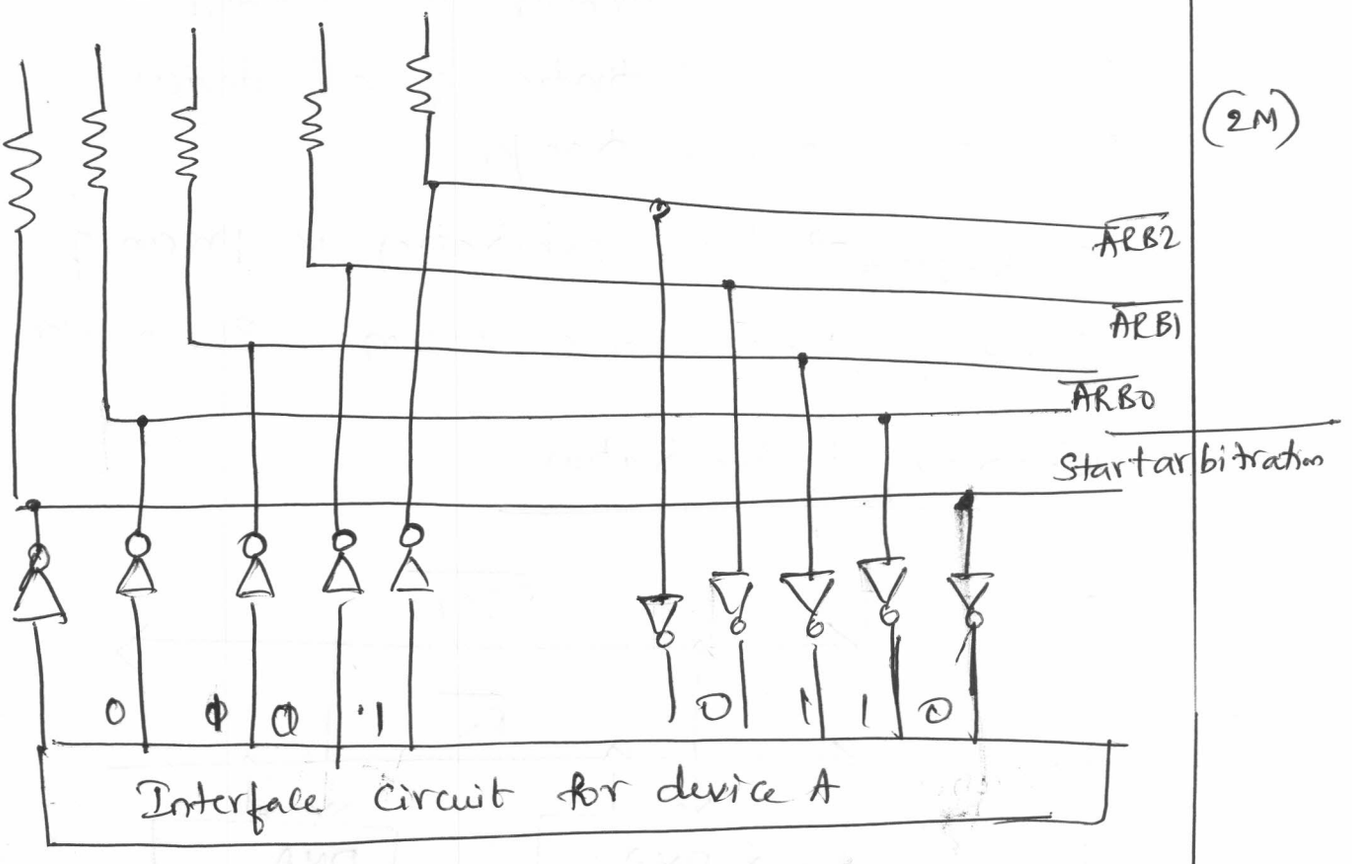
→ Current Bus master indicates to all devices that is using the bus, by activating the Open collector line called Bus Busy $\overline{BBSY}$

(2M)

Distributed Arbitration

(10)

(2M)



(2M)

→ Each device on the bus is assigned a 4-bit identification number; Assume that two devices A and B are requesting service having ID numbers 5 and 6 respectively. Device A transmits the pattern 0101 and device B transmits the pattern 0110. Since the arbitration lines are Active low, the code seen both the device is 0111

→ When device A detects a difference on line $\overline{ARB1}$ and $\overline{ARB0}$, it disables the drivers on that line.

→ Now the arbitration line change to 0110, which means that B has won the contention. Now, device B gets the bus mastership.

4) What is the need for an addressing mode? Explain the following addressing modes with examples. (11)

→ To access the data in different ways by the processor is refferred to as addressing mode. (1M)

(a) Immediate :- The operand is given explicitly in the instruction. (2M)

Ex:- MOV A, #20.

Above instruction copies operand 20 to register A.

(b) direct :- The addres of the location of the operand given explicitly as a part of the instruction. (2M)

Ex:- MOV A, 2000

Above instruction copies the contents of memory location 2000 in to the register.

(c) Indirect :- The effective addres of the operand is the contents of a register or the main memory location whose addres is given explicitly in the instruction. (2M)

Ex:- MOV A, (R0)

Ex:- MOV (LOC), R1

(d) Index :- The effective addres of the operand is generated by adding a constant to the contents of the register. (12) (2M)

Ex:- MOV 20(R1), R2.

(e) Relative :- The effective addres is determined by the index mode using program counter in place of the general purpose procesor register. (2M)

→ This addresing mode is commonly used to specify the target addres in branch instructions.

Ex:- JNZ Back.

5) Define the following terms.

a) Procesor clock (2M)

The time period of procesor clock is denoted by P., the clock rate is given by $R = \frac{1}{P}$ which is measured in cycles per second.

(b) RISC. (2M)

Reduced Instruction set computer, these Processors use hardwired control, they have very few instructions. Clock rate ranges from 20 – 120 MHZ

Ex:- intel i860, SPARC

(c) SPEC rating :- (13) (2M)

$$\text{Spec rating} = \frac{\text{Running time of the reference computer}}{\text{Running time of the computer under test}}$$

$$\text{Spec rating} = \left[\prod_{i=1}^{n} \text{SPEC}_i\right]^{1/n}$$

(d) Basic performance equation (2M)

$$T = \frac{N \times S}{R}$$

N = Number of actual instructions executed by the processor.

S = average number of basic steps.

R = clock Rate measured in clocks per second.

The above equation is known as basic Performance equation.

(e) Stack frame (2M)

During the execution of subroutine (or) nested subroutines the stack contains the entries that are needed by the subroutine and the entries of passing parameters. The map indicating such entries of the stack is called Stack frame