CMR INSTITUTE OF TECHNOLOGY

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Internal Assessment Test II –Nov. 2016

Sub:	Computer Organization			**Code:**	15CS34
Date:	03/11/2016	Duration: 90 mins	Max Marks: 50	**Sem:** III	**Branch:** 3A&B-ISE, 3C-CSE

Note: Answer any five questions:

1. Explain Sequential multiplication algorithm? Perform sequential multiplication for M=1001 and Q=1111. (5M+5M=10M)
2. Perform the operation of division using Restoring and Non Restoring method on the following pairs of numbers where X is the divisor and Y is the dividend X=0101, Y=11111. (5M+5M=10M)
3. Perform the operation of multiplication using Booth algorithm and bit pair recording on following pair of numbers where M=01001 and Q=01111. (5M+5M=10M)
4. Represent the following floating point number in single and double precision format (5M+5M=10M)
   a)1.725 b)-25.125

5a. A computer has L1 and L2 caches. The cache block consists of 8 words. The hit rate is 0.95 for both Caches. the time required to access an 8 words block in L1 cache is 1 cycle and in L2 cache is 10 cycles. Time needed to access L1 cache is 1 cycle, L2 cache is 10 cycles and main memory is 50 cycles. Calculate the average access time experienced by the processor. (6M)

5b. Bring out the comparison between different mapping function techniques (4M)

6. Write a short note on a) PCI Bus b) SCSI Bus (5M+5M=10M)

7. With a neat diagram explain serial interface Device. (10M)

II nd Internal Scheme & Solution

Computer Organization – 15CS34

1) Explain Sequential Multiplication algorithm? Perform Sequential multiplication for M=1001 and Q=1111

5x1=5M

Step 1 : Check for the Q_0 value

Case (a) : If $Q_0 = 1$

→ Add multiplicand with intermediate Product & replace in the same place (A+B) & place back in register A.

→ Then right shift the entire product by 1 bit.

Step 2 : If $Q_0 = 0$

→ No addition process is done

→ Shift the bit by 1 towards the right

Multiplicand M = 1001 (+9)

Multiplier Q = 1111 (+15)

C	A	Q
0	1001	1111
0	0100	1111
0	1101	1111
0	0110	1111

5x1=5M

```
0  1111        1111
0  0111        1111
1  0000        1111
0  1000        0111
```

Product.

2) Perform the operation of division using Restoring and non restoring method on the following pair of numbers using, where X is the divisor and Y is the dividend X = 0101, Y = 11111

5x1=5M

Restoring

```
                A              Q
              000000         11111
LS            000001         1111 □
Add 2's M     111011
              111100         1111 0
                                  ↓
Add M         000101
              000001         11110
LS            000011         1110 □
Add 2's M     111011
              111110         1110 0
                                  ↓
Add M         000101
              000011         11100
LS            000111         1100 □
              111011
              000010         11001
                                  ↑
```

LS 000101 1001

111011

000000 1001 /

LS 000001 0011

Add 2's QM 001011

111100 0011 0

000101

Add M 000001 00110

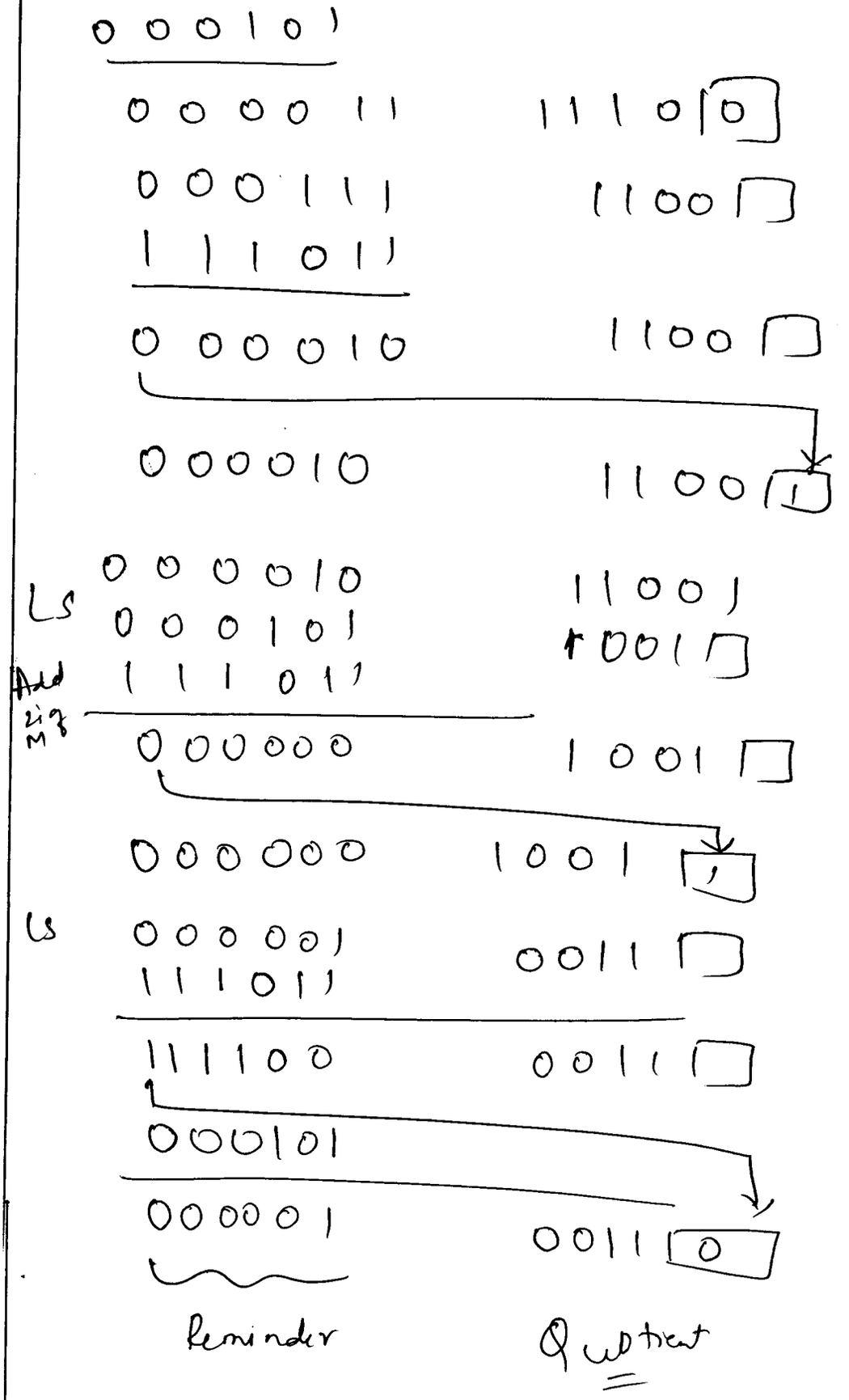
Remainder Quotient.

Non-Restoring

5x1 = 5M

X = 0101 (5), Y = 11111 (31)

	A	Y
	000000	11111
Left shift	000001	1111
Add 2's comp of M	111011	
	111100	1111 0
	000101	1110
	000011	1110
	111011	
	111110	1110


0 0 0 1 0 1
0 0 0 0 1 1
1 1 1 0 0
0 0 0 1 1 1
1 1 1 0 1 1
1 1 0 0
0 0 0 0 1 0
1 1 0 0
0 0 0 0 1 0
1 1 0 0
LS
0 0 0 1 0 1
1 0 0 1
Add 2's M
1 1 1 0 1 1
0 0 0 0 0 0
1 0 0 1
0 0 0 0 0 0
1 0 0 1
1
LS
0 0 0 0 0 1
1 1 1 0 1 1
0 0 1 1
1 1 1 1 0 0
0 0 1 1
0 0 0 1 0 1
0 0 0 0 1
0 0 1 1 0
Remainder
Quotient

3) Perform the operation of multiplication using Booth algorithm and bit pair recording of the following pair of numbers where M=01001 and Q=01111

Solution

M = 01001 (+9) Q=01111 (+15) 5x1=5M

Recoded Multiplier +1 0 0 0 -1

```
        0  1  0  0  1
     +1    0  0  0 -1
  ------------------------
  1  1  1  1  1  1  1  1  1  1
  0  0  0  0  0  0  0  0  0  x
  0  0  0  0  0  0  0  0  x  x
  0  0  0  0  0  0  0  x  x  x
  0  0  1  0  0  1  x  x  x  x
  ------------------------------
  0  0  1  0  0  0  0  1  1  1   (+135)
```

2's complement of multiplicand.

Bit pair Recording of the multiplier. 5x1=5M

Multiplier 0 0 1 1 1 1 0

Booth recoding 0 +1 0 0 0 -1

Bit pair recoding +1 0 -1

```
        0  1  0  0  1
     +1    0    -1
  ------------------------
  1  1  1  1  1  1  1  1  1  1
  0  0  0  0  0  0  0  0  x  x
  0  0  1  0  0  1  x  x  x  x
  ------------------------------
  0  0  1  0  0  0  0  1  1  1   (+135)
```

2's complement of multiplicand

4) Represent the following floating point numbers in single and double precision format.

(a) 1.725.

1.101110×2^0

S = 0 M = 10111001, E = 0

Single precision.

$E' = E + 127$

S = 0, E 0, m = 10111001

$E' = E + 127$

$0 + 127 = 127 = 1111111$

S	E	M
0	11111111	10111001

Double precision

$E' = E + 1023$

$= 0 + 1023 \rightarrow 11111111111$

0	11111111111	10111001

(b) −25.125

25 = 11001

.125 = 001

25.125 = 11001.001

Normalized form → 1.1001001×10^4

Single precision

S	E	M
1	10000011	1001001

Double precision

$S = 1, \quad E = 4, \quad m = 1001001$

$E^1 = E + 1023$

$= 4 + 1023$

$= 1027 \rightarrow 10000000011$

S	M	E
1	10000000011	1001001

5a) A computer has L_1 and L_2 caches. The cache block consists of 8 words. The hit rate is 0.95 for both caches, the time required to access an 8 words block in L1 cache in 1 cycle and in L2 cache is 10 cycles. Time needed to access L1 cache is 1 cycle, L2 cache is 10 cycles and main memory is 50 cycles. Calculate the average access time experienced by the processor. 5×1=5M

$T_{ave} = h_1 C_1 + (1-h_1)\, h_2 C_2 + (1-h_1)(1-h_2) M$ — 2M

$h_1 = 0.95, \quad h_2 = 0.95, \quad C_1 = 1 \text{ cycle}, \quad C_2 = 10 \text{ cycle}$

$M = 50 \text{ cycle}$. } 1M

$= 0.95 \times 1 + (1-0.95) \times 10 + (1-0.95)(1-0.95) \times 50$

$= 0.95 + 0.475 \times 0.125$

$= 1.55 \text{ cycle}$ } 3M

5b) Bring out the comparision between different mapping function techniques (8) (4M)

	Direct Mapping	Associative mapping	Set associative mapping.
(a)	Each block from the main memory has only one Possible location in the cache	A block of data from memory can be placed in to any cache block Position	A block of data from main memory can go into a particular block location of any direct-mapped cache.
(b)	Needs only one comparision	Needs comparision with all tag bits	Needs number of comparisions equal to number of blocks per set.
(c)	Main memory address is divided in to 3 fields. TAG, Block & WORD	Main memory address is divided in to two fields TAG & WORD	Main memory address is divided in to 3 fields TAG, SET & WORD.
(d)	Searching time is less	Searching time is more	Searching time increases with number of blocks per Set.

6. Write a short note on a) PCI Bus b) SCSI bus.

(9)

5x1=5M

PCI BUS

→ Peripheral component Inter connect Bus

→ PCI Bus supports the functions in a standardized format independently of any processor.

→ It is a low cost 32/64-bit bus having plug and play feature for connecting I/O devices

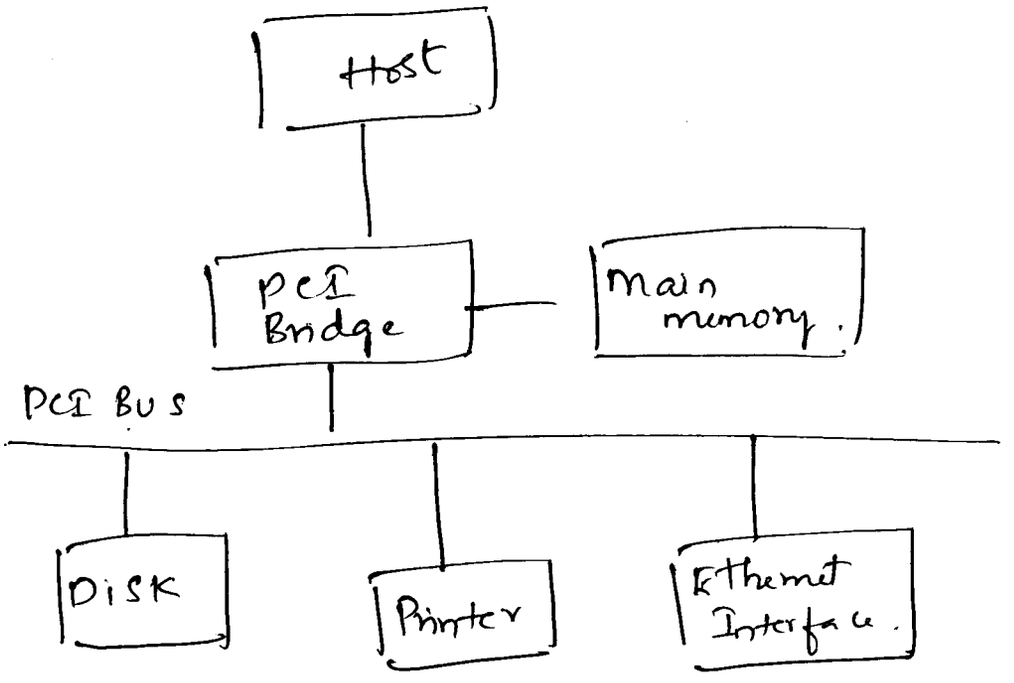
→ PCI Bus is defined for operation with either 5V or 3.3V power supply.

→ PCI Bus is basically designed to support this burst mode of operation.

→ PCI Bus supports three independent address spaces: memory, I/O and configuration.

→ Here A Master (processor or DMA controller) is called an Initiator in PCI terminology, the addressed device which responds to read and write commands is called <u>target</u>

→ A complete transfer operation on the bus, involving an address and burst of data is called a transaction.



@ Use of a PCI Bus in a Computer System.

b) SCSI BUS 5x1=5M

→ Small computer system Interface (SCSI)

→ A SCSI bus may have 8 (or) 16-data lines.

→ The bus may use a single ended transmission (SE) where each signal uses one wire with a common ground return for all signals.

→ There are two types of controllers connected to a SCSI bus- Initiator and target.

→ An Initiator will select a particular target and sends commands specifying the operations to be performed.

→ The SCSI Controller acts as Initiator and the disk controller acts as a target.

→ SCSI standard provides a mechanism needed to establish a logical connection and exchange messages between two controllers.

→ SCSI Standard defines the structure and contents of various types of packets that the controller exchange to handle different situations,

The initiator uses the packets to send the commands it receives (from the processor) to the target. The target responds with status information and data transfer operations.

4) With a neat diagram explain Serial interface Device — 10x1=10.

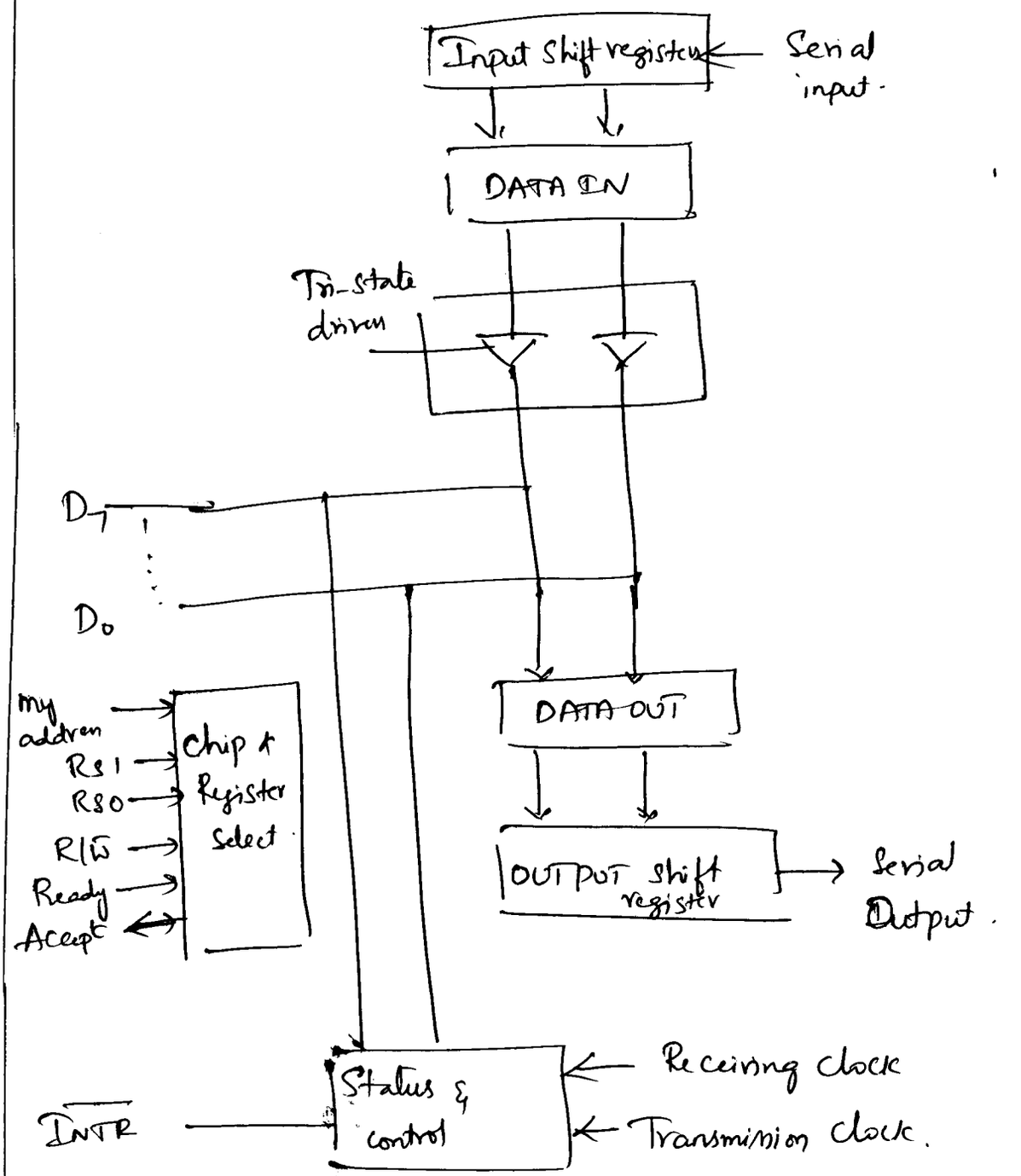
→ Serial port is used to connect the processor to I/O devices that require transmission of data one bit at a time.

→ The Serial Interface circuit is communicating in bit serial way on the device side and in bit parallel format on the bus side

→ When all 8-bits of data are received, the contents of the shift register are transferred to DATAIN register, in parallel.

→ The status flag SIN is set to 1 when new data are loaded in DATAIN; it is cleared to 0 when the processor reads the contents of DATAIN

→ SOUT flag related to output buffer DATAOUT is set to 1 then data are transferred from DATAOUT in to the output shift register and is cleared to 0



@ Serial interface circuit-