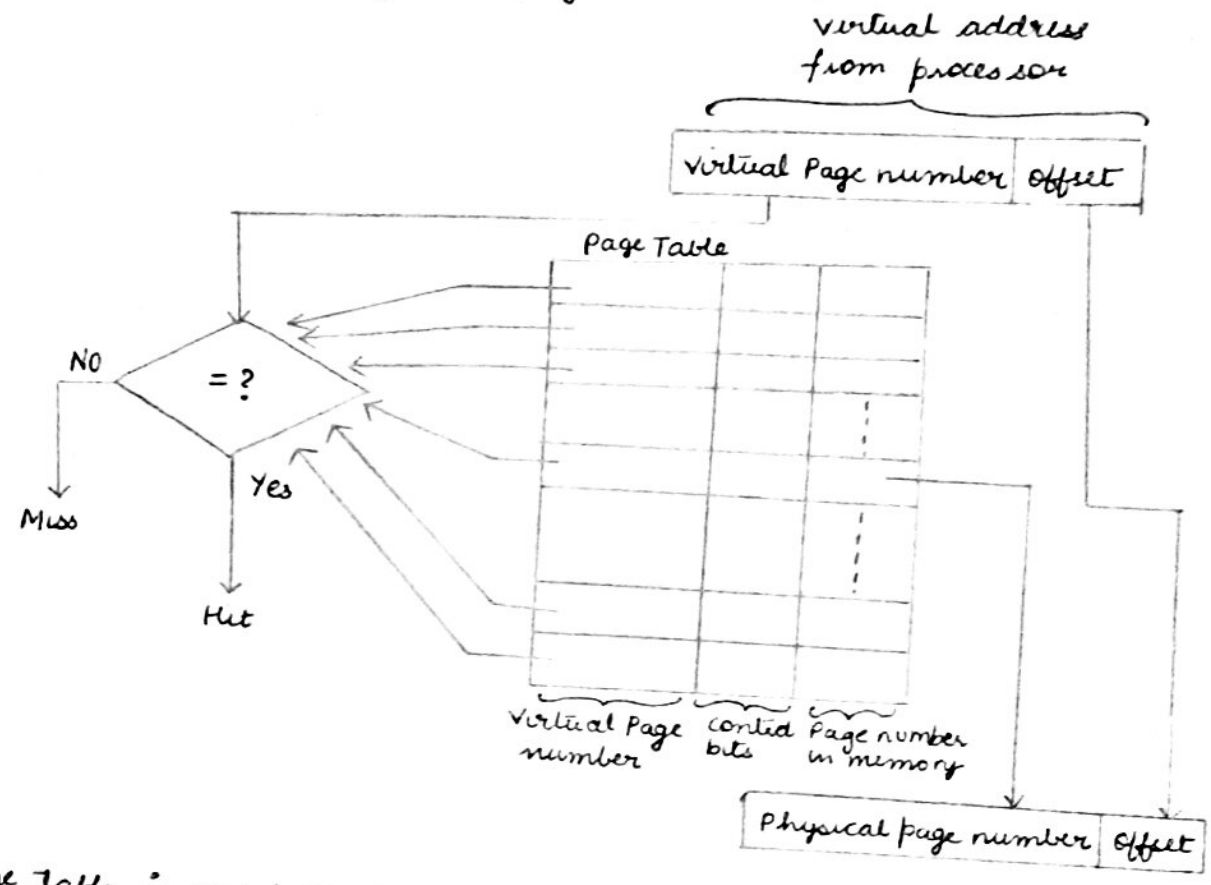
Improvement Test
Solutions

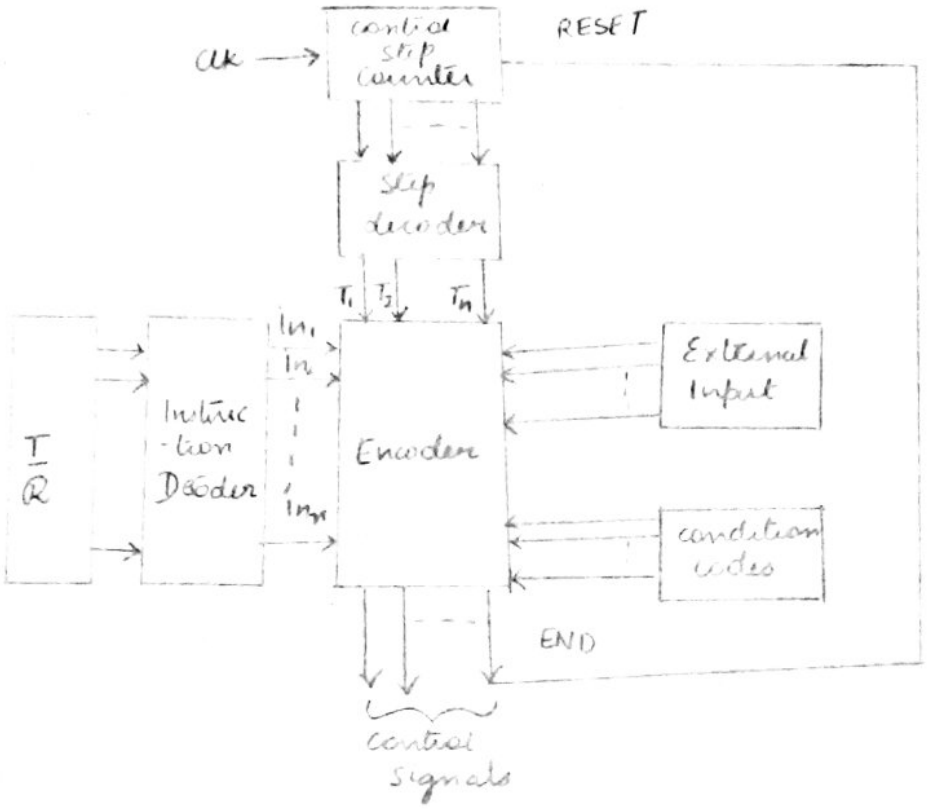
8)> With a neat diagram explain page table implementation



- The page table is used to keep the information about the main memory location of each page This information includes the main memory address where the page is stored and the current status of the page
- To obtain the address of the corresponding entry is the page table the virtual page number is added with the contents of page table base register
- TLB - Translation look aside buffer

  A copy of small position of pages table which has entries above most recently accessed pages stored in cache inside MMU called TLB
- If it gives miss, it is page default that is not in main memory
- When program generates an access request to a page that is not present in main memory a page fault is said to occur

Q2) With a neat diagram explain the organization of microprogrammed control



- In the hardwired control, the control units are fixed logic circuits to interpret instructions & generate control signals from them
- Fixed logics ~~are~~ circuits use contents of the control step counter, contents of the instruction register, contents of condition code flag & the external input signals such as MFC & interrupt & requests to generate control signals.
- Includes combinational circuits (decoder & encoder) generates required control outputs, depending on states of input
- The instruction decoder decodes the instruction loaded in IR If IR is an 8 bit register then instruction decoder generates 2^n, i.e., 256 lines; one for each instruction
- According to code in IR, only one line amongst all output lines of decoder goes high i.e, set to 1 and all other lines are set to 0.

- The step decoder provides a seperate signal line for each step, or time step slot, in a control sequence The encoder gets in the input from instruction decoder, step decoder, external inputs & condition codes
- It uses all these inputs to generate the individual control signals. After execution of each instruction end signal is generated which resets control step counter & make it ready for generation of control step for next instruction

83) Briefly explain the following Replacement Algorithms.

- FIFO

First In First out, This technique uses same concept that stack implementation uses in microprocessors
In this the block which is first loaded in the cache amongst the present blocks in the cache is selected for the replacement

- Optimal

Replaces the page that will not be used for longest period of time
In the replace string if no more elements to search on right, check left

- LRU

Last Recently used, In this technique the block in the set which has been in the cache longest with no reference to it, is selected for the replacement. Since we assume that more-recently used memory locations are more likely to be referenced again. The technique can be easily implemented in the two-way set associative cache organisation.

Q4) ~~Given~~ consider a disk unit having 24 surfaces with 14000 cylinders tracks per surface. Tracks are divided onto 400 sectors and each sector contains 512 bytes of data calculate the data transfer rate when k = 1000 rpm & also calculate the latency & access time if seek time is 6ms.

Given

$P = 24$

$Q = 14000$

$M = 400$

$N = 512$

$$D = (24 \times 14000 \times 400 \times 512)$$

$$= 6.88 \times 10^{10}$$

$$T_r = \frac{M \times N \times k}{60}$$

$$= \frac{400 \times 512 \times 1000}{60}$$

$$=$$

$$\text{Latency time} = \frac{60}{1000}$$

$$= 0.06 \text{ ms}$$

$$\text{Access time} = \frac{0.06}{2} + 6$$

$$= 6.03 \text{ ms}$$

Q5) Write a short note on

i) EPROM

Erasable Programmable Read Only Memory UV rays are used to erase the contents of program

The user cannot erase the ~~user~~ contents of certain selected memory locations

EPROM is cheap, reliable & hence they are widely used

EEPROM – Electrical Erasable Programmable Read Only Memory
uses Electrical signal. It is possible to integrate the ~~circuitry~~ circuitry into the computer, so that the EEPROM does not have to be removed from its socket for programming

FLASH Memory
It consists of non-volatile memory chips that can be used for storage by the computer or the user. Flash memory chips have begun to replace ROMs for storing system information, such as computers BIOS or basic input/ outsystem – the sequence of instructions that computer's ~~BIOS~~ follows during the boot process

86) Explain the sequences of operations needed to perform the following processor function

i) Fetching a word from memory

To fetch a word of data from memory, the processor gives the address of the memory location where the data is stored on the address bus & the activates the read operation. The processor loads the required address in MAR, whose output is connected to the address lines of the memory bus. At the same time processor sends the read signal of memory control bus to indicate the read operation. When the requested data is recieved from the memory it is stored into the MDR, from where it can be transfered to other processor registers

Storing a word in memory

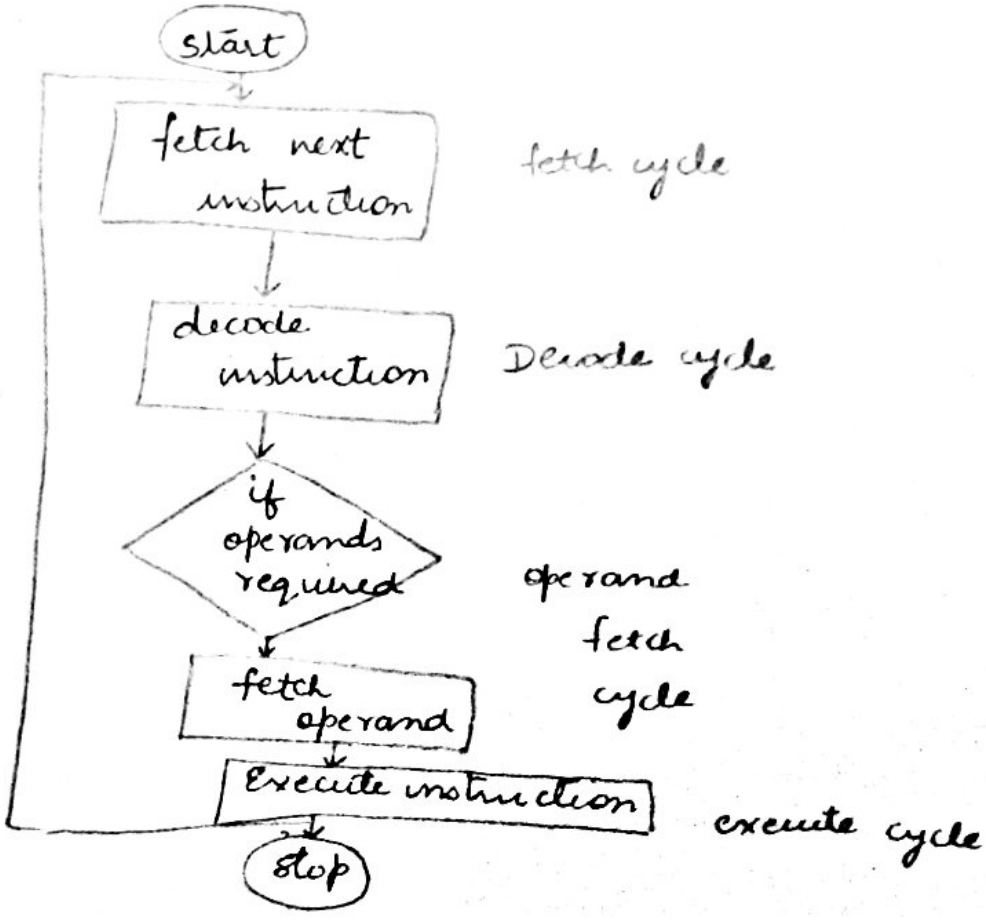
To write a word of data into a memory location processor has to load the address of the desired memory location in the MAR, load the data to be written in memory in MDR and ~~access~~ activates write operation Let us assume that we have to execute instruction MOVE R_1, (R_2) This instruction copies the contents of register R_1 into the memory whose location is specified by the contents of register R_2. The actions needed to execute this instruction are as follows

1) MAR $\leftarrow [R_2]$

2) MDR $\leftarrow [R_1]$

3) Activate control signal to perform write operation. If memory is slow, wait for Memory Function complete (MFC)

87) With a neat diagram explain basic instruction cycle of instruction



- When it ~~stab~~ starts it fetches the instruction to processor
- Then give the decode instruction
- If operands required again it fetches the operand
- Then executes the instruction if more operand is there it again go to start then repeats cycle
- Otherwise stops