CMR INSTITUTE OF TECHNOLOGY

Internal Assessment Test 1 – Sept. 2016

Sub:	Fundamentals of CMOS VLSI			**Code:**	10EC56
Date: 08/ 09 / 2016	Duration: 90 mins	Max Marks: 50	**Sem:** 5th	**Branch:**	ECE (A,B, C D) TCE (A,B)

Note: Answer any five questions.

1 With neat sketches explain the behaviour of n-channel MOSFET enhancement mode device under the influence of different terminal voltages. **[10M]**

2 a) List the expression for threshold voltage of an NMOS transistor and narrate the significance of each term in this equation. **[4M+6M]**

b) Calculate the threshold voltage with $\epsilon_{si} = 11.7\epsilon_o, \epsilon_{ox} = 3.9\epsilon_o$ for an nMOS transistor with $N_A = 2 \times \frac{10^{17}}{cm^3}, t_{ox} = 190°A$. Assume $\phi_{ms} = -0.85, Q_{fc} = 0\ C, N_i = 1.45 \times \frac{10^{10}}{cm^3}$.

3 a) What is noise margin? Obtain the values of V_{IL}, V_{IH}, V_{OL} and V_{OH} from transfer characteristics of a typical inverter. **[4M+6M]**

b) In a $0.5\mu m$ process $\mu_n = 44.69 \times \frac{10^{-3}m^2}{V-sec}, t_{ox} = 14.1nm$ and the $\left(\frac{W}{L}\right) = \frac{30}{5}$. The nMOS has $V_t = 0.71V$ and $V_{gs} = 1.5V$. At what levels of V_{ds} and I_d, will the MOSFET reach pinch-off mode? Hint: $(\epsilon_{ox} = 3.9\epsilon_o)$

4 Derive MOSFET current equation in different regions of operation. **[10M]**

5	Write a short notes on i) Differential inverter, ii) saturated load inverters.	**[5M+5M]**
6	Explain the NMOS fabrication process with neat sketches? Write the steps involved in production of E-beam masks.	**[7M+3M]**
7	Explain the CMOS inverter transfer characteristics highlighting the region of operation of the MOS transistor. Derive the relationship between V_{in} and V_{out} for Region C? Explain the effects of β_n/β_p ratio variations on the transfer characteristics of CMOS inverter.	**[6M+4M]**
8	Write a short notes on i) Body Effect, ii) Channel length modulation.	**[5M+5M]**

(1) With neat sketches explain the behaviorca of n-channel MOSFET enhancement mode device under the influence of different terminal voltages. — 10 marks

→

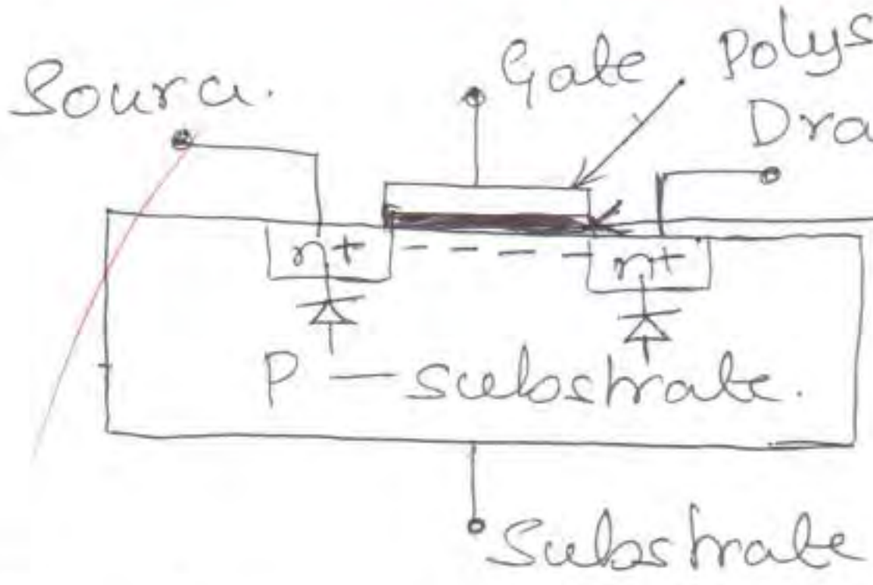


fig (1) - Structure of n-channel MOSFET.

Figure (1) shows the cross sectional structure of n-MOSFET. Starting material p-type semiconductor called substrate in which two n^+-regions are formed using diffusion process called source and drain. Source and drain are separated by small distance called channel. This channel is covered by a thin layer of silicon dioxide. On top of which a layer of ~~poly silicon~~ poly crystalline silicon is deposited.

~~When $V_{GS} \ll V_{th}$~~

When gate to source voltage is very much smaller than threshold voltage i.e., $V_{GS} \ll V_{th}$, mobile positive holes ~~in~~ are distributed throughout the p-type silicon substrate. This is shown in figure (2). This is termed as accumulation mode.

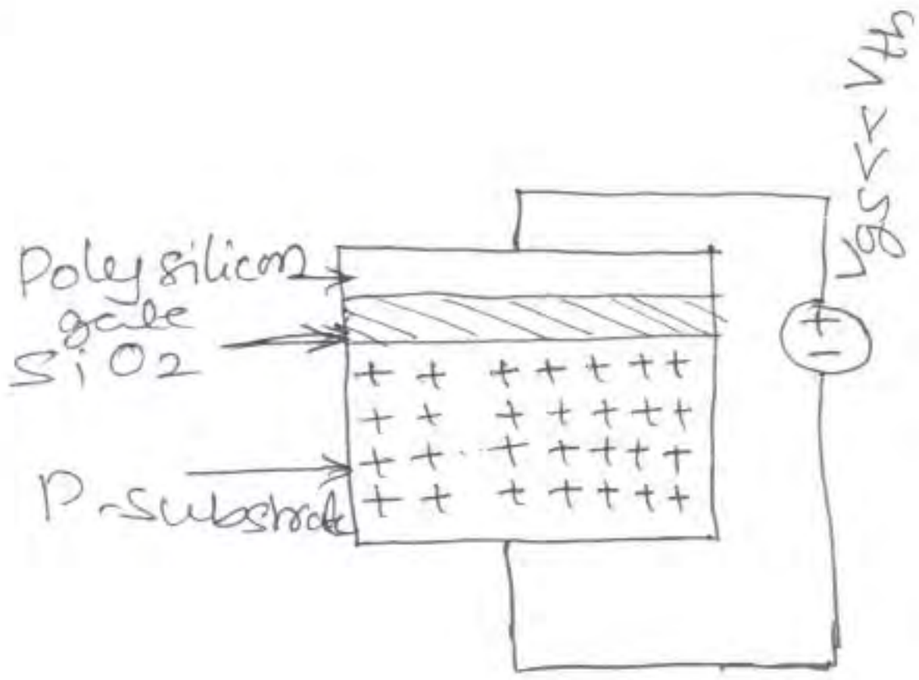


fig (2). Accumulation

As V_{GS} is raised above V_{th} in potential, the holes are repelled causing a depletion region under the gate. Now the structure is in depletion mode as shown in figure 3.

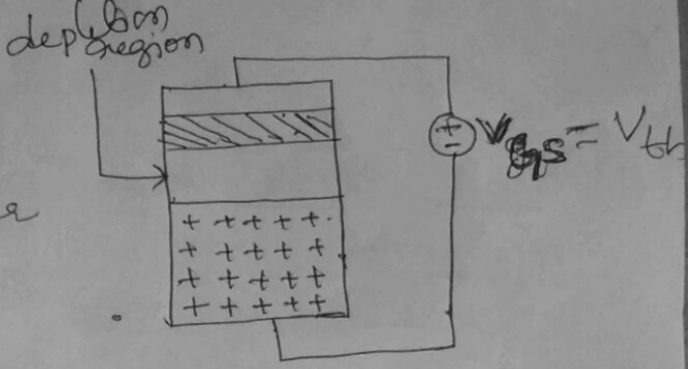


fig (3): Depletion mode

Raising V_{GS} above V_{th} results in electrons being attracted to the region of the substrate under the gate. A conducting layer of the electrons in the p-substrate gives rise to the name inversion mode shown in fig (4).

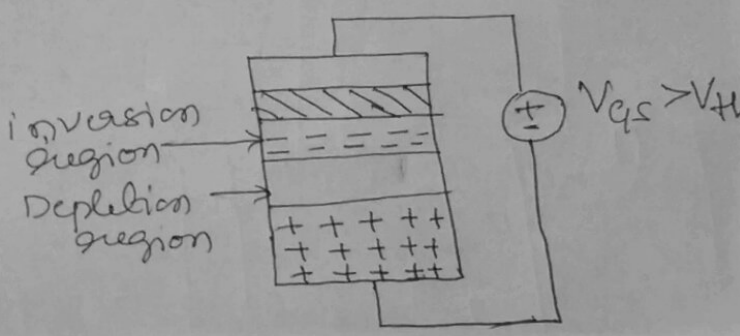
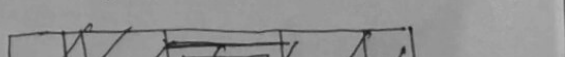


fig (4): Inversion mode

— 05 marks

In an inversion layer substrate junction the n-type layer is induced by the electric field of applied to the gate. This junction, instead of being metallurgical.



With gate to source voltage less than threshold voltage i.e., $V_{GS} < V_{th}$, there is no channel formation. Hence no current flows between source and drain. The MOSFET is said to be operated in cutoff region. The MOSFET structure is as shown in figure 5.

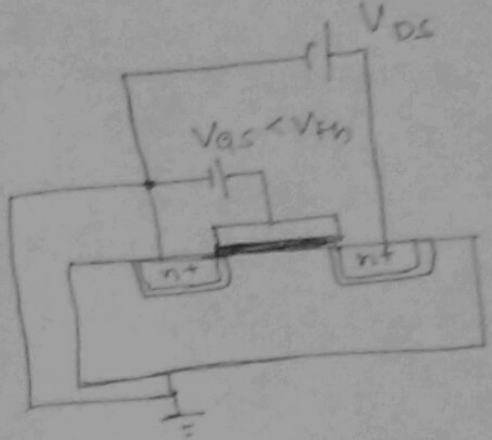


fig 5: Cutoff region.

With gate to source voltage greater than threshold voltage and drain to source voltage i.e., $V_{GS} > V_{th}$, $V_{DS} > 0$ such that $V_{GS} - V_{th} > V_{DS}$ two electrical fields are created within the device. They are Vertical component due to V_{GS} responsible for enhancement of the channel and horizontal component of the field due to V_{DS} responsible for sweeping the electrons in the channel from source to drain results in flow of current. The structure is as shown in figure 6. The device is said to be operated in linear or nonsaturated region.

In linear region, the voltage within the channel is, At source end voltage due to V_{DS} is zero.

$\therefore V_{GS} - V_{th} > V_{DS}$

$V_{GS} - V_{th} > V_{DS}$

$V_{GS} > V_{th}$

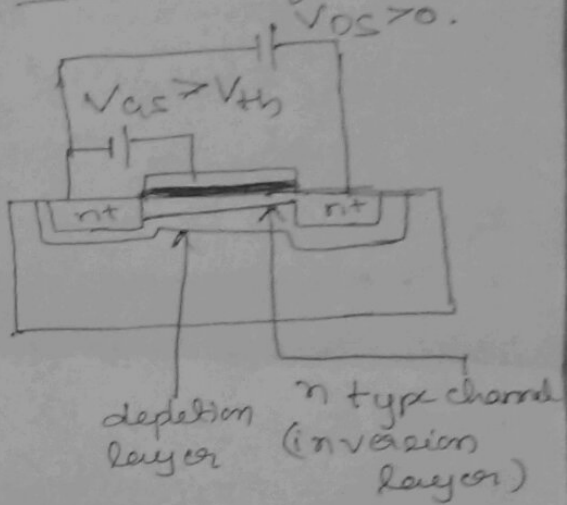


fig 6: linear region

(R) But at drain end ~~drain voltage is fully effective~~ only difference between gate and drain voltage is effective

Hence $V_{GS} - V_{th} > V_{DS}$

$V_G - V_S - V_{th} > V_{DS} - V_S$

$V_G - V_D > V_{th}$

$\therefore V_{GD} > V_{th}$

Hence in linear/nonsaturated region channel will reach from source to drain region. Increased drain to source voltage changes the shape of channel due to resistive drop along the channel.

With $V_{GS} > V_{th}$ and $V_{DS} > 0$.

such that $V_{GS} - V_{th} < V_{DS}$

the device is said to be operated in saturated region.

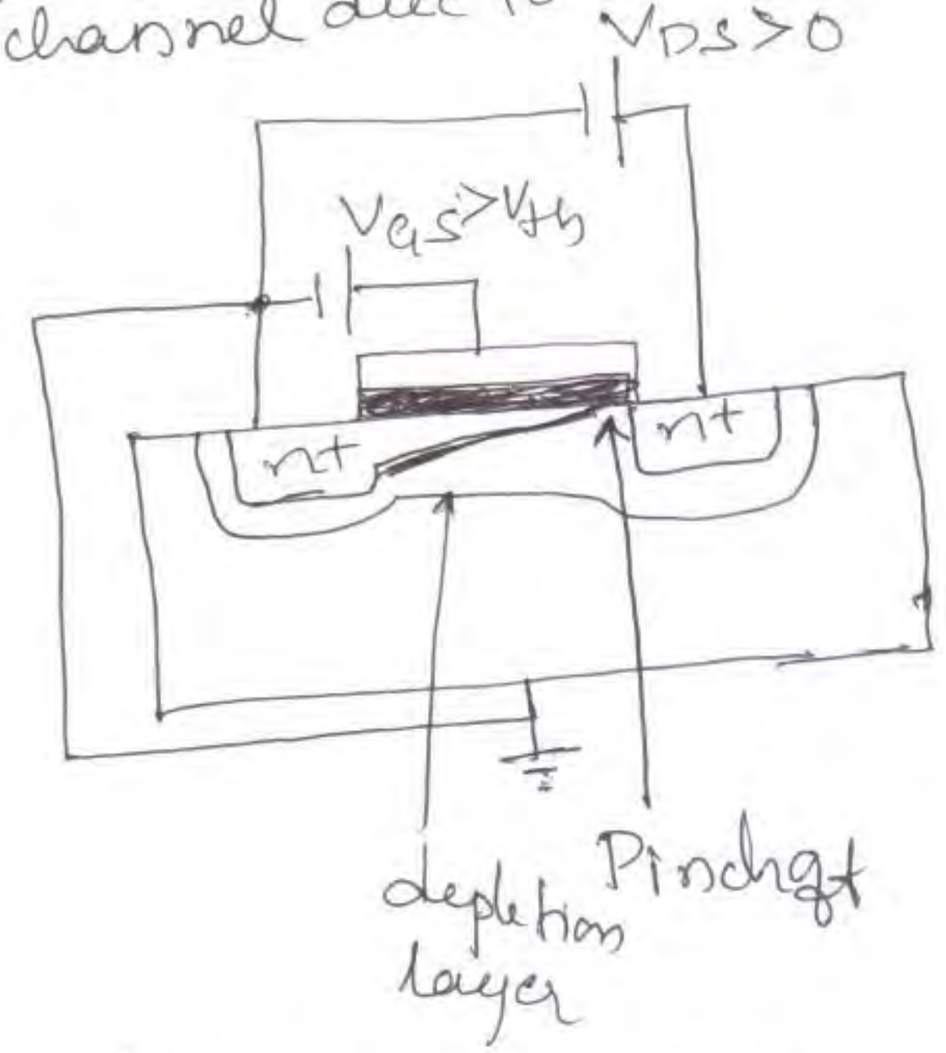


fig 7: saturation region

At the drain end the effective voltage is

$V_{GS} - V_{th} < V_{DS}$

$V_G - V_S - V_{th} < V_D - V_S$

$V_G - V_D < V_{th}$

$V_{GD} < V_{th}$

Gate to drain voltage is less than the threshold voltage. Hence channel will no longer reach the drain diffusion region. Hence channel is said to be pinched off. Current will no longer increases with increase in the drain to source voltage. conduction is brought about by drift mechanism of electrons under the influence of positive drain voltage.

As the electrons leave the channel they are injected (3) into the drain depletion region and subsequently accelerated toward the drain.

Voltage across the pinched off ~~region~~ channel fixed at $V_{GS} - V_{th}$. Current is independent V_{DS} but dependent on $V_{GS} - V_{th}$. The structure in saturation is shown in figure 7.

— 05 marks

(2)

(a) List the expression for threshold voltage ~~with~~ of an NMOS transistor and narrate the significance of each term in this equation.

— 04 marks

→ Threshold voltage is defined as the voltage applied between the gate and source of an MOS device below which the drain to source current drops to zero.

$$V_{th} = V_{th-mos} \pm V_{fb}.$$

$$V_{th} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}} + \frac{Q_b}{C_{ox}} + 2\phi_b.$$

ϕ_{ms} = metal to semiconductor work function difference

$\phi_{ms} = -0.9$ for n^+ gate over p-substrate.

$\phi_{ms} = -0.2$ for n^+ gate over n-substrate.

$Q_b = \sqrt{2q\epsilon_{si}N_A 2\phi_b}$ called bulk charge.

q = charge of an electron = 1.6×10^{-19} C.

$\epsilon_{si} = 11.9\epsilon_0$ = permittivity of Silicon

N_A = Acceptor Dopants density.

— 02 marks

ϕ_b = bulk potential = $\frac{kT}{q} \ln\left(\frac{N_A}{N_i}\right)$ ø. in volts

$k = 1.38 \times 10^{-23}$ J/°k = Boltzmann Constant.

T = Temperature in °k

Ni = Intrinsic carrier concentration = $1.45 \times 10^{10}/cm^3$ at 300° k.

ϵ_0 = Absolute permitivity = 8.854×10^{-14} F/cm.

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ = gate oxide capacitance per unit area.

$\epsilon_{ox} = 3.9\epsilon_0$ = permitivity of silicon dioxide.

t_{ox} = thickness of the gate oxide.

02 marks

② ⓑ Calculate the threshold voltage with $\epsilon_{Si} = 11.7\epsilon_0$, $\epsilon_{ox} = 3.9\epsilon_0$ for an nMos transistor with $N_A = 2 \times 10^{17}/cm^3$, $t_{ox} = 190$ Å. Assume $\phi_{ms} = -0.85$, $Q_{fc} = 0$ C, $N_i = 1.45 \times 10^{10}/cm^3$

— 06 marks

$$V_{th} = 2\phi_b + \frac{Q_b}{C_{ox}} - \frac{Q_{fc}}{C_o} + \phi_{ms} \rightarrow ①$$

Since $Q_{fc} = 0$

① ⇒

$$V_{th} = 2\phi_b + \frac{Q_b}{C_{ox}} + \phi_{ms}$$

$t_{ox} = 190 \times 10^{-10}$ m

$= 190 \times 10^{-10} \times 10^2$ cm

$t_{ox} = 190 \times 10^{-8}$ cm

$\phi_{ms} = -0.85$

$Q_{fc} = 0$ C.

$N_i = 1.45 \times 10^{10}/cm^3$

$N_A = 2 \times 10^{17}/cm^3$

$\epsilon_{ox} = 3.9\epsilon_0$

$\epsilon_{Si} = 11.7\epsilon_0$

$\epsilon_0 = 8.854 \times 10^{-14}$ F/cm

$t_{ox} = 190$ Å $= 190 \times 10^{-10}$ m

~~$t_{ox} = 190 \times 10^{-10} \times 10^2$ cm~~

~~$= 190 \times 10^{-8}$ cm~~

At $T = 300^\circ K$

$$\phi_b = \frac{kT}{q} \ln\left(\frac{N_A}{N_i}\right)$$

$$\phi_b = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \ln\left[\frac{2 \times 10^{17}}{1.45 \times 10^{10}}\right]$$

$\boxed{\phi_b = 0.4253 \text{ Volts}}$ ——— 1 1/2 marks

$$Q_b = \sqrt{2 G_{Si} q N_A 2\phi_b}$$

$$= \sqrt{2 \times 11.7 \times 8.854 \times 10^{-14} \times 1.6 \times 10^{-19} \times 2 \times 10^{17} \times 2 \times 0.4253.}$$

$\boxed{Q_b = 2.374 \times 10^{-7} \text{ C.}}$ ——— 1 1/2 marks ~~0.3M~~

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \epsilon_0}{190 \times 10^{-8}} = \frac{3.9 \times 8.854 \times 10^{-14}}{190 \times 10^{-8}.}$$

$\boxed{C_{ox} = 1.817 \times 10^{-7} \text{ F/cm}^2.}$ ——— 1 1/2 marks

$$V_{th} = 2 \times 0.425 + \frac{2.374 \times 10^{-7}}{1.817 \times 10^{-7}} - 0.85.$$

$$= 0.85 + 1.306 - 0.85$$

$\boxed{V_{th} = 1.306 \text{ Volts}}$ ——— 1 1/2 marks

3@ what is noise margin? Obtain the values of V_{IL}, V_{IH}, V_{OL} and V_{OH} from transfer characteristics of a typical inverter.

4 marks

→ Noise margin is a parameter that allows to determine the allowable noise voltage on the input of a gate so that the output will not be affected.

Low noise margin NM_L is defined as the difference in the magnitude between the maximum low output voltage of the driving gate and the maximum input low voltage recognized by the driven gate.

i.e., $NM_L = |V_{ILmax} - V_{OLmax}|$

High noise margin NM_H is defined as the difference in magnitude between minimum high output voltage of the driving gate and the minimum input high voltage recognized by the driven gate.

i.e., $NM_H = |V_{IHmin} - V_{OHmin}|$.

V_{IHmin} = minimum high input voltage

V_{ILmax} = maximum low input voltage

V_{OHmin} = minimum high output voltage

V_{OLmin} = minimum low output voltage.

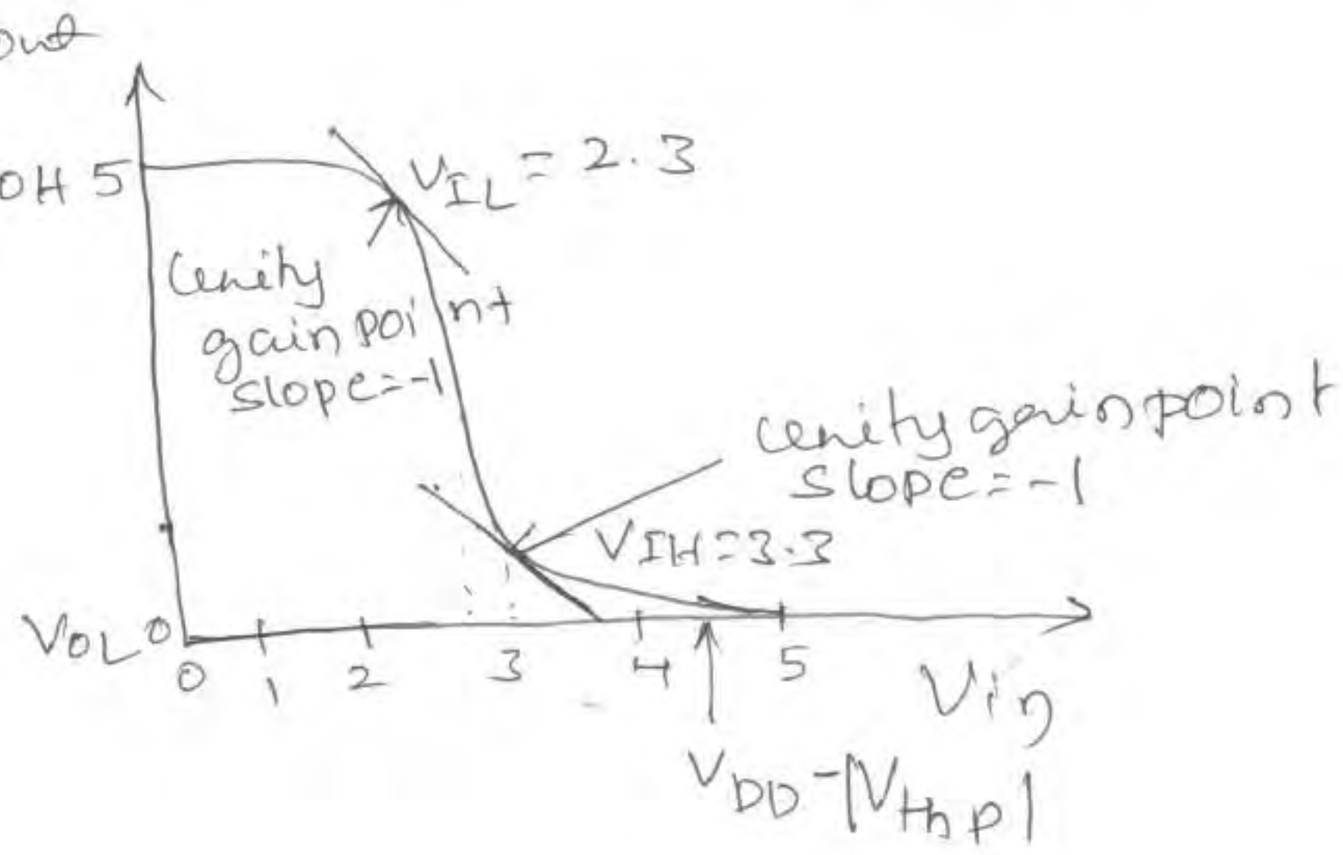
— 2 marks

$V_{IH} = V_{IL}$ is desirable means transfer characteristic should switch abruptly. requires high gain in the transition region.

V_{IL} is found out by determining the unity gain point in the inverter transfer characteristic.
V_{IL} is in region B of inverter ~~region~~ operation

Similarly V_{IH} is found using unity gain point. ~~is the~~ and is in region B of inverter operation.

Found that $V_{IL} = 2.3$, $V_{IH} = 3.3$



2 marks

(3)(b) In a 0.5μm process $\mu_n = 440.69 \times 10^{-3} \frac{m^2}{V\text{-sec}}$, $t_{ox} = 14.1nm$ and the $\frac{W}{L} = \frac{30}{5}$. The nMOS has $V_{th} = 0.71V$ and $V_{GS} = 1.5V$. At what levels of V_{DS} and I_{DS}, will the MOSFET reach pinch off mode? (Hint: $\epsilon_{ox} = 3.9\epsilon_0$)

— 06 marks

→ $t_{ox} = 14.1nm$

$= 14.1 \times 10^{-9} m$

$= 14.1 \times 10^{-9} \times 10^{2} cm$

$\boxed{t_{ox} = 14.1 \times 10^{-7} cm}$

$\mu_n = 440.63 \times 10^{-3} \frac{m^2}{V\text{-sec}}$

$t_{ox} = 14.1nm$

$\frac{W}{L} = \frac{30}{5}$

$V_{th} = 0.71V$

$V_{GS} = 1.5V$

$\epsilon_{ox} = 3.9\epsilon_0$.

For pinch off to occur

$V_{DS} = V_{DSsat} = V_{GS} - V_{th}$

$= 1.5 - 0.71$

$\boxed{V_{DSsat} = 0.79V}$

— 03 marks

The current in pinch off mode is given by

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_0}{14.1 \times 10^{-7}} = \frac{3.9 \times 8.854 \times 10^{-14}}{14.1 \times 10^{-7}}$$

$\boxed{C_{ox} = 2.44 \times 10^{-7} F/cm^2}$

~~I_{DSat}~~ ~~$= 440.63 \times 10^{-3} \frac{cm^2}{V\text{-sec}}$~~

~~$\mu_n = 440.63 \times 10^{-3} \times 10^{-4} \frac{m^2}{V\text{-sec}}$~~

$\mu_n = 44.63 \times 10^{-3}\ m^2/V\text{-sec}$

$\mu_n = 44.63 \times 10^{-3} \times 10^4\ cm^2/V\text{-sec}$

$\mu_n = 44.63 \times 10\ cm^2/V\text{-sec}$

$m^2 = m \times m$

$= 10^2\ cm \times 10^2\ cm$

$= 10^4\ cm^2$

$$\therefore I_{DS} = \frac{44.63 \times 10 \times 2.44 \times 10^{-7}}{2} \times \frac{30}{5} [1.5 - 0.7]^2.$$

$$\boxed{I_{DS} = 2.038 \times 10^{-4} = 0.203\ mA\ Amp.}$$

03 marks

(4) Derive MOSFET current equation in different regions of operation. — 10 Marks

→ There are three regions of operations for MOSFET. They are

1. cut off region.
2. Linear / non saturation / unsaturated region.
3. Saturation region.

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1. cut off region:

This region is defined for $V_{GS} < V_{th}$ i.e., gate to source voltage is less than threshold voltage. Due to this channel is not established hence current flow between source and drain is zero. i.e., $I_{DS} = 0$. — 02 marks

① Cut off region:

This region is defined for gate to source voltages less than threshold voltage

i.e., $V_{GS} < V_{th}$.

In this region there is no channel enhancement between source to drain. Hence there is no current flow from drain to source.

→ 02 marks

Hence $I_{DS} = 0$.

~~② Linear region / non saturated / unsaturated~~

~~This region is defined~~

~~② Linear / non saturated / unsaturated region~~

As $V_{GS} > V_{th}$ and $V_{DS} > 0$.

i.e., Gate to source voltage greater than threshold voltage V_{th} and drain to source voltage greater than zero, channel is established and carriers start ~~moving~~ flowing from source to drain hence conventional current flows from drain to source

$$\therefore I_{DS} = -I_{SD} = \frac{\text{Charge induced in channel } (Q_c)}{\text{Electron transit time } (\tau)}$$

→ (1)

Transit time τ_{SD} = $\frac{\text{Length of the channel } (L)}{\text{velocity } (v)}$ → (2) (7)

velocity $v = \mu \mathcal{E}_{DS}$ → (3)

μ → mobility of carriers

$\mathcal{E}_{DS}$ → Electric field between drain to source.

$$\mathcal{E}_{DS} = \frac{V_{DS}}{L} \rightarrow (4)$$

V_{DS} = Voltage between drain to source

Substitute (4) in (3).

$\therefore$ (3) ⇒ $v = \frac{\mu V_{DS}}{L}$ → (5)

Substitute (5) in (2)

$\therefore$ (2) ⇒

$$\tau_{SD} = \frac{L}{\mu V_{DS}/L}$$

$$\tau_{SD} = \frac{L^2}{\mu V_{DS}} \rightarrow (6)$$

. 03 marks

Linear / non saturated region

Charge Induced in the channel due to gate to source voltage greater than threshold voltage

i.e., $V_{GS} > V_{th}$

Voltage in the channel varies linearly with distance from source due to IR drop in the channel

In linear region $V_{GS} - V_{th} > V_{DS}$.

At source end the voltage with in the channel is $V_{GS} - V_{th}$. That is drain effect due to. drain to source voltage at source end is completely zero.

As the distance from source increases towards drain region the drain to source voltage effects become significant.

So the average voltage within the channel is

$$V_q = \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \rightarrow (7)$$

Charge induced / unit area = $E_q \epsilon_{ox} = E_q \epsilon_{ins} \epsilon_0 WL$ ⑧

Total charge $Q_c = E_q \epsilon_{ox} WL = E_q \epsilon_{ins} \epsilon_0 WL$

E_q = Average electric field. gate to channel.

ϵ_{ox} = ~~relative~~ permitivity of gate oxide.

ϵ_{ins} = relative permitivity of insulator = 3.9.

ϵ_0 = permitivity of free space = 8.85×10^{-14} F/

t_{ox} = oxide thickness.

$$\therefore E_q = \frac{V_q}{t_{ox}} \rightarrow ⑧$$

using ⑦ in ⑧

$$E_q = \frac{\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)}{t_{ox}}$$

$$\therefore Q_c = \epsilon_{ox} WL \frac{\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)}{t_{ox}} \rightarrow ⑨$$

using ⑨ and ⑥ in ①

① ⇒

$$I_{DS} = \frac{\frac{\epsilon_{ox} WL}{t_{ox}} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)}{\frac{L^2}{\mu V_{DS}}}$$

$$I_{DS} = \mu \frac{\epsilon_{ox} WK}{L^2 t_{ox}} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) V_{DS}$$

$$\therefore \boxed{I_{DS} = \mu \frac{C_{ox}}{t_{ox}} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]} \text{ in amps}$$

where $\frac{C_{ox}}{t_{ox}} = C_{ox}$

$$\therefore \boxed{I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]} \text{ in amps} \quad -10$$

(3) Saturation region

0.3 marks

This region is defined for

$$V_{GS} > V_{th}$$

$$V_{DS} \geq V_{GS} - V_{th}.$$

For pinch off to occur $V_{DS} = V_{DSat} = V_{GS} - V_{th}$

using this result in (10)

we get

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{th})(V_{GS} - V_{th}) - \frac{(V_{GS} - V_{th})^2}{2} \right)$$

$$= \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{th})^2 - \frac{(V_{GS} - V_{th})^2}{2} \right)$$

$$= \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{th})^2}{2}$$

$$\boxed{I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2} \text{ in amps.}$$

0.2 marks

(5) Write a short notes on
(i) Differential inverter — 5 marks
(ii) Saturated load inverters. — 5 marks

→

(i) Differential inverter

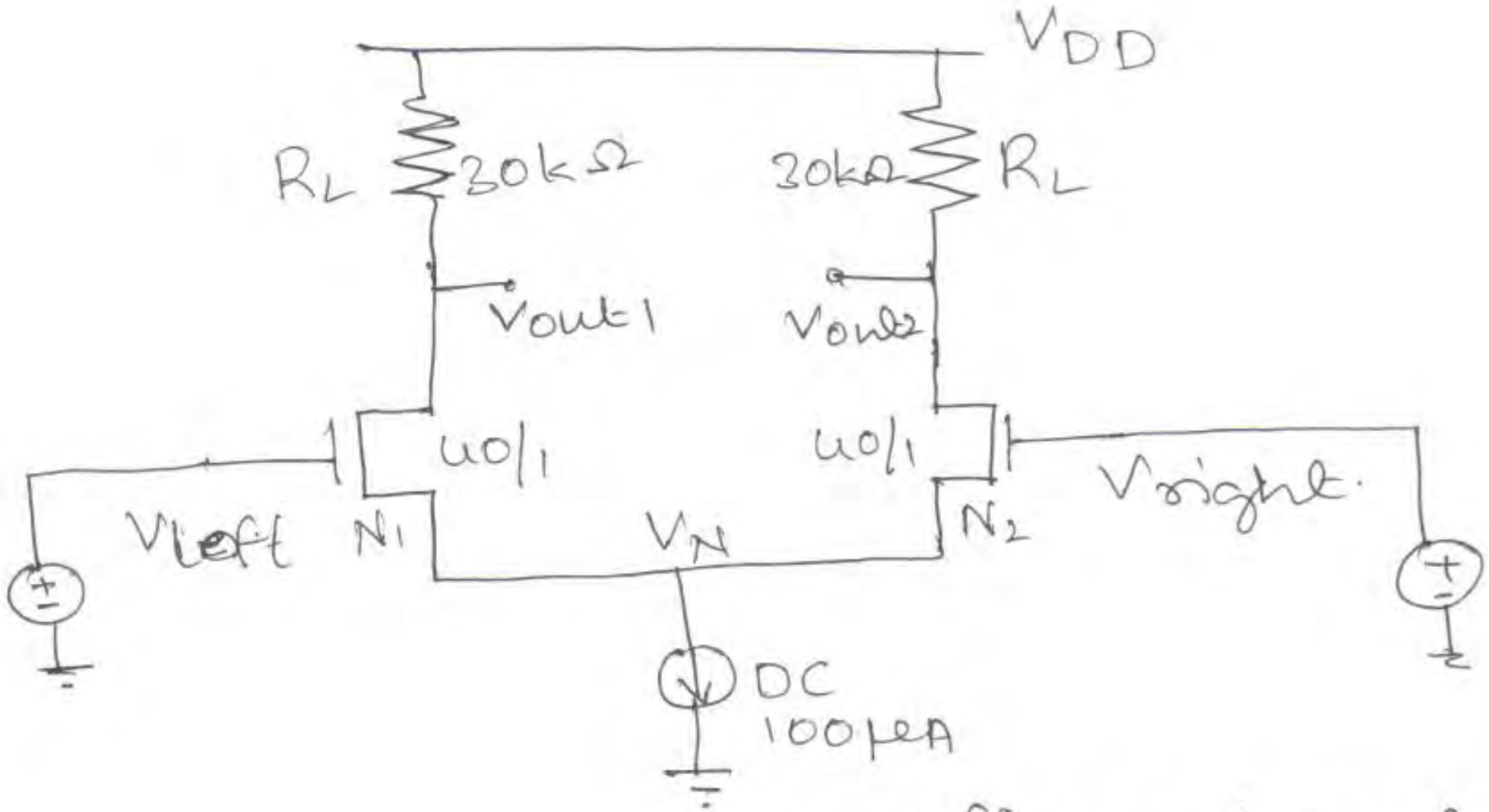


Fig 1: differential inverter circuit

An inverter that uses two differential inputs and produce two differential outputs is called differential inverter The circuit diagram is shown in figure 1. Which uses two resistive load, two nmos transistors whose source is commoned and connected to current source that is in turn connected to ground. Drains of two nMOS transistors connected to the resistors.

→ (Com)

1 mark

when V_{left}, V_{right} are set to same voltage $V_{quiscent}$ then each transistor has a V_{GS} of $V_{quiscent} - V_N$.

V_N is the voltage across current source

I_{DS} in each transistor is equal and $V_{out1} = V_{out2}$.

∴ Applying common signals to both inputs therefore. results in no gain. This gain is called common mode gain.

Diffrential mode gain: If V_{left} is raised by δV and V_{right} is lowered by δV, then current in N_1 increased by δI and current in N_2 will decrease by δI. V_{out1} decrease by δIR & V_{out2} increase by δIR.

∴ Diffrential gain from V_{left} to V_{out1} is

$$A_{diff} = \frac{2\delta IR}{2\delta V} = \frac{\delta IR}{\delta V}$$

$$\boxed{A_{diff} = -g_m R.}$$

Diffrential gain resulted from applying a diffrential signals to the inputs.

Common mode rejection ratio: It is the ratio of Common mode gain and diffrential gain.

$$CMRR = \frac{\text{Diffrencial gain}}{\text{Common mode gain.}}$$

— 3 marks

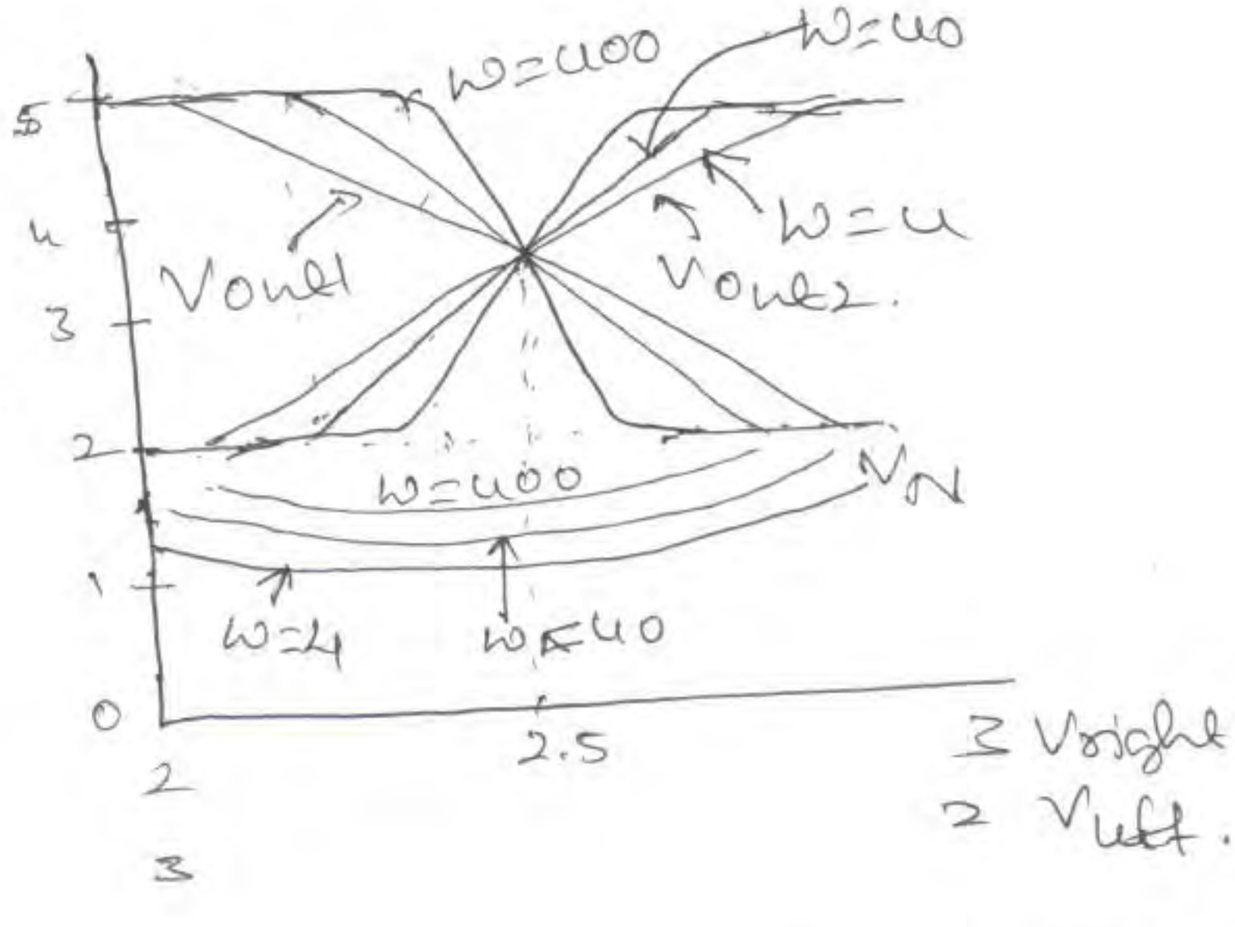


figure 2:- Input output characteristics of differential inverter.

Figure 2 shows the input output characteristics of differential inverter for different values of ~~total~~ channel widths of nMOSFET. — 1 mark

(ii) Saturated load inverters.

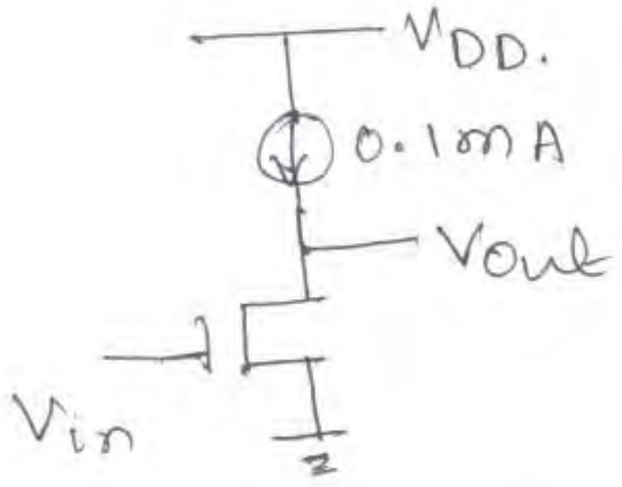


Fig 1. Generic circuit of saturated load inverter.

Saturated load inverter consists of an nMOS driver transistor whose gate is tied with input signal. The load is a constant current source as shown in figure ①.

— 01 mark

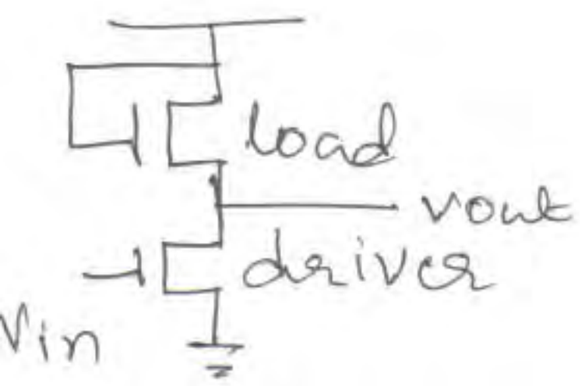


fig 2.

Figure 2 shows a saturation load inverter in which current source in figure ① @ is replaced by a nMos inverter whose gate is permanently connected to Drain. Hence load transistor operates in saturation region because $V_{DSload} > V_{GSload} - V_{thload}$. Output is always lowered by one threshold by V_{DD}. when $V_{in} < V_{thdriver}$.

The input output characteristics are as shown in figure ②.

It has small low noise margin makes this inverter nonoptimal as a conventional logic circuit.

Used whenever nMOS only circuits are preferred.

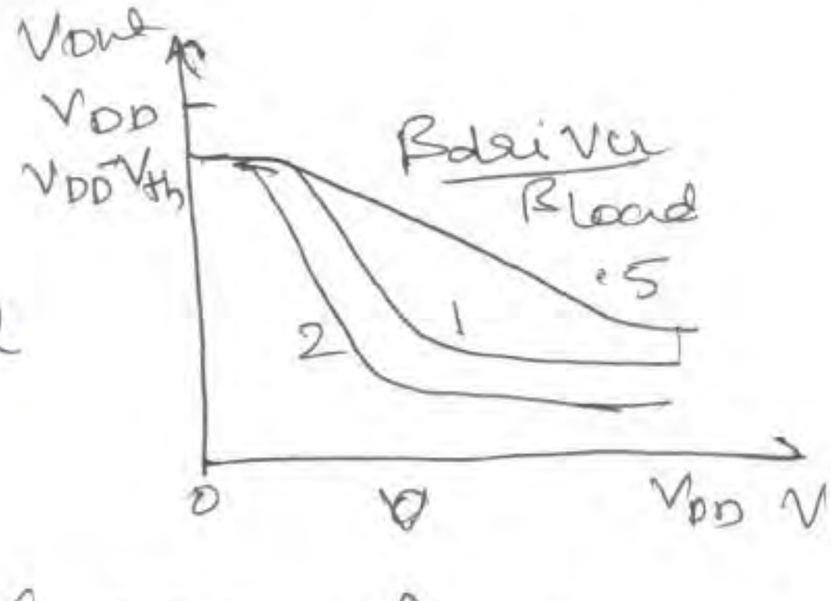


fig 2: Transfer characteristics

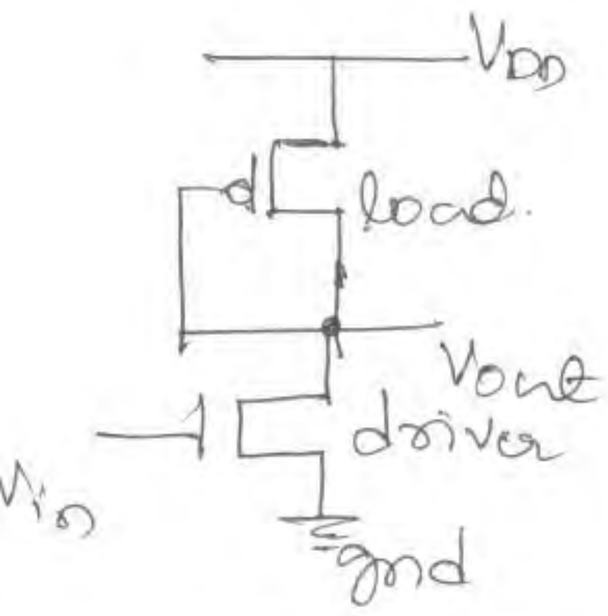
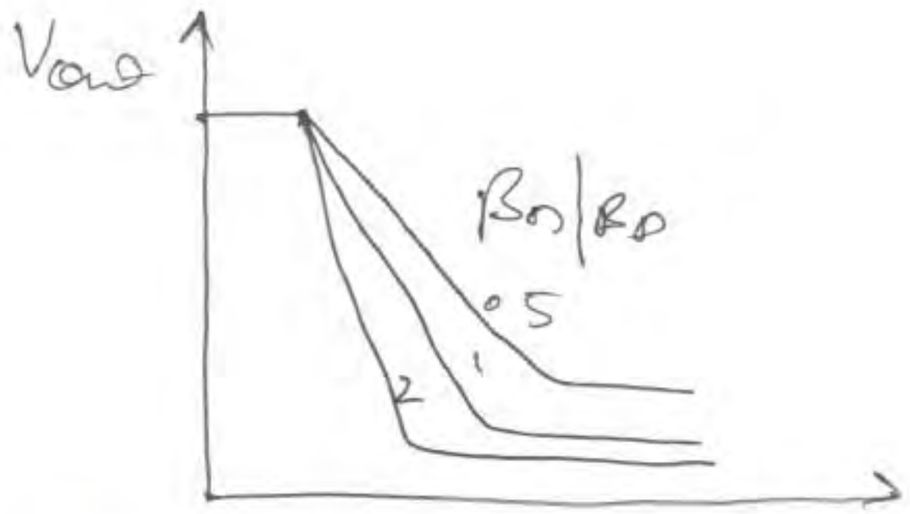


fig 3: ⓐ PMOS based saturated load inverter



ⓑ Transfer characteristics

Here PMOS transistor gate is connected to the output terminal. Output raises to a pthreshold ~~from V~~ drop from V_{DD}. PMOS is in saturation, ~~too~~ small V_{in} driver transistor is in saturation.

$$I_{DSdriver} = \frac{\beta_{driver}}{2}(V_{in} - V_{thn})^2$$

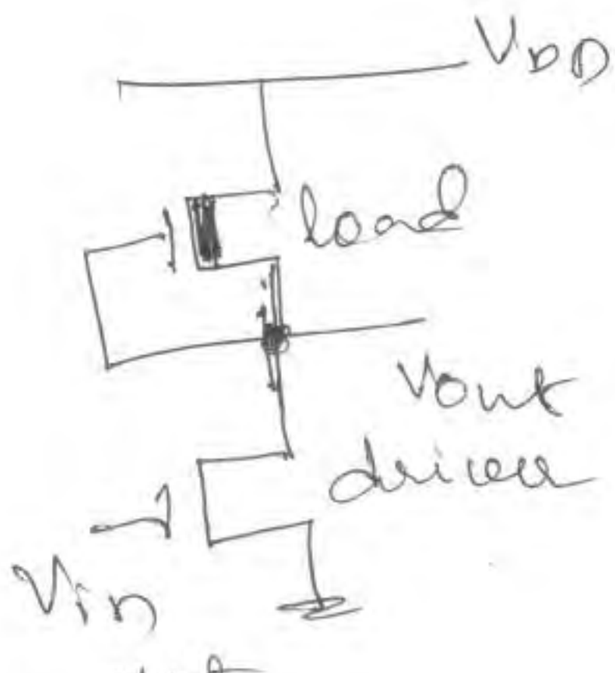
$$I_{DSload} = -\frac{\beta_{load}}{2}(V_{out} - V_{DD} - V_{tp})^2$$

~~VOW~~ $I_{DSload} = -I_{DSdriver}$

$$V_{out} = V_{DD} + V_{tp} + \sqrt{k}(V_{in} - V_{tn})$$

$$k = \frac{\beta_{driver}}{\beta_{load}}$$ — 02 marks

One more variant of saturated load inverter is as shown in fig 4. which uses depletion mode ~~load~~ nMOSas load whose gate is connected to the output terminal. Since threshold voltage is negative hence output raises to complete V_{DD} and close to zero. when V_{in} is zero and V_{DD} respectively as shown in figure 4(b).



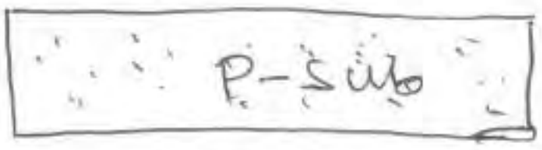
→ 2 marks

fig 4: Depletion load inverter.

⑥ Explain the nMOS fabrication process with neat sketches? write the steps involved in production of E-beam masks (7m+3m)

→ NMOS fabrication steps are outlined as bellows

①



Thin wafer cut from single crystal of silicon of high purity into which p type impurities are introduced. Thickness of the wafer is 0.4mm & a diameter of 75 to 150mm.

②

A layer of Silicon dioxide of thickness 1μm is grown to protect surface, acts as barrier to dopants during processing & provide insulating substrate onto which other layers to be deposited and patterned.

③ The A layer of photo resist is deposited onto the wafer and spun to achieve an even distribution of required thickness

④

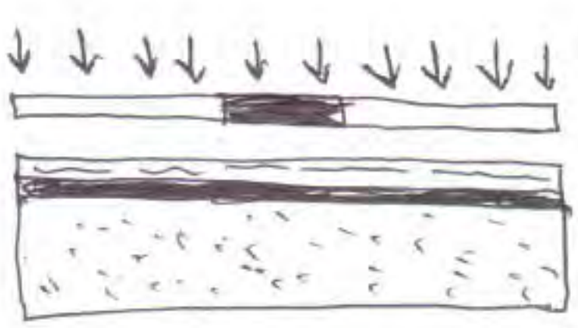


Photo resist layer ③ is then exposed to ~~ultra light~~ ultra violet light through a mask to define region into which diffusion take place along with its channel.

Exposed areas of photo resist is polymerized. Areas required for diffusion are shielded by the mask.

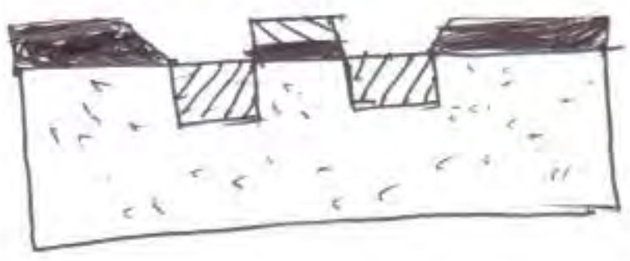
(5) Those

$ Subsequently the areas not exposed to UV light are etched away along with the underlying silicon dioxide so that a ~~window~~ wafer surface is exposed in the window defined by the mask. Remaining photo resist is removed.

(6)

A thin layer of silicon dioxide (0.1μm) is grown over entire chip and polysilicon is deposited on top to form gate structure. Polysilicon layer consists of heavily doped polysilicon deposited by chemical vapor deposition (CVD). Precise control of dopant concentration and thickness is necessary.

(7) Further photoresist and masking allows the polysilicon to be patterned as shown above. Then thin oxide is remove to expose areas into which n type impurites are to be diffused to form the source and drain as shown below.

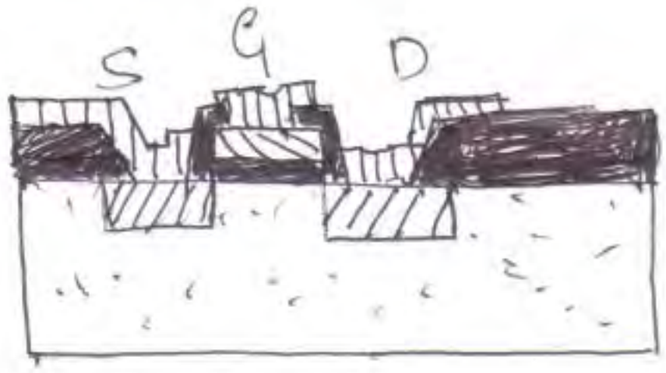


Diffusion is a process in which wafer is heated, ~~to a high~~ to a high temperature and passing a gas containing the desired n-type impurity over the surface. As Polysilicon with underlying thin oxide act as masks during diffusion process. This process is called self aligning.

(8)

Thick oxide grown allowed again, then masked with photoresist and etched to expose selected areas of polysilicon gate and the source and drain regions where connections are to be made.

(9)



Metal is then deposited over the surface to a thickness of 1 μm, this layer is then masked and etched to form the required interconnection pattern.

— 07 marks

Production of E-beam masks

① Starting material is chrome plated glass plate coated with E-beam sensitive resist.

② E-beam machine is loaded with mask description data (MEBES).

③ Plates are loaded into the E-beam machine where they are exposed with patterns specified by the customers mask data

④ After exposure to the ~~new~~ E-beam, the plates are introduced into the developer to bring out the the patterns left by the E-beam in the resist coating.

⑤ ~~Cycle~~ This cycle followed by bake cycles and plasma descumming. which removes the resist residue.

⑥ The chrome is then etched and the plate is stripped of the remaining, ~~remaining~~ E-beam resist.

— 08 marks

7) Explain the CMOS inverter transfer characteristics highlighting the region of operation of the MOS transistor. Derive the relationship between V_{in} and V_{out} for region C? Explain the effects of B_n/B_p ratio variations on the transfer characteristics of CMOS inverter.

[6M + 4M]

→

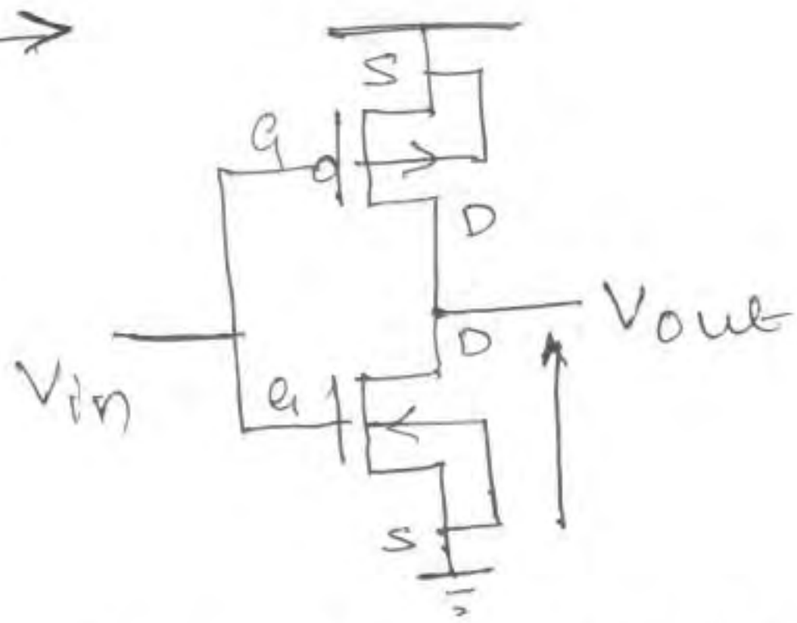
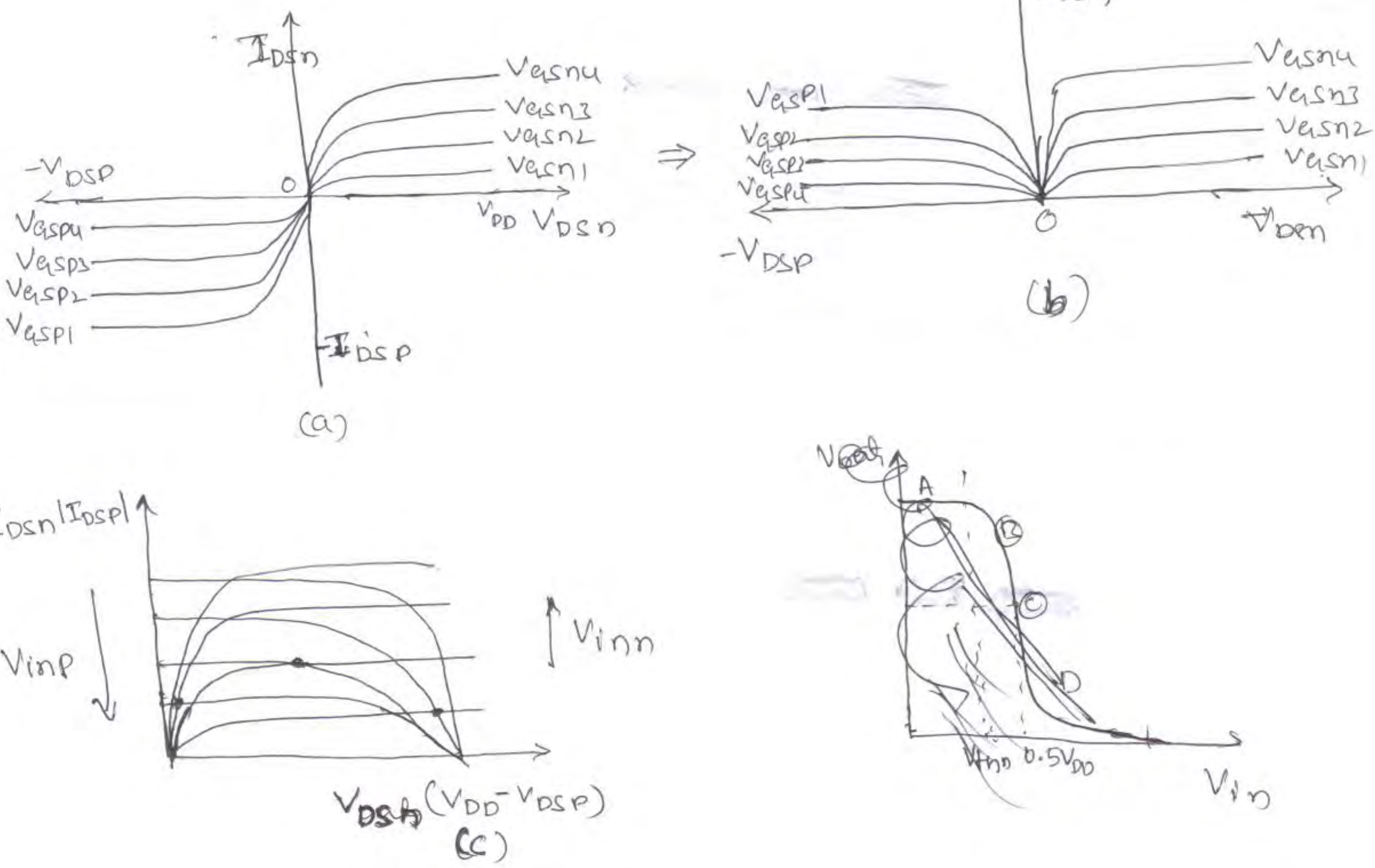
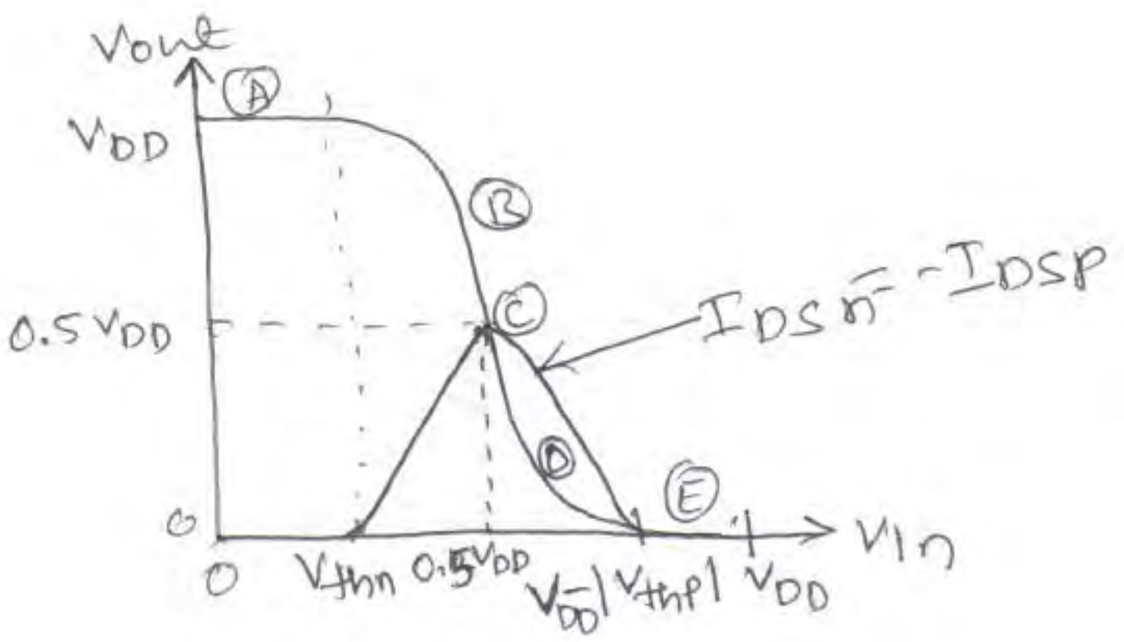


fig 1. CMOS inverter.

The circuit diagram of CMOS inverter is as shown in figure 1.





(d)

fig 2: Derivation of CMOS inverter characteristics

fig 2a shows the ~~output~~ graphical representations of the simple algebraic equations described below.

In linear region

$$I_{DSn} = \mu_n C_{ox} \frac{W}{L} \left((V_{GSn} - V_{thn}) V_{DSn} - \frac{V_{DSn}^2}{2} \right)$$

$$I_{DSp} = -\mu_p C_{ox} \frac{W}{L} \left((V_{GSp} - V_{thp}) V_{DSp} - \frac{V_{DSp}^2}{2} \right)$$

In saturation region

$$I_{DSn} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GSn} - V_{thn})^2$$

$$I_{DSp} = -\frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{GSp} - V_{thp})^2$$

In Cutoff region

$$I_{DSn} = 0 \; ; \; I_{DSp} = 0.$$

Fig 2b shows absolute value of the p-transistor drain current I_{DS} leads to inverting of P-device characteristics.

Fig 2c shows the superimposed curves of two transistor characteristics.

The input output transfer characteristics is determined by the ^Points of common Vgs intersection.

The intersection points in fig 2c for common V_{GS} gives the magnitude of current flowing in the circuit.

~~Before plotting the input o.~~

Figure 2D shows the resultant input output transfer characteristic of CMOS inverter.

Operation of CMOS Inverter is devided into 5 regions The state of ~~these~~ PMOS and nMOS in five regions is given below

Regions	nMOS	PMOS
A	cut off	linear
B	Saturation	linear
C	Saturation	Saturation
D	linear	saturation
E	linear	cut off

— OU marks.

Region C

We know that

$$I_{DSP} = -I_{DSn}$$

$$+\frac{\beta_P}{2}\left[V_{GSP} - V_{thP}\right)^2 = +\frac{\beta_n}{2}\left(V_{GSn} - V_{thn}\right)^2 \quad \rightarrow (1)$$

By ~~$V_{GSP} = V_{in} - V_{DD}$~~

$$V_{GSP} = V_G - V_S = V_{in} - V_{DD}$$

$$V_{GSn} = V_G - V_S = V_{in} - 0 = V_{in}.$$

① ⇒

$$\beta_p (v_{in} - v_{DD} - v_{thp})^2 = \beta_n (v_{in} - v_{thn})^2$$

$$\beta_p (v_{in} - v_{DD} - v_{thp})^2 = \beta_n (v_{thn} - v_{in})^2$$

$$(v_{in} - v_{DD} - v_{thp})^2 = \frac{\beta_n}{\beta_p} (v_{thn} - v_{in})^2$$

taking square root on both sides

$$v_{in} - v_{DD} - v_{thp} = \sqrt{\frac{\beta_n}{\beta_p}} (v_{thn} - v_{in})$$

$$v_{in} + \sqrt{\frac{\beta_n}{\beta_p}} v_{in} = \sqrt{\frac{\beta_n}{\beta_p}} v_{thn} + v_{DD} + v_{thp}$$

$$\boxed{v_{in} = \frac{v_{DD} + v_{thp} + \sqrt{\frac{\beta_n}{\beta_p}} v_{thn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}}$$

By setting $\beta_n = \beta_p$ and $v_{thn} = -v_{thp}$

$$v_{in} = \frac{v_{DD} + v_{thp} + \left(\sqrt{\frac{\beta_n}{\beta_n}} \cdot -v_{thp}\right)}{1 + \sqrt{\frac{\beta_n}{\beta_n}}}$$

$$\boxed{v_{in} = \frac{v_{DD}}{2}}$$

Region c exists only for one point.

Possible ranges of output voltage V_{out} for NMOS FET, $V_{GSn} - V_{thn} \le V_{DSn}$

for PMOS: $V_G - V_{thn} \ge V_{DD}$ -

Possible range of V_{out}

for nMOSFET:

$$V_{GSn} - V_{thn} < V_{DSn}$$

$$V_G - V_S - V_{thn} < V_D - V_S$$

$$V_{in} - V_{thn} < V_{out} \quad \text{— (2)}$$

for PMOSFET

$$V_{GSP} - V_{thP} > V_{DSP}$$

$$V_G - V_S - V_{thP} > V_D - V_S$$

$$V_{in} - V_{thP} > V_{out} \quad \rightarrow (3)$$

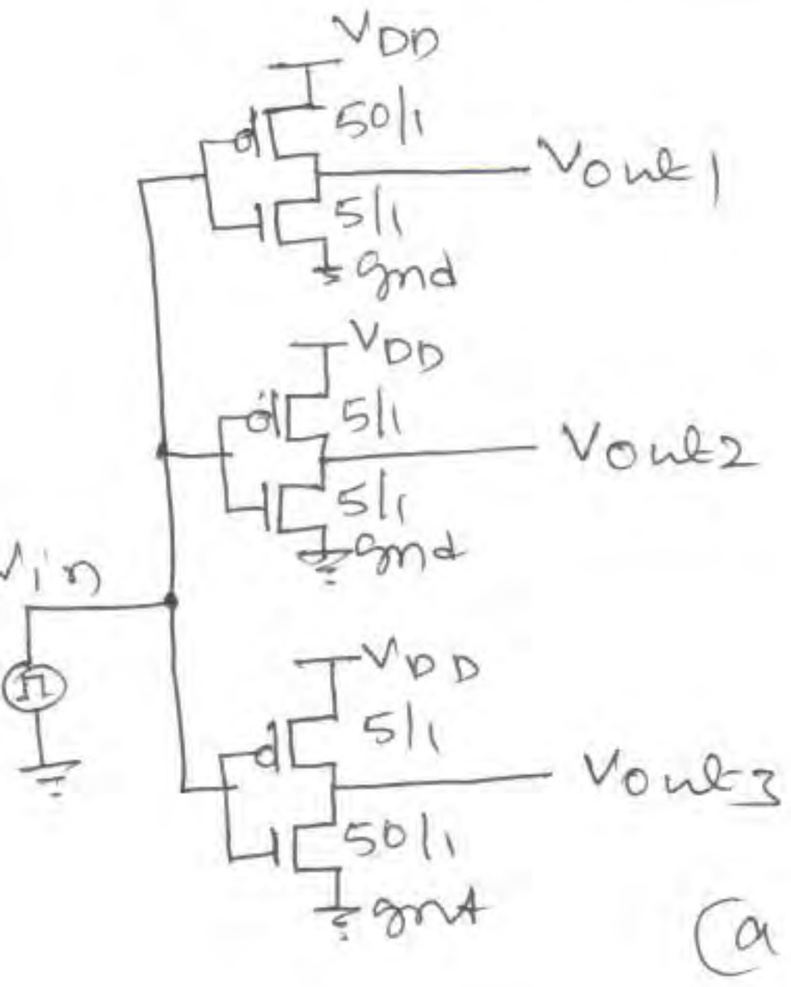
Using (2) and (3)

$$V_{in} - V_{thn} < V_{out} < V_{in} - V_{thP}$$

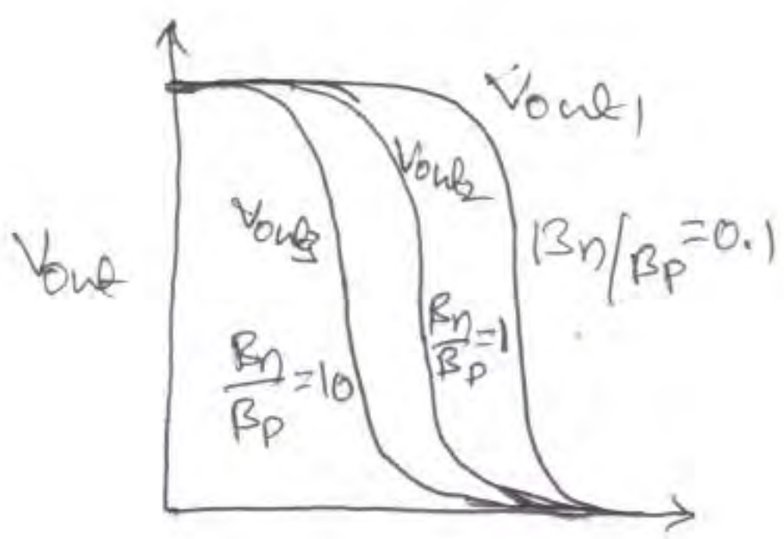
Region (C) point is also called as inverter threshold denoted by V_{inv}

——— 02 marks

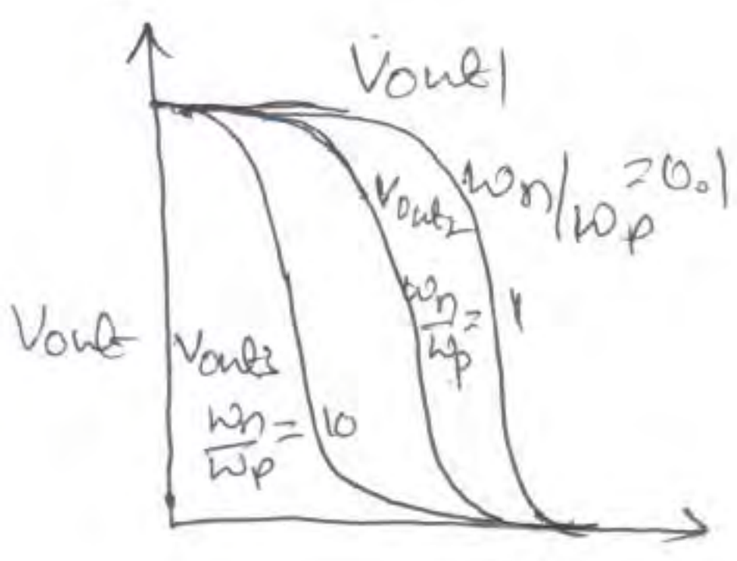
B_n/B_p Variations



(a)



(b)



(c)

figure 3: circuit diagram & influence of B_n/B_p on DC Transfer characteristic.

Gate threshold voltag V_{inv} depends on β_n/β_p
This is evident from figure 3(b) & (c).
As β_n/β_p increases V_{inv} at which $V_{in} = V_{out}$ decreases.

$\frac{\beta_n}{\beta_p}$ can be changed by changing the device dimensions

Variations in DC transfer characteristics dece to variations in β_n/β_p and hence dec to variation in $\frac{W_n}{W_p}$ is shown in figure 3(b) and (c).

~~with $\frac{\beta_n}{\beta_p} = 1$, allows inverter to have equal with a capacitive load to charge and discharge in equal times by providing equal current-source and current-sink capabilities.~~

when $\frac{\beta_n}{\beta_p} = 1$, allows the inverter to charge and discharge the capacitive load in equal times by providing equal current source and current-sink capabilities.

when $\frac{\beta_n}{\beta_p} > 1$ allows the inverter to have more current sinking capability than current sourcing capability

when $\frac{\beta_n}{\beta_p} < 1$ inverter will have high current sourcing capability than current sinking capability. 01 marks

As the temperature ~~increases~~ of the MOS device increases the effective carrier mobility μ decreases. This results in a decrease in β. They are related as

~~$\beta \propto T^{-1.5}$~~ $\mu \propto T^{-1.5}$

~~$\therefore \mu \propto T$~~ $\therefore \beta \propto T^{-1.5}$ 01 marks

$\therefore I_{DS} \propto T^{-1.5}$

Mobility of both holes and electrons are similarly affected this ratio is independent of temperature to a good approximation.

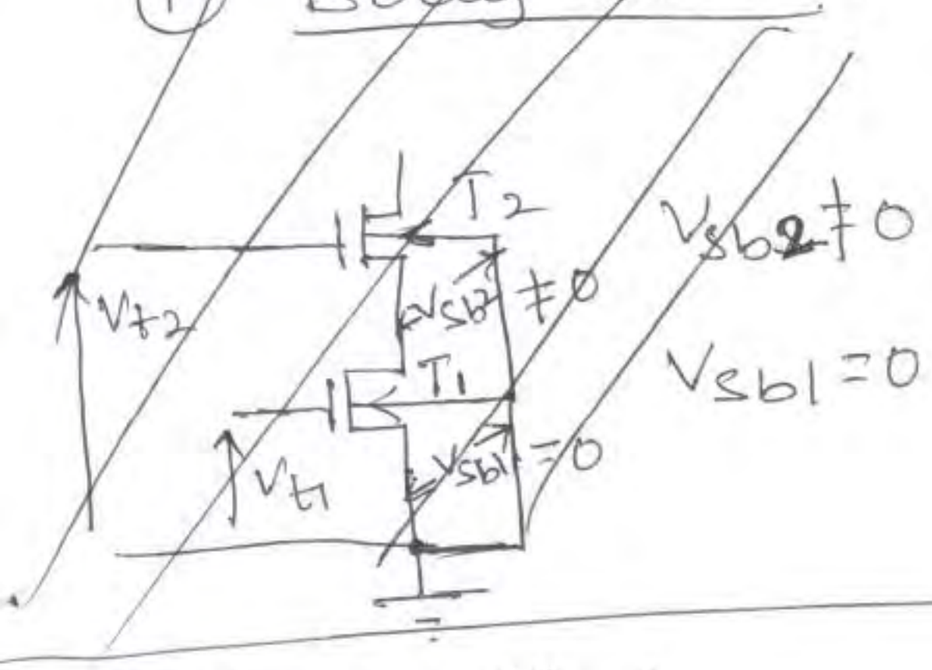
Both V_{thn} and V_{thp} decrease slightly as temperature increases, and the extent of region A is reduced while the extent of Region E increases.

— 01 marks

⑧ Write a short notes on (i) Body effect. (ii) channel length modulation

— (5M+5M)

(i) Body effect:



(i) Body effect.

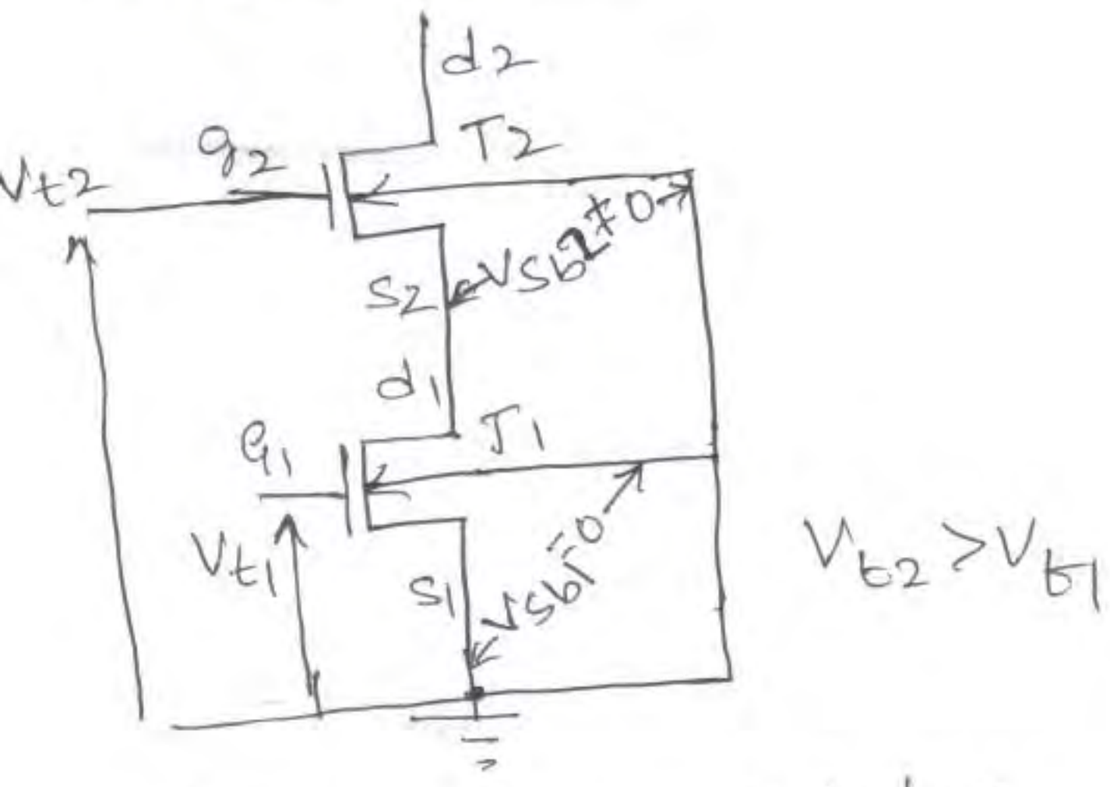


Fig 1: Effect of substrate bias on series connected n transistors.

All the devices are formed on a single substrate. Therefore substrate voltage is normally equal.

In some cases while arranging the transistors to form a gating functions it might be necessary to connect

several devices in series as shown in figure (1) for example a NAND gate.

These source to substrate voltage for T_1 transistor is zero where as for T_2 it is is not zero

i.e., $V_{sb1} = 0$ for T_1

& $V_{sb2} \neq 0$ for T_2.

Due to the non zero V_{sb}, as V_{sb} increases the width of the channel-substrate depletion layer also increases. resulting in an increase in the density of the trapped carriers in depletion layer. For charge neutrality to hold, channel charge must decrease. Results in increase in the gate-channel voltage drop leads to increase in threshold voltage V_{th} since V_{sb} adds to the channel substrate junction potential.

∴ The modified threshold voltage expression is

$$V_{thb} = V_{fb} + 2\phi_b + \frac{\sqrt{2\epsilon_{si} q N_A (2\phi_b + |V_{sb}|)}}{C_{ox}}$$

$$V_t = V_{tho} + \gamma \left(\sqrt{2\phi_b + |V_{sb}|} - \sqrt{2\phi_b} \right).$$

V_{tho} = threshold voltage with source to substrate voltage $V_{sb} = 0$.

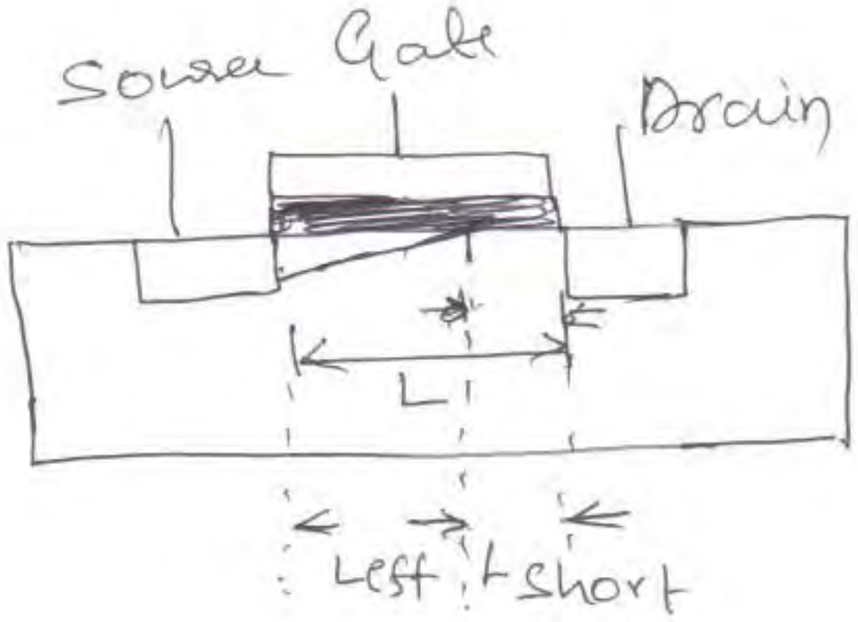
γ = constant describes substrate bias effect.

$$\gamma = \frac{t_{ox}}{\epsilon_{ox}} \sqrt{2 q \epsilon_{si} N_A} = \frac{1}{C_{ox}} \sqrt{2 q \epsilon_{si} N_A}$$

——— 05 marks

~~(b)~~

(ii) channel length modulation.



As devices are scaled down, variations in drain to source voltage leads to variation in the effective length of the channel. This is called as channel length modulation.

Ideally the drain to source current I_{DS} in saturation region should be independent of V_{DS}. But as devices are scaled down I_{DS} depends on V_{DS}. variations in V_{DS} as given by

$$I_{DS} = \frac{k}{2}\frac{w}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})$$

λ = channel length modulation factor

varies has value in the range 0.02 V^{-1} to 0.05 V^{-1}

k = process gain factor = $\frac{\mu\varepsilon}{t_{ox}}$

Effective channel length is

$$L_{eff} = L - L_{short}$$

$$L_{short} = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_{DS}-(V_{GS}-V_{th}))}$$

~~Since~~

Thus rather than appearing as a constant current source with infinite output impedance, MOS device has finite output impedance.

— 05 marks