

Internal Assessment Test - II

Sub:	DSP ALGORITHMS AND ARCHITECTURE	Code:	10EC751
Date:	04 / 11 / 2016	Duration:	90 mins
		Max Marks:	50
		Sem:	VII
		Branch:	ECE A & C

Answer ALL Questions

OBE  
Marks CO RBT

1 (a) Describe the operation of the following instructions.

[04] CO3 L2

- i) MPY 13, B
- ii) ADD \*AR3, A
- iii) MPY \*AR2-, \*AR4+0, B
- iv) SUBS \*AR2-, B

(b) Complete FIG.1 for the instruction:

[03] CO3 L3

SUB \*AR1+, 14, A

	Before Instruction		After Instruction
A	00 0000 1200	A	
C		C	
SXM	1	SXM	
AR1	0100	AR1	
<b>Data Memory</b>			
0100h	1500	0100h	

Fig.1

(c) The correct instruction which loads accumulator B using indirect addressing mode (AR3) and fetches the operand after incrementing the address by constant 8h is:

[02] CO3 L2

- i) LD \*+AR3(8), B
- ii) LD \*AR3(8), B
- iii) LD \*+AR3(8)%, B
- iv) LD AR3\*(8), B

2 (a) Differentiate between direct and indirect addressing modes.

[03] CO3 L2

(b) The instruction for shifting accumulator B by 8 bits towards left and adding it to accumulator A is \_\_\_\_\_

[02] CO3 L2

3 (a) Explain the following assembler directives of TMS320C54XX processors:

[04] CO4 L2

- i) .mmregs
- ii) .include'xx'
- iii) .data
- iv) .bss

(b) Which of the following instruction formats given below are correct?

[02] CO3 L2

- i) LD #1, A

- ii) LD #ACh, B
- iii) LD #255, B
- iv) LD #3Fh, B

4 (a) The initial values of AR1, AR3 and A are 84,81, and 1, respectively. [10] CO3 L3  
 The values stored in memory location 81,82,83 and 84 are 2,3,4 and 6, respectively.

Using pipeline operation table, give the values of registers AR3, AR1, T & accumulator A, after completion of each cycle, for the instructions:

```
ADD *AR3+, A
LD *AR1+, T
MPY *AR3+, B
ADD B, A
```

5 (a) Describe the steps required to load the accumulator with the contents of data [05] CO3 L3  
 memory address 310h. Use Table.1.

**Data Memory Addresses of the TMS320C541**

Pages	Available Addresses (Decimal)	Available Addresses (Hexadecimal)
0	96 to 127	60h to 7Fh
1	128 to 255	80h to FFh
2	256 to 383	100h to 17Fh
3 to 38	384 to 4991	180h to 137Fh
39	4992 to 5119	1380h to 13FFh

Table.1

6 (a) What is the advantage of using Q notation? Give an example. [02] CO4 L1

(b) Find the Q15 representation for the following numbers [02] CO4 L2  
 i) 0.560123  
 ii) - 0.160123

(c) Write an assembly language program for tms320c54xx processors to multiply [05] CO4 L2  
 two Q15 numbers to produce Q15 result


7 (a) What is an interpolation filter? [03] CO4 L1

(b) Why are poly-phase sub-filters used? [03] CO4 L1

Course Outcomes		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1:	Apply basic signal processing concepts in sampling, discrete sequences, DFT, FFT and digital filters. Explain basic DSP architecture and computational blocks.	3	0	3	0	0	0	0	0	0	0	0	0
CO2:	Explain bus architecture digital signal processors, memory and data addressing modes, individual architectural blocks and features for external interfacing.	2	0	3	0	0	0	0	0	0	0	0	0
CO3:	Explain the differences in commercial DSP devices, addressing modes and memory space specifically for TMS320c54xx, program control, instructions, programming and pipeline operations	3	0	3	0	0	0	0	0	0	0	0	0
CO4:	Use the instruction and code basic algorithms for FIR, IIR filters and FFT. Explain and apply Q-notation. Apply algorithms for overflow and scaling and bit-reversed indexing on TMS320c54xx	3	2	3	2	0	0	0	0	0	0	0	0
CO5:	Develop algorithms for accessing interrupts interfacing peripherals, external buses.	3	2	3	3	0	0	0	0	0	0	0	0
CO6:	Develop and analyze algorithms for DSP bio-telemetry receivers, speech processing and image processing.	3	2	3	3	0	0	0	0	0	0	0	0

Cognitive level	KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PO1 - *Engineering knowledge*; PO2 - *Problem analysis*; PO3 - *Design/development of solutions*; PO4 - *Conduct investigations of complex problems*; PO5 - *Modern tool usage*; PO6 - *The Engineer and society*; PO7- *Environment and sustainability*; PO8 - *Ethics*; PO9 - *Individual and team work*; PO10 - *Communication*; PO11 - *Project management and finance*; PO12 - *Life-long learning*

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1 (a)	Describe the operation of the following instructions. i) B = TREG*13 ii) Add the value contained in data memory address pointed to by AR3 to accumulator A iii) B = AR2 x AR4, T=AR2-1, AR4=AR4+AR0 iv) B = B-UNS(AR2), AR2=AR2-1						[04]	CO3	L2																												
(b)	<p>SUB *AR1+, 14, A</p> <table border="0" style="width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;">Before Instruction</th> <th colspan="2" style="text-align: center;">After Instruction</th> </tr> </thead> <tbody> <tr> <td>A</td> <td><input type="text" value="00 0000 1200"/></td> <td>A</td> <td><input type="text" value="FF FAC0 1200"/></td> </tr> <tr> <td>C</td> <td><input type="text" value="x"/></td> <td>C</td> <td><input type="text" value="0"/></td> </tr> <tr> <td>SXM</td> <td><input type="text" value="1"/></td> <td>SXM</td> <td><input type="text" value="1"/></td> </tr> <tr> <td>AR1</td> <td><input type="text" value="0100"/></td> <td>AR1</td> <td><input type="text" value="0101"/></td> </tr> <tr> <td colspan="2">Data Memory</td> <td colspan="2"></td> </tr> <tr> <td>0100h</td> <td><input type="text" value="1500"/></td> <td>0100h</td> <td><input type="text" value="1500"/></td> </tr> </tbody> </table> <p style="text-align: center;">Fig.1</p>						Before Instruction		After Instruction		A	<input type="text" value="00 0000 1200"/>	A	<input type="text" value="FF FAC0 1200"/>	C	<input type="text" value="x"/>	C	<input type="text" value="0"/>	SXM	<input type="text" value="1"/>	SXM	<input type="text" value="1"/>	AR1	<input type="text" value="0100"/>	AR1	<input type="text" value="0101"/>	Data Memory				0100h	<input type="text" value="1500"/>	0100h	<input type="text" value="1500"/>	[03]	CO3	L3
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2 (a)	Differentiate between direct and indirect addressing modes. <b>Direct addressing</b> uses seven bits of the instruction to encode an offset relative to DP or to SP. The offset plus DP or SP determine the actual address in data memory. <b>Indirect addressing</b> uses the auxiliary registers to access memory						[03]	CO2	L2																												
(b)	ADD B, 8, A						[02]	CO3	L2																												
3 (a)	i) .mmregs <ul style="list-style-type: none"> <li>Permits the memory mapped registers to be referred using names ARx, SP etc.</li> </ul> ii) .include'xx' <ul style="list-style-type: none"> <li>Informs the assembler to insert a list of instructions in the file xx to be inserted for assembly</li> </ul> iii) .data <ul style="list-style-type: none"> <li>Assemble into data memory area</li> </ul> iv) .bss						[04]	CO4	L2																												

	<ul style="list-style-type: none"> <li>Used to reserve a block of memory which is uninitialized</li> </ul>																																																																																																																	
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4 (a)	<p>The initial value of AR1, AR3, A are 84,81,1 &amp; the values stored in memory location 81,82,83,84 are 2,3,4,6.</p> <p>Using pipeline operation table, give the values of registers AR3, AR1, T &amp; accumulator A, after completion of each cycle, for the instructions:</p> <p>ADD *AR3+, A  LD *AR1+, T  MPY *AR3+, B  ADD B, A</p> <table border="1"> <thead> <tr> <th>Cycle</th> <th>Pre-fetch</th> <th>Fetch</th> <th>Decode</th> <th>Access</th> <th>Read</th> <th>Exec &amp; Write</th> <th>AR3</th> <th>AR1</th> <th>A</th> <th>T</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>ADD</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>81</td> <td>84</td> <td>1</td> <td>X</td> </tr> <tr> <td>2</td> <td>LD</td> <td>ADD</td> <td></td> <td></td> <td></td> <td></td> <td>81</td> <td>84</td> <td>1</td> <td>X</td> </tr> <tr> <td>3</td> <td>MPY</td> <td>LD</td> <td>ADD</td> <td></td> <td></td> <td></td> <td>81</td> <td>84</td> <td>1</td> <td>X</td> </tr> <tr> <td>4</td> <td>ADD</td> <td>MPY</td> <td>LD</td> <td>ADD</td> <td></td> <td></td> <td>82</td> <td>84</td> <td>1</td> <td>X</td> </tr> <tr> <td>5</td> <td></td> <td>ADD</td> <td>MPY</td> <td>LD</td> <td>ADD</td> <td></td> <td>82</td> <td>84</td> <td>1</td> <td>X</td> </tr> <tr> <td>6</td> <td></td> <td></td> <td>ADD</td> <td>MPY</td> <td>LD</td> <td>ADD</td> <td>83</td> <td>85</td> <td>03</td> <td>06</td> </tr> <tr> <td>7</td> <td></td> <td></td> <td></td> <td>ADD</td> <td>MPY</td> <td>LD</td> <td>83</td> <td>85</td> <td>03</td> <td>06</td> </tr> <tr> <td>8</td> <td></td> <td></td> <td></td> <td></td> <td>ADD</td> <td>MPY</td> <td>83</td> <td>85</td> <td>03</td> <td>06</td> </tr> <tr> <td>9</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>ADD</td> <td>83</td> <td>85</td> <td>15h</td> <td>06</td> </tr> </tbody> </table>	Cycle	Pre-fetch	Fetch	Decode	Access	Read	Exec & Write	AR3	AR1	A	T	1	ADD						81	84	1	X	2	LD	ADD					81	84	1	X	3	MPY	LD	ADD				81	84	1	X	4	ADD	MPY	LD	ADD			82	84	1	X	5		ADD	MPY	LD	ADD		82	84	1	X	6			ADD	MPY	LD	ADD	83	85	03	06	7				ADD	MPY	LD	83	85	03	06	8					ADD	MPY	83	85	03	06	9						ADD	83	85	15h	06	[10]	CO3	L3
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	<p style="text-align: center;">Fig.2</p> <ol style="list-style-type: none"> <li>1. To calculate the page number we need to divide 310h (784) by 80h (128) and round down to the nearest whole number.</li> <li>2. This gives us page number 6, which starts at address 718 (300h).</li> <li>3. We then add the offset supplied by the operand.</li> </ol> <p>LD #6, DP ; Set data memory page pointer to page 6. This gives us access to data memory addresses 300h to 37Fh.</p> <p>LD 10h, A ; Load accumulator A with the contents of data memory address 300h + 10h = 310h.</p>			
6 (a)	What is the advantage of using Q notation? Give an example.	[02]	CO4	L1
(b)	<p>Find the Q15 representation for the following numbers</p> <ol style="list-style-type: none"> <li>i) 0.560123 <ol style="list-style-type: none"> <li>a. <math>0.560123 \times 32768 = 18354 = 47B2h</math></li> </ol> </li> <li>ii) -0.160123 <ol style="list-style-type: none"> <li>a. <math>0.160123 \times 32768 = 5246 = 147Eh</math></li> <li>b. 2's complement of 147Eh = EB82</li> </ol> </li> </ol>	[02]	CO4	L2
(c)	<p>Write an assembly language program for tms320c54xx processors to multiply two Q15 numbers to produce Q15 result</p> <pre> .mmregs .data N1 .word 4000h N2 .word 2000h N1xN2 .space 10h .text .ref .global_main .sect ".vectors" RESET b .global_main Nop Nop .global_main: stm #N1,AR2 ld *AR2+,T mpyr *AR2+,A sth A,1,*AR2 nop nop .end </pre>	[05]	CO4	L2
7 (a)	<p>What is an interpolation filter?</p> <p>An interpolation filter is used to increase the sampling rate. The interpolation process involves inserting samples between the incoming samples to create additional samples to increase the sampling rate for the output. One way to implement an interpolation filter is to first insert zeros between samples of the original sample sequence. The zero-inserted sequence is then passed through an appropriate low-pass digital FIR filter to generate the interpolated sequence.</p>	[03]	CO4	L1

(b)	Why are poly-phase sub-filters used? In interpolation filter there are many multiplies in which one of the multiplying elements is zero. Such multiplies need not be included in computation if the computation is rearranged to take advantage of this fact. One such scheme, based on generating what are called polyphase subfilters, is available for reducing the computation	[03]	CO4	L1
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CO4:	Use the instruction and code basic algorithms for FIR, IIR filters and FFT. Explain and apply Q-notation. Apply algorithms for overflow and scaling and bit-reversed indexing on TMS320c54xx	3	2	3	2	0	0	0	0	0	0	0	0
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CO6:	Develop and analyze algorithms for DSP bio-telemetry receivers, speech processing and image processing.	3	2	3	3	0	0	0	0	0	0	0	0

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