10EC56

FUNDAMENTAL OF CMOS VLSI DESIGN

IAT2 SOLUTION 2016-17

DEPARTMENT OF ECE

CMRIT

CMR INSTITUTE OF TECHNOLOGY

USN | | | | | | | | | | |

Internal Assesment Test - II

Sub:	Fundamental of CMOS design							Code:	10EC55
Date:	03 / 10/ 2016	Duration:	90 mins	Max Marks:	50	Sem:	5	Branch:	ECE/TCE (All sec)

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	List and explain the λ-based design rules for PMOS, NMOS and CMOS logic designs	[10]	CO1	L1
2	Draw the Schematic circuit, stick diagram & layout for $y = A\bar{B} + ABC$ using CMOS design.	[10]	CO2	L3
3 (a)	Describe domino CMOS logic? How does it eliminate the issues related to cascading?	[05]	CO3	L2
(b)	Discuss the merits and demerits of Pseudo NMOS logic of 'NAND' gate.	[05]	CO3	L2
4	Explain the working principle of dynamic CMOS logic and clocked CMOS logic. Give their merits and demerits	[10]	CO3	L4
5	Discuss bus arbitration logic for n-line bus.	[10]	CO4	L2
6 (a)	Discuss the architectural issues to be followed in the design of a VLSI subsystem.	[05]	CO4	L2
(b)	Explain two-phase clock signal generator using D flip-flops.	[05]	CO5	L4

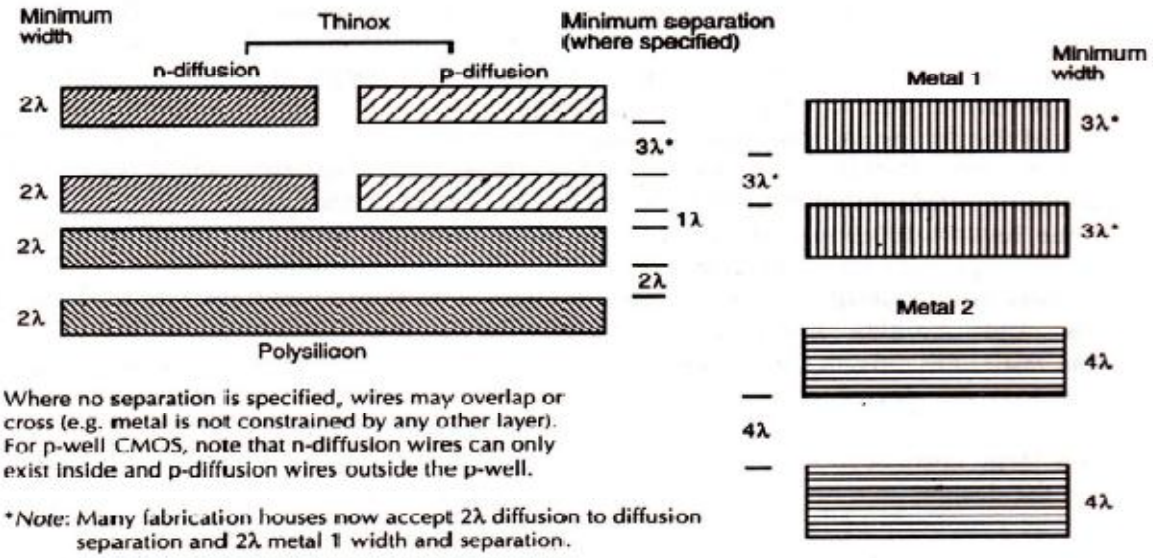
Course Outcomes		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1:	Summarize the concepts of MOSFET associated with transistor design.	3	3	-	-	-	-	-	-	-	1	-	-
CO2:	Relate the circuit design using Separate models of Stick diagrams and layouts	3	3	-	-	-	-	-	-	-	1	-	-
CO3:	Explain different model developments and connect different logic structures.	3	3	-	-	-	-	-	-	-	1	-	-
CO4:	Apply sub system design using leaf cells to make structured design for high regularity of VLSI systems	3	3	-	-	-	-	-	-	-	1	-	-
CO5:	Design memory modules with clocking strategy using different approaches and methodologies	3	3	-	-	-	-	-	-	-	1	-	-
CO6:	Describe the concept of testing and layout mapping	3	3	-	-	-	-	-	-	-	1	-	-

Cognitive level	KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PO1 - *Engineering knowledge*; PO2 - *Problem analysis*; PO3 - *Design/development of solutions*; PO4 - *Conduct investigations of complex problems*; PO5 - *Modern tool usage*; PO6 - *The Engineer and society*; PO7- *Environment and sustainability*; PO8 – *Ethics*; PO9 - *Individual and team work*; PO10 - *Communication*; PO11 - *Project management and finance*; PO12 - *Life-long learning*

1. List and explain the λ-based design rules for PMOS, NMOS and CMOS logic designs.

Design Rules for wires:- nMOS and CMOS



① Minimum width of n-diffusion is - 2λ

Minimum width of p-diffusion is - 2λ.

Minimum separation between two diffusion layers is 3λ.

Minimum separation between polysilicon and diffusion layer is 1λ.

Minimum width of polysilicon layer is 2λ.

Minimum separation between two polysilicon layer is 2λ.

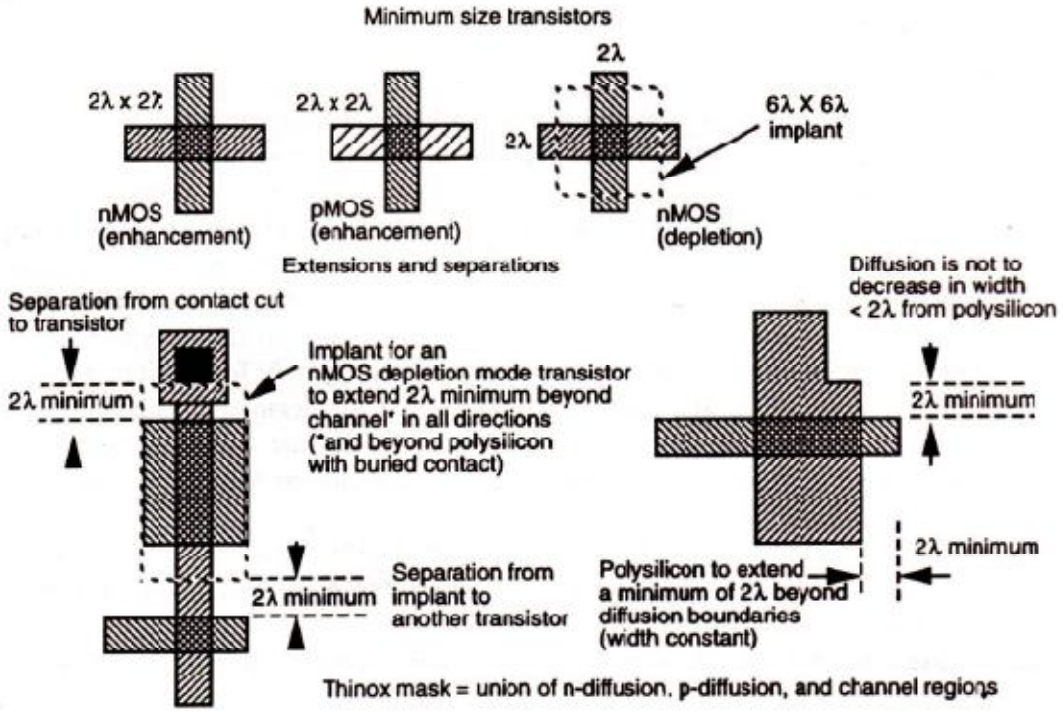
Minimum width of metal 1 is 3λ.

Minimum separation between 2 metal 1 layers is 3λ.

Minimum width of metal 2 is 4λ.

Minimum separation between 2 metal 2 layers is 4λ.

Design Rules for Transistors :- nMOS and CMOS



Implant layer size is 6λ×6λ and placed around the intersection of polysilicon and diffusion.

Extension of implant from channel is 2λ.

Separation from implant to another transistor is 2λ.

Extension of polysilicon beyond channel is 2λ

Extension of diffusion beyond channel is 2λ.

2. Apply the Schematic circuit, stick diagram & layout for $y = \bar{A}\bar{B} + ABC$ using CMOS design.

$y = \bar{A}\bar{B} + ABC$

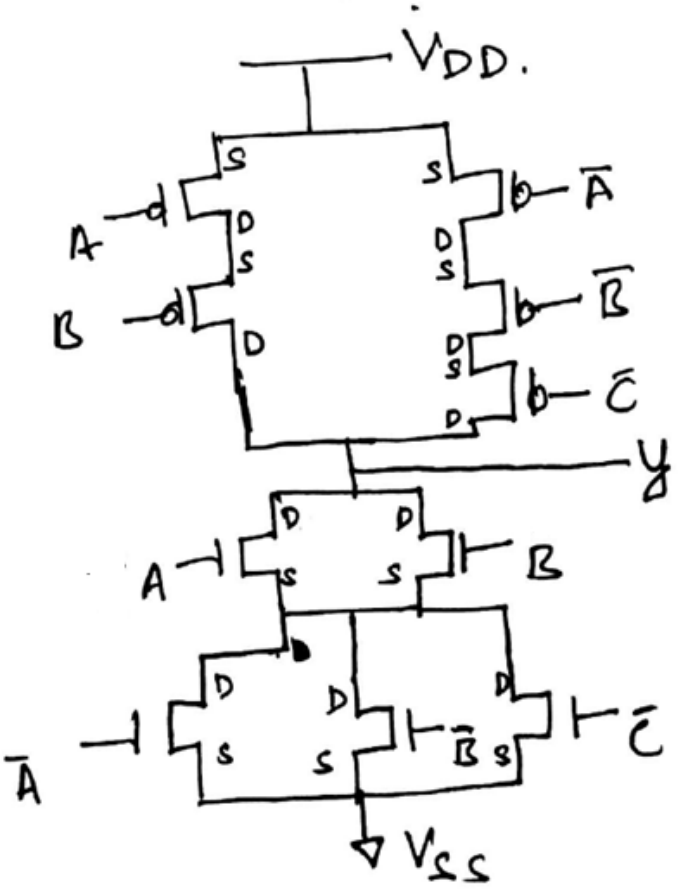
Use ~~dem~~ Demorgans theorem

$$y = \overline{\overline{\bar{A}\bar{B} + ABC}}$$

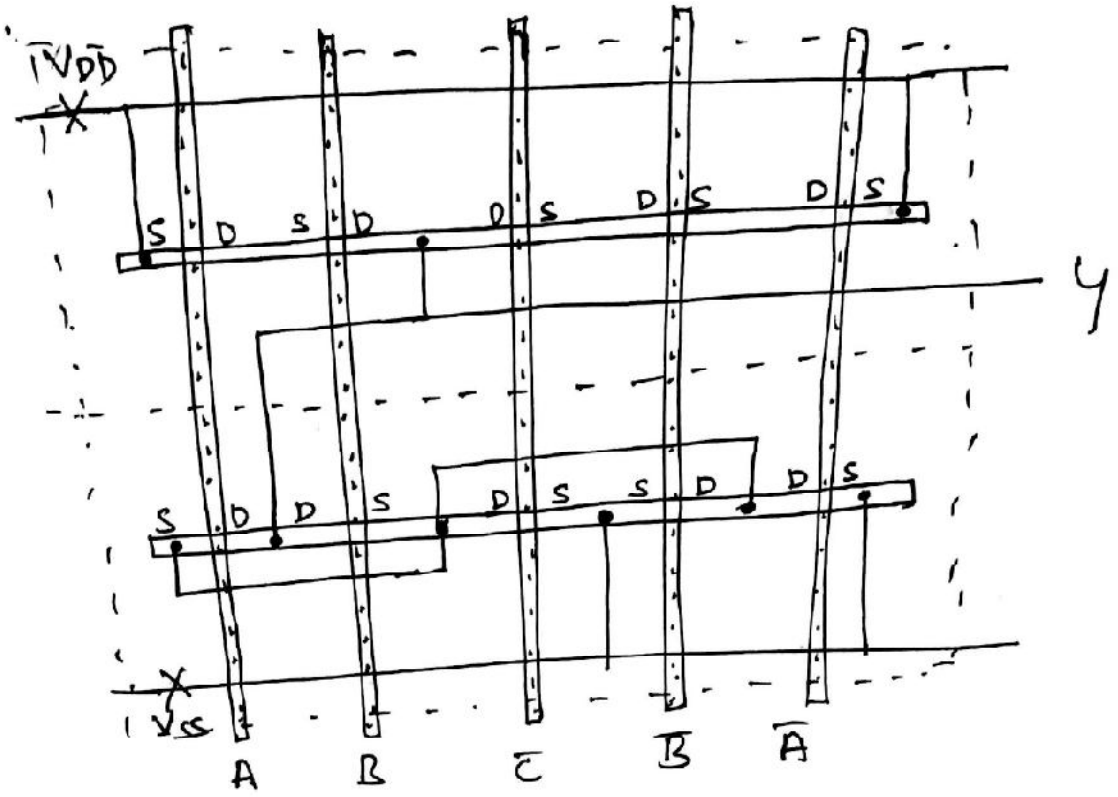
$$= \overline{\bar{A}\bar{B} \cdot \overline{ABC}} = \overline{\left(\bar{\bar{A}} + \bar{\bar{B}}\right) \cdot \left(\bar{A} + \bar{B} + \bar{C}\right)}$$

$$y = \overline{(A+B)(\bar{A}+\bar{B}+\bar{C})}$$

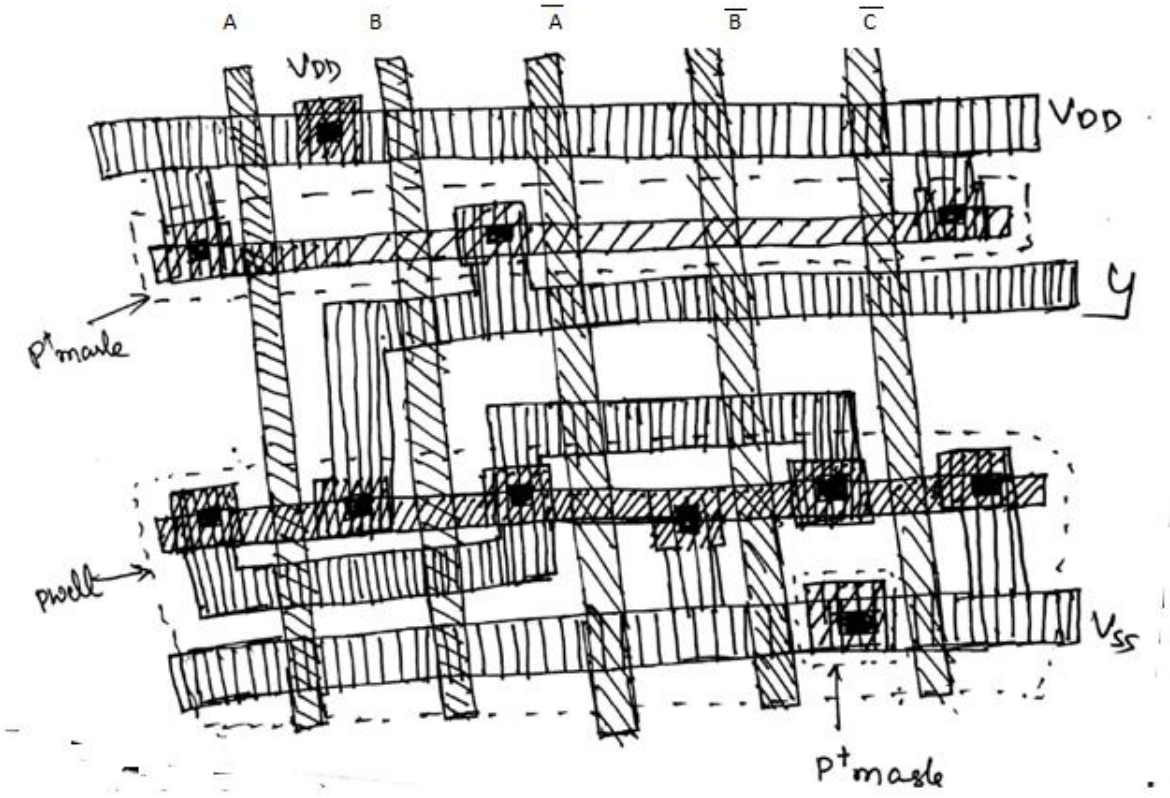
Schematic diagram



Stick Diagram

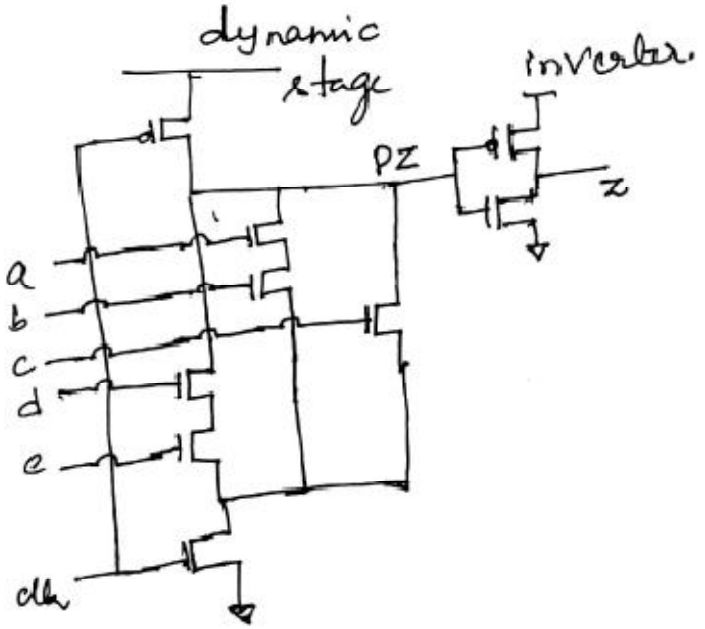


Layout:



3. a) Describe domino CMOS logic? How does it eliminate the issues related to cascading?

Domino CMOS logic structure consists of a dynamic logic block and its output drives the input of a static inverter as shown below.



— 02 marks

During precharge (clk=0), the output node of the dynamic gate is precharged high and the output of the buffer is low.

As subsequent logic blocks are fed from this buffer, transistors in subsequent logic blocks will be turned off during the precharge phase.

When the gate is evaluated the output will conditionally discharge, allowing the output of the

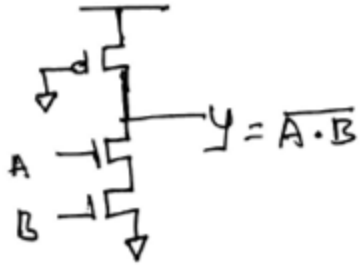
buffer to conditionally go high. Thus each gate in sequence can make almost one transition (1 to 0). Buffer makes only one transition from 0 to 1.

Any number of logic gates may be cascaded, provided that sequence can evaluate within the evaluate clock phase.

— 03 marks

b) Discuss the merits and demerits of Pseudo NMOS logic of 'NAND' gate.

Pseudo nMOS NAND gate.



— 0

Merits of pseudo nMOS logic.

① Number of transistors required to implement a logic is N+1, where as CMOS required 2N transistors

② Its Minimum load is only one unit gate load. as compared CMOS which has two unit gate load.

③ Since less number of transistors are required. can accommodate more have higher transistor density

— 02 marks

Demerits:

~~(2) Static to main drain transis~~

① Gain ratio of the n-driver transistor to p-transistor load R_{driver}/R_{load} has to be selected to yeild sufficient gain to generate consistent high and low logic levels.

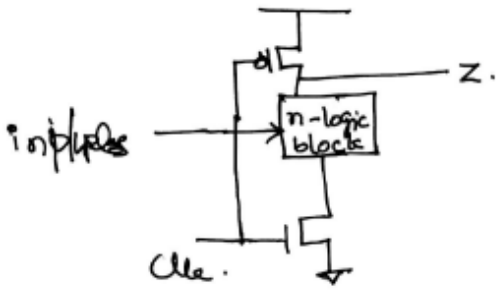
② Static power dissipation: PMOS is always on. whenever a pull down chain is on a static current flows in the circuit from V_{DD} to ground.

③ If minimum sized driver transistors are used the gain of the pull up has to be decreased to provide adequate noise margin leads to slow rise time of the gate.

– 02 marks

4. Explain the working principle of dynamic CMOS logic and clocked CMOS logic. Give their merits and demerits

- Basic dynamic CMOS gate is shown



– 01 marks

It consists of an n-transistor logic structure whose output node is precharged to V_{DD} by a p-transistor when clk = 0 and conditionally discharged by an n-transistor connected to V_{SS} when clk = 1.

02 – mar

Precharge phase occurs when clk = 0.

01 – marks

Evaluation phase occurs when clk = 1.

Inputs can change only during precharge but not during evaluat When the gates are precharged, the outputs nodes are charged to V_{DD}. During the evaluate phase, the output of the first gate will conditionally discharg Some delay will be incurred due to the finite pull-c time. Thus the precharged node (N_1) can discharge the output node of the following gate (N_2) before the first gate is correctly evaluated.

– 02 marks

merits:

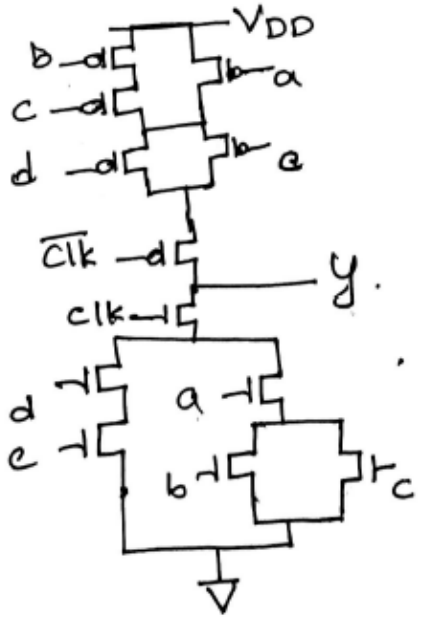
① Requires only N+2 number of transistors. where N is number of inputs. Hence transistor density is more.

Demerits:

Charge redistribution effect can corrupt the output node voltage. 01 marks

Clocked CMOS (C^2MOS)

Basic structure of C^2MOS is



— 01 marks

C^2MOS is a similar in structure of CMOS except one PMOS and nmos transistors in series with P-MOS and n-MOS logic. — 01 marks

Merits:

① Reduced dynamic power dissipation due to metal gate CMOS layout considerations

② Used to form clocked structures.

③ Used as a remedy for hot electron effects.

— 03 marks

Demerits:

Area requirements is large since it needs $2n+2$ transistors to implement a logic.

— 01 marks

5. Discuss bus arbitration logic for n-line bus.

→ Functional requirement of the bus arbitration logic is as given in the truth table

A_n	...	A_3	A_2	A_1	A_n^P	...	A_3^P	A_2^P	A_1^P
0	...	0	0	0	0	...	0	0	0
0	...	0	0	1	0	...	0	0	1
0	...	0	1	X	0	...	0	1	0
0	...	1	X	X	0	...	1	0	0
:		:	:	:	:		:	:	:
1	...	X	X	X	1	...	0	0	0

X → dont care.

If highest priority line A_n is high, then output line A_n^P will be hi and all other output lines are Lo (logic 0) irrespective of the state of other ~~outputs~~. input lines $A_1, A_2 \ldots A_{n-1}$. A_{n-1}^P will be high only when A_{n-1} is high and A_n is low.

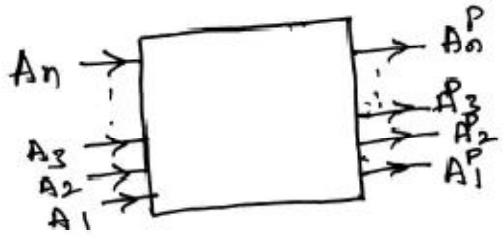
i.e., $A_n^P = A_n$

$A_{n-1}^P = \overline{A_n} A_{n-1}$

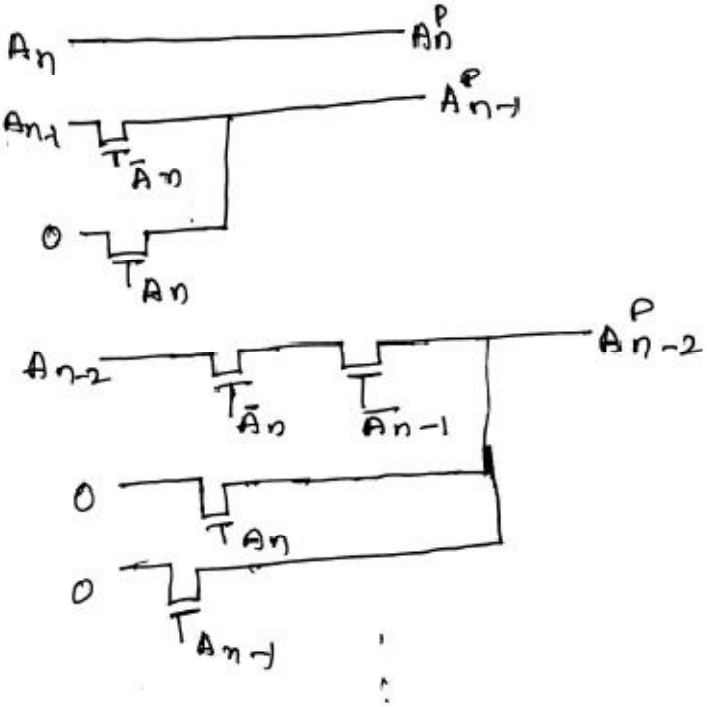
$A_{n-2}^P = \overline{A_n}\,\overline{A_{n-1}} A_{n-2}$.

$A_1^P = \overline{A_0}\,\overline{A_{n-1}}\,\overline{A_{n-2}} \ldots A_1$

→ 03 marks



Implementation of this circuit is as follows.



schematic diagram

A regular structure having been arrived at, the requirements for each cell may be expressed as follows:

$$A_i^p = \begin{cases} g_{i+1} & \text{if } A_i = 1 \\ \text{or } 0 & \text{otherwise} \end{cases}$$

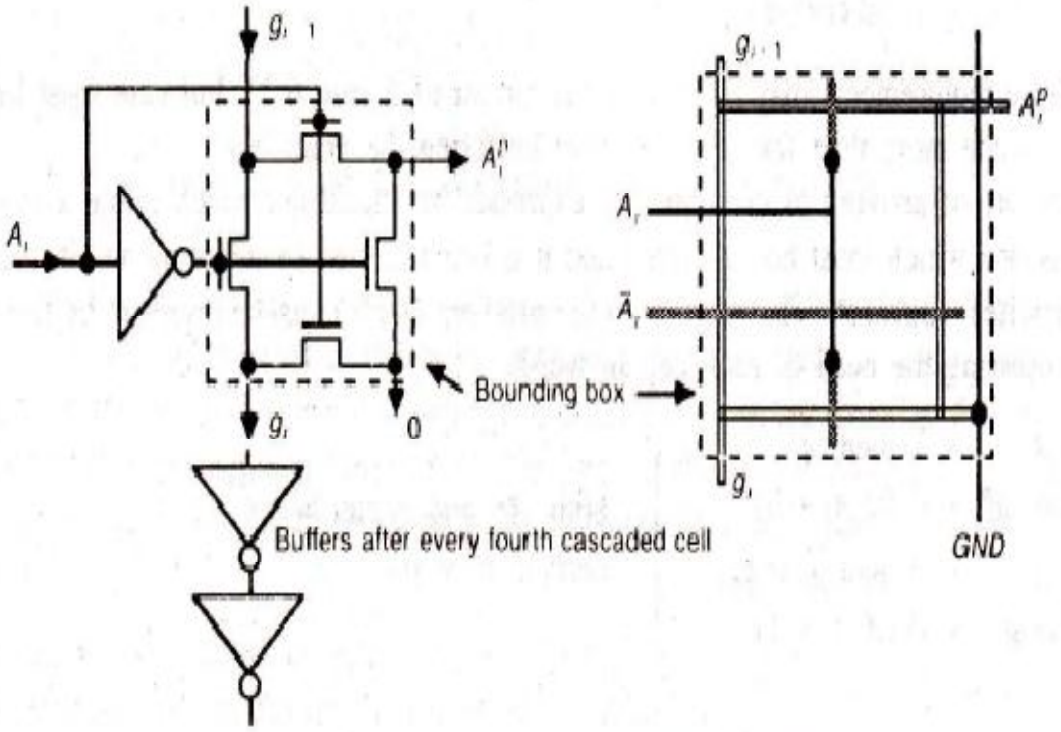
$$g_i = \begin{cases} 0 & \text{if } A_i = 1 \\ \text{or } g_{i+1} & \text{otherwise} \end{cases}$$

Can be reformulated as

If A_i = 1 then $A_i^p = g_{i+1}$,
else A_i^p = 0 (if A_i = 0)

If A_i = 0 then $g_i = g_{i+1}$
else g_i = 0 (if A_i = 1)

} both A_i^p and g_i can be derived from g_{i+1}



(a) Circuit (b) Stick diagram

—04 marks

Contd.

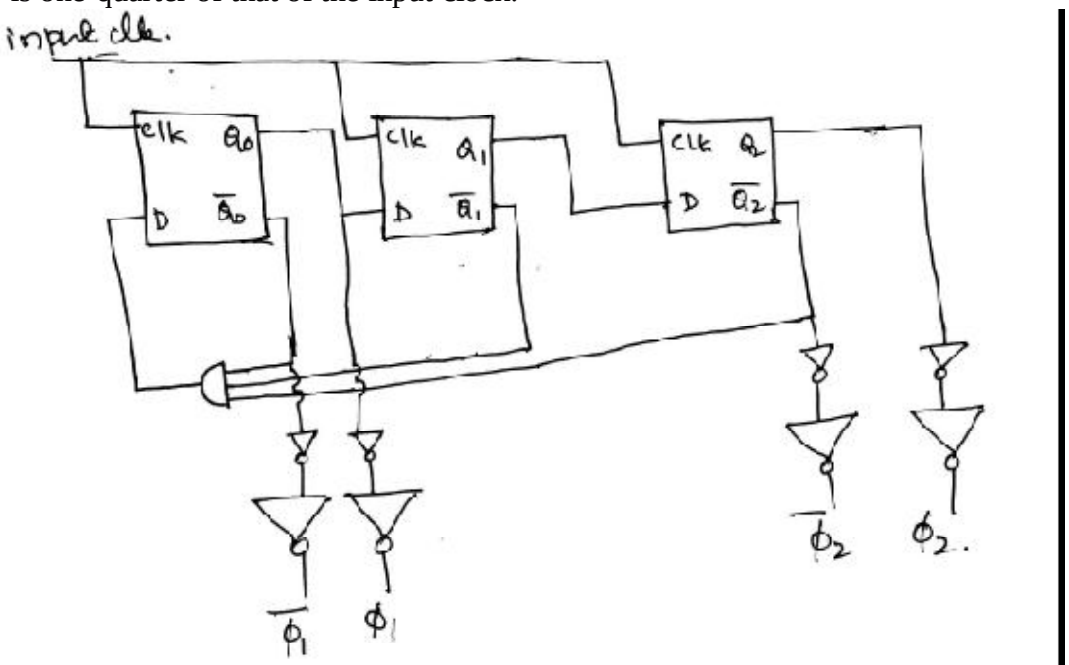
6. a) Discuss the architectural issues to be followed in the design of a VLSI subsystem.

→ The architectural issues of subsystem design

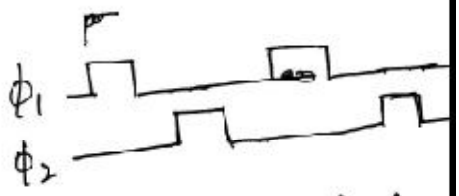
① Define the requirements
② Partition the overall architecture into appropriate subsystem.
③ Consider communication paths carefully in order to develop sensible interrelationships between subsystems.
④ Draw the floorplan of how the system is to map onto the silicon.
⑤ Aim for regular structures. For maximum replicab
⑥ Draw the ~~stickable~~ stick diagrams and ~~max~~ symbolic diagrams.
⑦ Convert each cell to a layout.
⑧ Carry out a design rule check.
⑨ Simulate the performance of each cell.

b) Explain two-phase clock signal generator using D flip-flops.

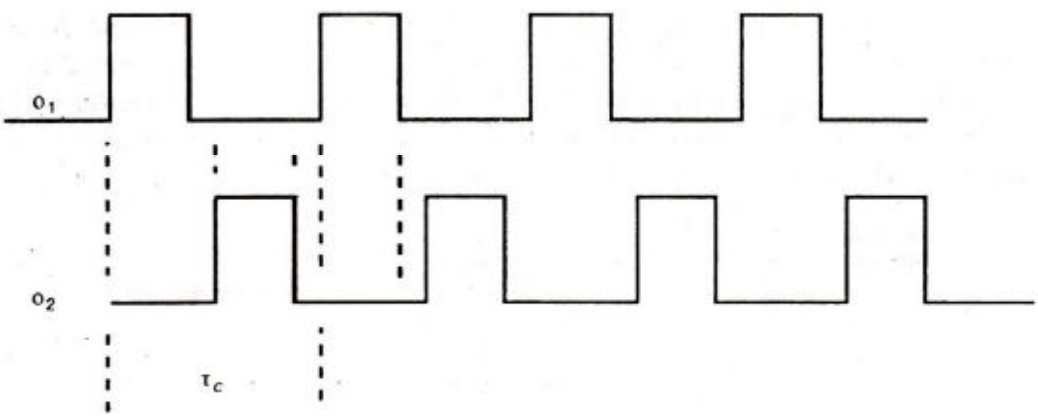
A number of techniques are used to generate the two clock phases. One popular method is illustrated in figure given below and it will be seen that the output frequency is one-quarter of that of the input clock.



steps	clk	Q_0	Q_1	Q_2
0	↑	0	0	0
1	↑	1	0	0
2	↑	0	1	0
3	↑	0	0	1
4	↑	0	0	0
5	↑	1	0	0
6	↑	0	1	0
7	↑	0	0	1
8	↑	0	0	0
9	↑	1	0	0



Non overlapping clock Signals.



A very simple arrangement using combinational logic and generating a two-phase clock at the frequency of a single-phase input clock is set out in following figure