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10CS33

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019

Logic Design

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO full questions from each part.

PART – A

- 1 a. Write a circuit diagram to show TTL NAND Gate and explain. (10 Marks)
 b. Define: i) duty cycle ii) universal logic gates iii) HDL iv) Tristate inverter. (04 Marks)
 c. Realize NOT, OR and AND gates using NOR gates. (06 Marks)
- 2 a. Write K-map for the minterm expression $f(A, B, C, D) = \sum_m (0, 1, 2, 3, 5, 7, 9, 10, 11, 13, 15)$ and write minimal SOP expression. (06 Marks)
 b. Explain static '1' hazard with an example. (04 Marks)
 c. Solve the following minterm expression using Quine McCluskey's method.
 $f(A, B, C, D) = \sum_m (0, 1, 4, 5, 7, 10, 11, 13, 14, 15)$. (10 Marks)
- 3 a. Show block diagram and circuit diagram representation for 4:1 MUX and explain. (08 Marks)
 b. Write circuit diagram for 2-bit magnitude comparator and explain. (06 Marks)
 c. Write verilog HDL code for 2:4 decodes. (04 Marks)
 d. What are programmable logic arrays? (02 Marks)
- 4 a. Write the circuit diagram for TTL clock and explain. (07 Marks)
 b. Write circuit diagram and explain JK MASTER-SLAVE FLIP-FLOP. (08 Marks)
 c. Write verilog HDL implementation for +ve edge triggered D-flip-flop. (05 Marks)

PART – B

- 5 a. Write verilog HDL code for implementing 3 bit shift right register using +ve edge triggered flip-flop. (06 Marks)
 b. Explain universal shift register with the help of suitable diagram. (10 Marks)
 c. Show the circuit diagram for Jhonson Counter. (04 Marks)
- 6 a. Write verilog HDL code for 3 bit binary counter. (06 Marks)
 b. What are i) Presettable counters ii) Counter modulus. (04 Marks)
 c. Show the circuit diagram for 4-bit synchronous counter and explain. Assume $n \geq 3$. (09 Marks)
 d. Why decoding gates are required in counter circuits. (01 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, $42+8=50$, will be treated as malpractice.

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- 7 a. What are Moore and Melay models in sequential circuits? (08 Marks)
b. Write K-map and state diagram for the asynchronous sequential circuit shown in Fig.Q.7(b). (10 Marks)

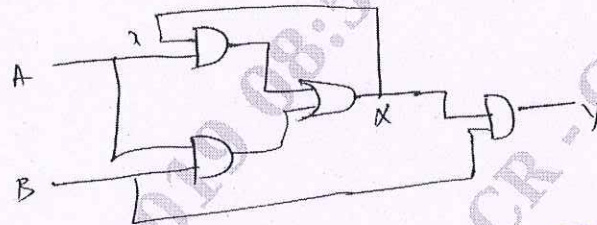


Fig.Q.7(b)

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- c. Define critical race and oscillation in asynchronous sequential circuits. (02 Marks)
- 8 a. Show the diagram and timing behaviour of o/p of dual slope A/P converter and explain. (10 Marks)
b. Find the: i) Resolution ii) Maximum conversion time of 8 bit converter given 500kHz clock and full scale o/p of 5V. (05 Marks)
c. How does R-ZR network convert digital input to analog o/p? Explain with the diagram. (05 Marks)
